Q657

T-52-30-08

National Semiconductor

74ACQ657 • 54ACTQ/74ACTQ657 Quiet Series Octal Bidirectional Transceiver with 8-Bit Parity Generator/Checker and TRI-STATE® Outputs

General Description

The 'ACQ/'ACTQ657 contains eight non-inverting buffers with TRI-STATE outputs and an 8-bit parity generator/checker. Intended for bus oriented applications, the device combines the '245 and the '280 functions in one package.

The 'ACQ/'ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

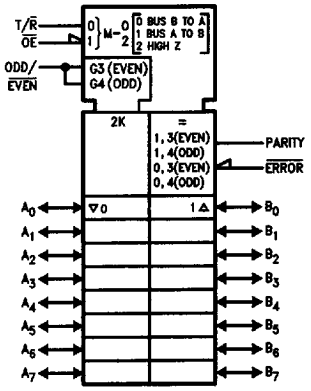
Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Combines the '245 and the '280 functions in one package
- 300 mil 24-pin slim dual-in-line package
- Outputs source/sink 24 mA
- 'ACTQ has TTL-compatible inputs
- Standard Military Drawing (SMD)
  — 'ACTQ657: 5962-92197

Ordering Code: See Section 8

Logic Symbols

IEEE/IEC



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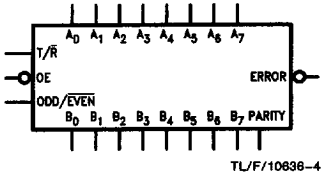

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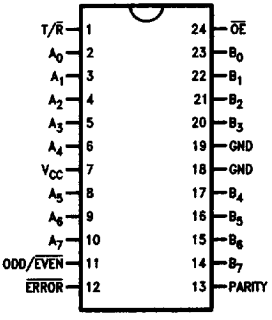
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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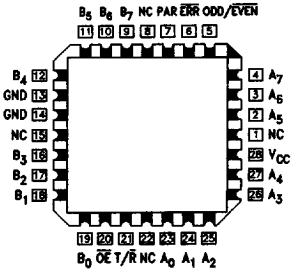
Pin Assignment for LCC



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Pin Names	Description
A_0–A_7	Data Inputs/TRI-STATE Outputs
B_0–B_7	Data Inputs/TRI-STATE Outputs
T/R	Transmit/Receive Input
OE	Enable Input
PARITY	Parity Input/TRI-STATE Output
ODD/EVEN	ODD/EVEN Parity Input
ERROR	Error TRI-STATE Output

Functional Description

The Transmit/Receive (T/$\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active HIGH) enables data from the A port to the B port; Receive (active LOW) enables data from the B port to the A port.

The Output Enable ($\overline{OE}$) input disables the parity and $\overline{ERROR}$ outputs and both the A and B ports by placing them in a HIGH-Z condition when the Output Enable input is HIGH.

When transmitting (T/$\overline{R}$ HIGH), the parity generator detects whether an even or odd number of bits on the A port are HIGH and compares these with the condition of the parity select (ODD/$\overline{EVEN}$). If the Parity Select is HIGH and an even number of A inputs are HIGH, the Parity output is HIGH.

In receiving mode (T/$\overline{R}$ LOW), the parity select and number of HIGH inputs on port B are compared to the condition of the Parity input. If an even number of bits on the B port are HIGH, the parity select is HIGH, and the PARITY input is HIGH, then $\overline{ERROR}$ will be HIGH to indicate no error. If an odd number of bits on the B port are HIGH, the parity select is HIGH, and the PARITY input is HIGH, the $\overline{ERROR}$ will be LOW indicating an error.

Function Table

Number of Inputs That Are High	Inputs			Input/ Output	Outputs	
	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$	Parity	$\overline{ERROR}$	Outputs Mode
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Immaterial	H	X	X	Z	Z	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Function Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High-Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

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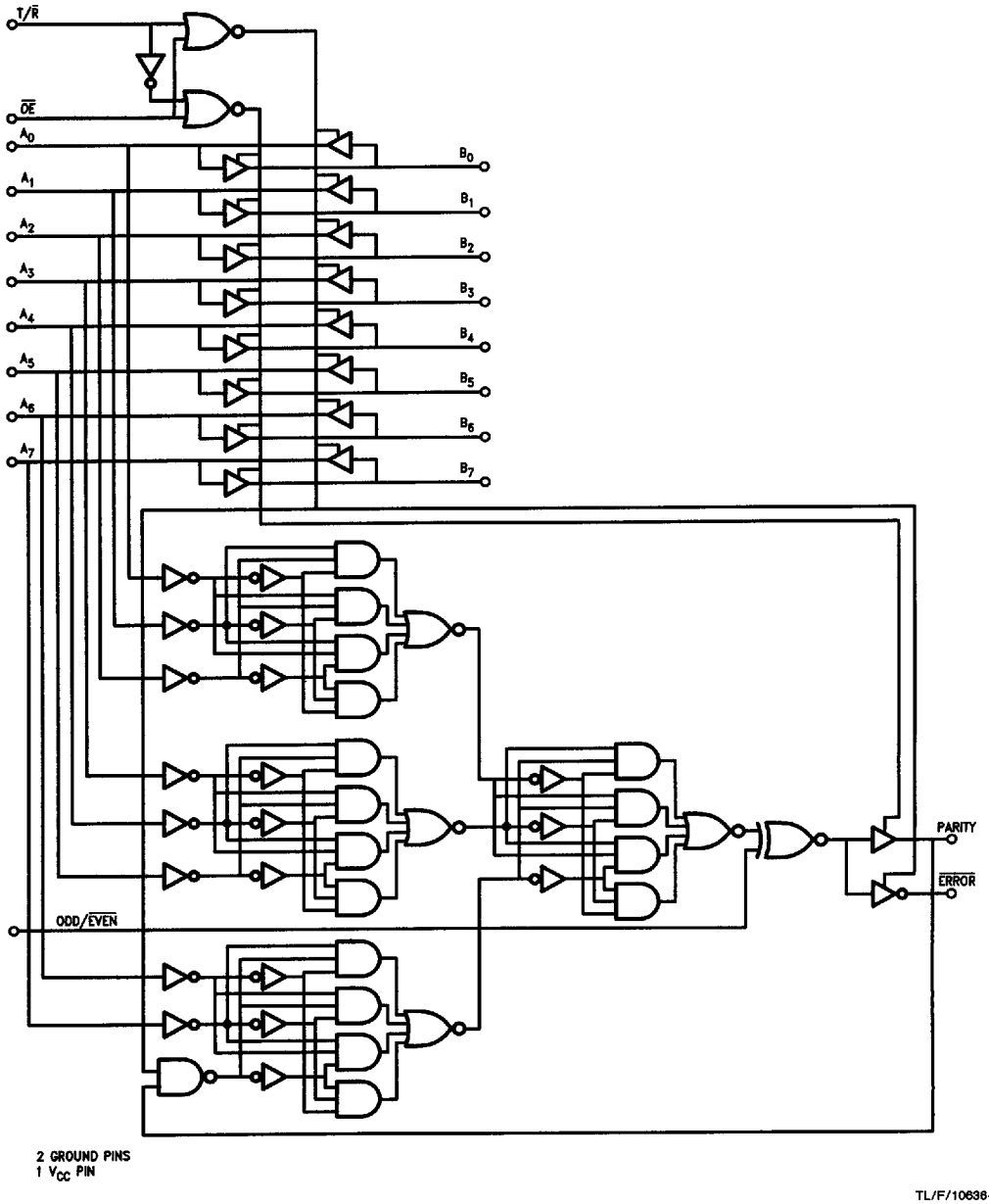
Functional Block Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 MA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT circuits outside databook specifications

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACQ	2.0V to 6.0V
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A) (Note 2)	
74ACQ/ACTQ	−40°C to +85°C
54ACTQ	−55°C to +125°C
Minimum Input Edge Rate ΔV/Δt	
'ACQ Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ΔV/Δt	
'ACTQ Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 2: All commercial packaging is not recommended for applications requiring greater than 200 temperature cycles from −65°C to +150°C

DC Characteristics for 'ACQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACQ T_A = +25°C Typ	74ACQ T_A = −40°C to +85°C Guaranteed Limits		Units	Conditions
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.76		I_{OH} −24 mA
		5.5		4.85	4.76		−24 mA

*Maximum of 8 outputs loaded; thresholds on input associated with output under test.

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DC Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACQ $T_A = +25°C$ Typ	74ACQ $T_A = +25°C$ Guaranteed Limits	74ACQ $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{OL}	Maximum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V	I_{OUT} = 50 μA
		3.0 4.5 5.5		0.36 0.36 0.36	0.44 0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current ($\overline{T/R}$, $\overline{OE}$, ODD/$\overline{EVEN}$ Inputs)	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND (Note 1)
I_{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80.0	μA	V_{IN} = V_{CC} or GND (Note 1)
I_{OZT}	Maximum I/O Leakage Current (A_n, B_n Inputs)	5.5		±0.6	±6.0	μA	V_I(OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5		V	*Figures 2-12, 13* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2		V	*Figures 2-12, 13* (Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	3.1	3.5		V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.9	1.5		V	(Notes 2, 4)

*Maximum of 8 outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

Note 2: Plastic DIP package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 5V. One output @ GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) Inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}) f = 1 MHz.

DC Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$ Typ	74ACTQ $T_A = +25°C$ Guaranteed Limits	54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current ($T/\overline{R}$, $\overline{OE}$, ODD/$\overline{EVEN}$ Inputs)	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZT}	Maximum I/O Leakage Current (A_n, B_n Inputs)	5.5		±0.6	±11.0	±6.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND (Note 1)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	*Figures 2-12, 13* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2			V	*Figures 2-12, 13* (Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	1.9	2.2			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Plastic DIP package.

Note 3: Max number of outputs defined as (n). n − 1 Data Inputs are driven 0V to 3V; one output @ GND

Note 4: Max number of Data Inputs (n) switching (n − 1) inputs switching 0V to 3V ('ACQ) Input-under-test switching; 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}) f = 1 MHz.

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AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = 25°C$, $C_L = 50$ pF			74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay A_n to B_n, B_n to A_n	3.3	2.5	8.0	11.5	2.5	12.0	ns	2-3, 4
		5.0	1.5	5.0	7.5	1.5	8.0		
t_{PLH}, t_{PHL}	Propagation Delay A_n to Parity	3.3	3.0	11.5	16.5	3.0	17.0	ns	2-3, 4
		5.0	2.0	7.0	10.5	2.0	11.0		
t_{PLH}, t_{PHL}	Propagation Delay ODD/$\overline{\text{EVEN}}$ to PARITY	3.3	3.0	10.0	15.0	3.0	15.5	ns	2-3, 4
		5.0	2.5	6.5	10.0	2.5	10.5		
t_{PLH}, t_{PHL}	Propagation Delay ODD/$\overline{\text{EVEN}}$ to $\overline{\text{ERROR}}$	3.3	3.0	10.0	15.0	3.0	15.5	ns	2-3, 4
		5.0	2.5	6.5	10.0	2.5	10.5		
t_{PLH}, t_{PHL}	Propagation Delay B_n to $\overline{\text{ERROR}}$	3.3	3.5	11.5	16.0	3.5	16.5	ns	2-3, 4
		5.0	2.5	7.0	10.5	2.5	11.0		
t_{PLH}, t_{PHL}	Propagation Delay PARITY to $\overline{\text{ERROR}}$	3.3	3.0	9.0	13.5	3.0	14.0	ns	2-3, 4
		5.0	2.0	6.0	9.0	2.0	9.5		
t_{PZH}, t_{PZL}	Output Enable Time $\overline{OE}$ to A_n/B_n	3.3	2.5	9.0	13.5	2.5	14.0	ns	2-5, 6
		5.0	2.0	6.0	9.0	2.0	9.5		
t_{PHZ}, t_{PLZ}	Output Disable Time $\overline{OE}$ to A_n/B_n	3.3	1.0	8.5	13.0	1.0	13.5	ns	2-5, 6
		5.0	1.0	5.5	8.5	1.0	9.0		
t_{PZH}, t_{PZL}	Output Enable Time $\overline{OE}$ to $\overline{\text{ERROR}}$ (Note 1)	3.3	2.5	9.0	13.5	2.5	14.0	ns	2-5, 6
		5.0	2.0	6.0	9.0	2.0	9.5		
t_{PHZ}, t_{PLZ}	Output Disable Time $\overline{OE}$ to $\overline{\text{ERROR}}$	3.3	1.0	8.5	13.0	1.0	13.5	ns	2-5, 6
		5.0	1.0	5.5	8.5	1.0	9.0		
t_{PZH}, t_{PZL}	Output Enable Time $\overline{OE}$ to PARITY	3.3	2.5	9.0	13.5	2.5	14.0	ns	2-5, 6
		5.0	2.0	6.0	9.0	2.0	9.5		
t_{PHZ}, t_{PLZ}	Output Disable Time $\overline{OE}$ to PARITY	3.3	1.0	8.5	13.0	1.0	13.5	ns	2-5, 6
		5.0	1.0	5.5	8.5	1.0	9.0		
t_{OSHL}, t_{OSLH}	Output to Output Skew** A_n, B_n to B_n, A_n	3.3		1.0	1.5		1.5	ns	
		5.0		0.5	1.0		1.0		

*Voltage Range 3.3 is 3.3V ±0.3V

Voltage Range 5.0 is 5.0V ±0.5V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design. Not tested.

Note 1: These delay times reflect the TRI-STATE recovery time only and not the signal time through the buffers or the parity check circuitry. To assure VALID information at the $\overline{\text{ERROR}}$ pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the $\overline{\text{ERROR}}$ output after the $\overline{\text{ERROR}}$ pin has been enabled (Output Enable times). VALID data at the $\overline{\text{ERROR}}$ pin ≥ (A to PARITY) + (Output Enable Time).

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = 25°C$, $C_L = 50$ pF			54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay A_n to B_n, B_n to A_n	5.0	1.5	5.0	8.0	1.5	9.0	1.5	8.5	ns	2-3, 4
t_{PLH}, t_{PHL}	Propagation Delay A_n to Parity	5.0	2.5	7.5	11.0	1.5	13.5	2.5	11.5	ns	2-3, 4
t_{PLH}, t_{PHL}	Propagation Delay ODD/$\overline{\text{EVEN}}$ to PARITY	5.0	2.5	6.5	10.5	1.5	10.5	2.5	11.0	ns	2-3, 4
t_{PLH}, t_{PHL}	Propagation Delay ODD/$\overline{\text{EVEN}}$ to $\overline{\text{ERROR}}$	5.0	2.5	6.5	10.5	1.5	11.0	2.5	11.0	ns	2-3, 4
t_{PLH}, t_{PHL}	Propagation Delay B_n to $\overline{\text{ERROR}}$	5.0	3.0	7.5	11.0	1.5	13.5	3.0	11.5	ns	2-3, 4
t_{PLH}, t_{PHL}	Propagation Delay PARITY to $\overline{\text{ERROR}}$	5.0	2.0	6.0	9.5	1.5	10.5	2.0	10.0	ns	2-3, 4
t_{PZH}, t_{PZL}	Output Enable Time $\overline{OE}$ to A_n/B_n	5.0	2.0	6.0	9.5	1.5	12.0	2.0	10.0	ns	2-5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time $\overline{OE}$ to A_n/B_n	5.0	1.0	5.0	9.0	1.5	9.0	1.0	9.5	ns	2-5, 6
t_{PZH}, t_{PZL}	Output Enable Time $\overline{OE}$ to $\overline{\text{ERROR}}$ (Note 1)	5.0	2.0	6.0	9.5	1.5	11.5	2.0	10.0	ns	2-5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time $\overline{OE}$ to $\overline{\text{ERROR}}$	5.0	1.0	6.0	9.0	1.5	9.0	1.0	9.5	ns	2-5, 6
t_{PZH}, t_{PZL}	Output Enable Time $\overline{OE}$ to PARITY	5.0	2.0	6.0	9.5	1.5	11.5	2.0	10.0	ns	2-5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time $\overline{OE}$ to PARITY	5.0	1.0	5.0	9.0	1.5	8.5	1.0	9.5	ns	2-5, 6
t_{OSHL}, t_{OSLH}	Output to Output Skew** A_n, B_n to B_n, A_n	5.0		0.5	1.0				1.0	ns	

*Voltage Range 5.0 is 5.0V ±0.5V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design. Not tested.

Note 1: These delay times reflect the TRI-STATE recovery time only and not the signal time through the buffers or the parity check circuitry. To assure VALID information at the $\overline{\text{ERROR}}$ pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the $\overline{\text{ERROR}}$ output after the $\overline{\text{ERROR}}$ pin has been enabled (Output Enable times). VALID data at the $\overline{\text{ERROR}}$ pin ≥ (A to PARITY) + (Output Enable Time).

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	160.0	pF	$V_{CC} = 5.0V$