MOTOROLA

Advance Information

256K x 4 CMOS Dynamic RAM Page Mode

514256A

Commercial Plus and Mil/Aero Applications

ELECTRICALLY TESTED PER:
MPG514256A

The 514256A is a 1.0µ CMOS high-speed, dynamic random access memory. It is organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The 514256A requires only nine address lines; row and column address inputs are multiplexed. The 514256A is available in a 300 mil, 20 lead ceramic DIL and in a 350 x 675 mil, 20/26 lead surface-mount LCC package.

- Three-State Data Outputs
- Fast Page Mode
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle Refresh: 514256A = 8 ms
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): 514256A-8 = 80 ns (Max)
  514256A-9 = 90 ns (Max)
  514256A-11 = 110 ns (Max)
  514256A-12 = 120 ns (Max)
- Low Active Power Dissipation: 514256A-8 = 495 mW (Max)
  514256A-9 = 440 mW (Max)
  514256A-11 = 385 mW (Max)
  514256A-12 = 330 mW (Max)
- Low Standby Power Dissipation: 514256A = 5.5 mW (Max, CMOS Levels)

AVAILABLE AS
1) JAN: N/A
2) SMD: N/A
3) 883:514256A-XX/BXAJC
X = CASE OUTLINE AS FOLLOWS:
PACKAGE: DIL:R
LCC: U
XX = Speed in ns (8, 9, 11, 12)
The letter "M" appears after the speed on LCC.

PIN NAMES

A0-A8	Address Inputs
DQ0-DQ3	Data Input/Outputs
$\overline{G}$	Output Enable
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No Connection

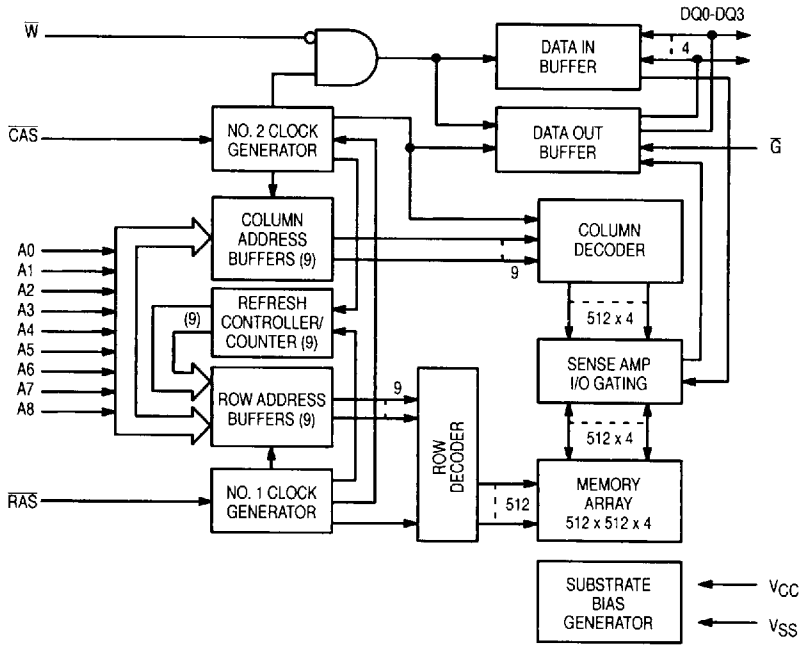
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1.0 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1.0 to +7.0	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	1.0	W
Operating Temperature Range	T_A	–55 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



PIN ASSIGNMENTS

Function	Case 729-02 DIL	Case 756E-01 LCCC	Burn-In Condition		Function	Case 729-02 DIL	Case 756E-01 LCCC	Burn-In Condition	
			Static	Dynamic				Static	Dynamic
DQ0	1	1	High	A21	A4	11	14	Low	1/2 A3
DQ1	2	2	High	A21	A5	12	15	Low	1/2 A4
$\overline{W}$	3	3	High	$\overline{A20}$	A5	13	16	Low	1/2 A5
$\overline{RAS}$	4	4	High	1.6µs / 4µs	A7	14	17	Low	1/2 A6
NC	5	5	NC	NC	A8	15	18	Low	1/2 A7
A0	6	9	Low	250kHz	$\overline{G}$	16	22	V_{CC}	V_{CC}
A1	7	10	Low	1/2 A0	$\overline{CAS}$	17	23	High	0.8µs / 1.2µs
A2	8	11	Low	1/2 A1	DQ2	18	24	High	A21
A3	9	12	Low	1/2 A2	DQ3	19	25	High	A21
V_{CC}	10	13	V_{CC}	V_{CC}	V_{SS}	20	26	Gnd	Gnd

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = −55 to +125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	—	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
514256A-8, t_{RC} = 150 ns		—	90		
514256A-9, t_{RC} = 170 ns		—	80		
514256A-11, t_{RC} = 200 ns		—	70		
514256A-12, t_{RC} = 220 ns		—	60		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	4.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CAS}$ = V_{IH})	I_{CC3}			mA	2
514256A-8, t_{RC} = 150 ns		—	90		
514256A-9, t_{RC} = 170 ns		—	80		
514256A-11, t_{RC} = 200 ns		—	70		
514256A-12, t_{RC} = 220 ns		—	60		
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL})	I_{CC4}			mA	2, 3
514256A-8, t_{PC} = 45 ns		—	70		
514256A-9, t_{PC} = 50 ns		—	60		
514256A-11, t_{PC} = 60 ns		—	50		
514256A-12, t_{PC} = 65 ns		—	40		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} −0.2 V) 514256A	I_{CC5}	—	2.0	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
514256A-8, t_{RC} = 150 ns		—	90		
514256A-9, t_{RC} = 170 ns		—	80		
514256A-11, t_{RC} = 200 ns		—	70		
514256A-12, t_{RC} = 220 ns		—	60		
Input Leakage Current (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	−10	10	µA	
Output Leakage Current ($\overline{CAS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	−10	10	µA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A8	C_{in}	5.0	pF	4
	$\overline{G}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		7.0	pF	4
Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	DQ0-DQ3	C_{out}	7.0	pF	4

NOTES:

1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Measured with one address transition per page mode cycle.
4. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = −55 to +125°C, Unless Otherwise Noted)

READ, WRITE, AND READ-WRITE CYCLES

Parameter	Symbol		514256A-8		514256A-9		514256A-11		514256A-12		Unit	Notes
	Standard	Alt.	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	150	—	170	—	200	—	220	—	ns	5-9
Read-Write Cycle Time	t_{RELREL}	t_{RMW}	205	—	225	—	265	—	275	—	ns	5-9
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	50	—	60	—	65	—	ns	5-8
Fast Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRMW}	100	—	105	—	120	—	125	—	ns	5-8
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	80	—	90	—	110	—	120	ns	5-8, 10, 11
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	25	—	25	—	25	—	25	ns	5-8, 10, 12
Access Time from Column Address	t_{AVQV}	t_{AA}	—	40	—	45	—	55	—	60	ns	5-8, 10, 13
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	40	—	45	—	55	—	60	ns	5-8, 10
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	0	—	ns	5-8, 10
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	0	20	ns	5-8, 14
Transition Time (Rise and Fall)	t_T	t_T	—	50	—	50	—	50	—	50	ns	5-8
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	60	—	70	—	80	—	90	—	ns	5-8
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	80	10,000	90	10,000	110	10,000	120	10,000	ns	5-8
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	80	100,000	90	100,000	110	100,000	120	100,000	ns	5-8
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	25	—	25	—	ns	5-8
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	80	—	90	—	110	—	120	—	ns	5-8
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	25	10,000	25	10,000	30	10,000	35	10,000	ns	5-8
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	25	60	25	70	30	80	35	95	ns	5-8, 15
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	40	15	45	20	55	20	60	ns	5-8, 16
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	10	—	10	—	ns	5-8
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	10	—	10	—	15	—	15	—	ns	5-8
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	10	—	ns	5-8

READ, WRITE, AND READ-WRITE CYCLES (continued)

Parameter	Symbol		514256A-8		514256A-9		514256A-11		514256A-12		Unit	Notes
	Standard	Alt.	Min	Max	Min	Max	Min	Max	Min	Max		
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	0	—	ns	5-8
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	15	—	15	—	ns	5-8
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	0	—	ns	5-8
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	20	—	20	—	ns	5-8
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	60	—	65	—	80	—	85	—	ns	5-8
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	40	—	45	—	55	—	60	—	ns	5-8
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	0	—	ns	5-8
Read Command Hold Time	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	0	—	ns	5-8, 17
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	0	—	ns	5-8, 17
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	15	—	15	—	20	—	20	—	ns	5-8
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	60	—	65	—	80	—	85	—	ns	5-8
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	20	—	20	—	20	—	ns	5-8
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	25	—	25	—	ns	5-8
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	25	—	25	—	ns	5-8
Data In Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	0	—	ns	5-8, 18
Data In Hold Time	t_{CELDX}	t_{DH}	15	—	20	—	20	—	20	—	ns	5-8, 18
Data In Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	60	—	65	—	80	—	85	—	ns	5-8
Refresh Period 514256A	t_{RVRV}	t_{RFSH}	—	8.0	—	8.0	—	8.0	—	8.0	ms	5-8
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	0	—	ns	5-8, 19
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	50	—	50	—	60	—	60	—	ns	5-8, 19
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	100	—	120	—	140	—	150	—	ns	5-8, 19

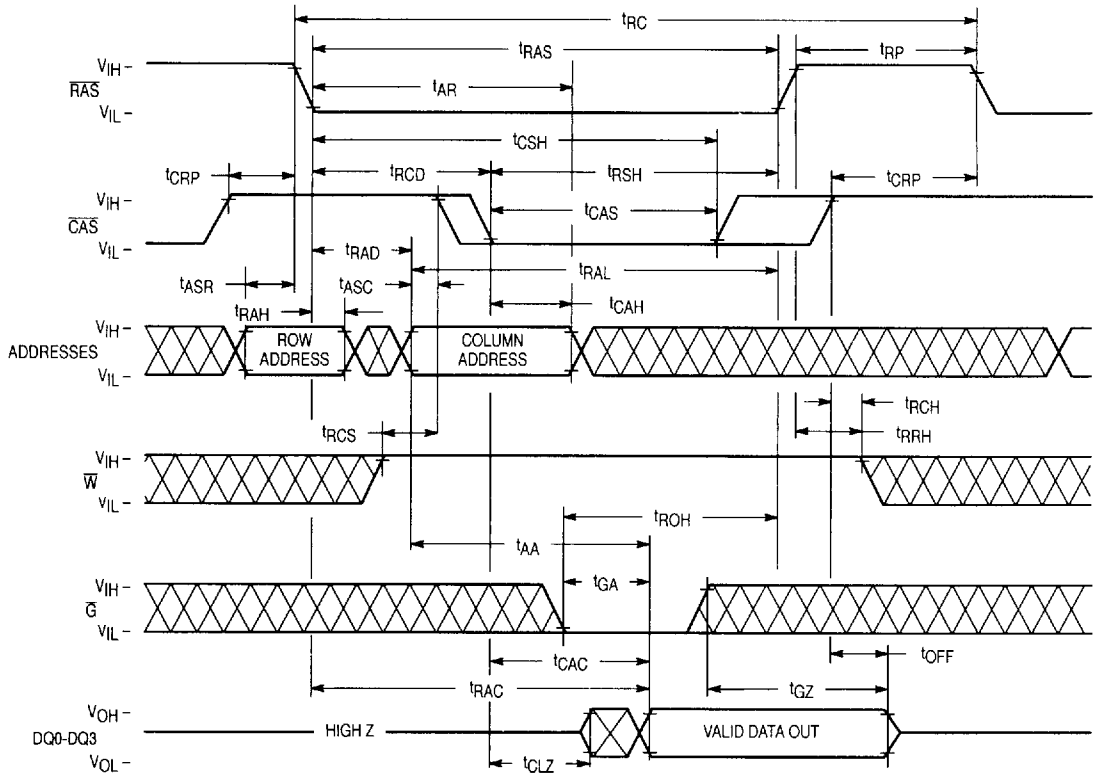
READ, WRITE, AND READ-WRITE CYCLES (continued)

Parameter	Symbol		514256A-8		514256A-9		514256A-11		514256A-12		Unit	Notes
	Standard	Alt.	Min	Max	Min	Max	Min	Max	Min	Max		
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	70	—	75	—	90	—	95	—	ns	5-8, 19
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	10	—	10	—	ns	5-8
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	—	30	—	30	—	30	—	ns	5-8
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	0	—	ns	5-8
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	—	40	—	50	—	50	—	ns	5-8
$\overline{RAS}$ Hold Time Referenced to $\overline{G}$	t_{GLREH}	t_{ROH}	10	—	10	—	20	—	20	—	ns	5-8
$\overline{G}$ Access Time	t_{GLQV}	t_{GA}	—	20	—	20	—	25	—	25	ns	5-8
$\overline{G}$ to Data Delay	t_{GLHDX}	t_{GD}	20	—	20	—	25	—	25	—	ns	5-8
Output Buffer Turn-Off Delay Time from $\overline{G}$	t_{GHQZ}	t_{GZ}	0	25	0	25	0	30	0	30	ns	5-8, 14
$\overline{G}$ Command Hold Time	t_{WLGL}	t_{GH}	25	—	25	—	30	—	30	—	ns	5-8

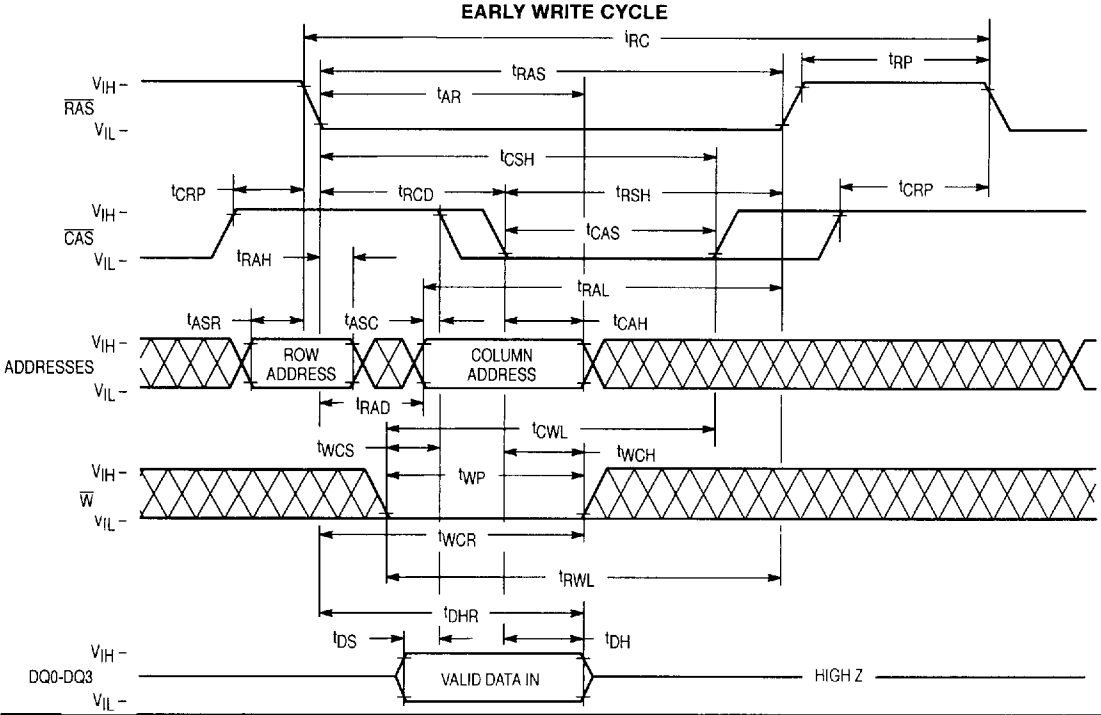
NOTES:

5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measures between V_{IH} and V_{IL}.
6. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
7. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
8. AC measurements t_T = 5.0 ns.
9. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
10. Measured with a current load equivalent to 2 TTL (–200 µA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
11. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
12. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
13. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
14. t_{OFF} (max) and/or t_{GZ} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
15. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
16. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.
17. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
18. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{W}$ leading edge in delayed write or read-write cycles.
19. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

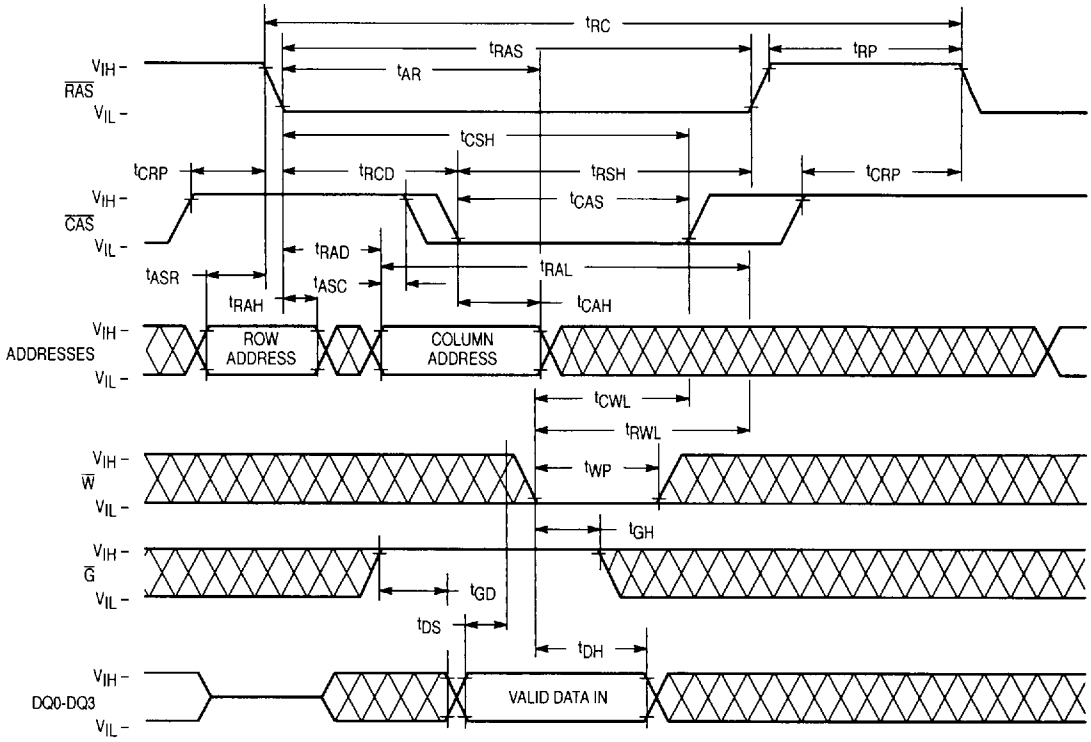
READ CYCLE



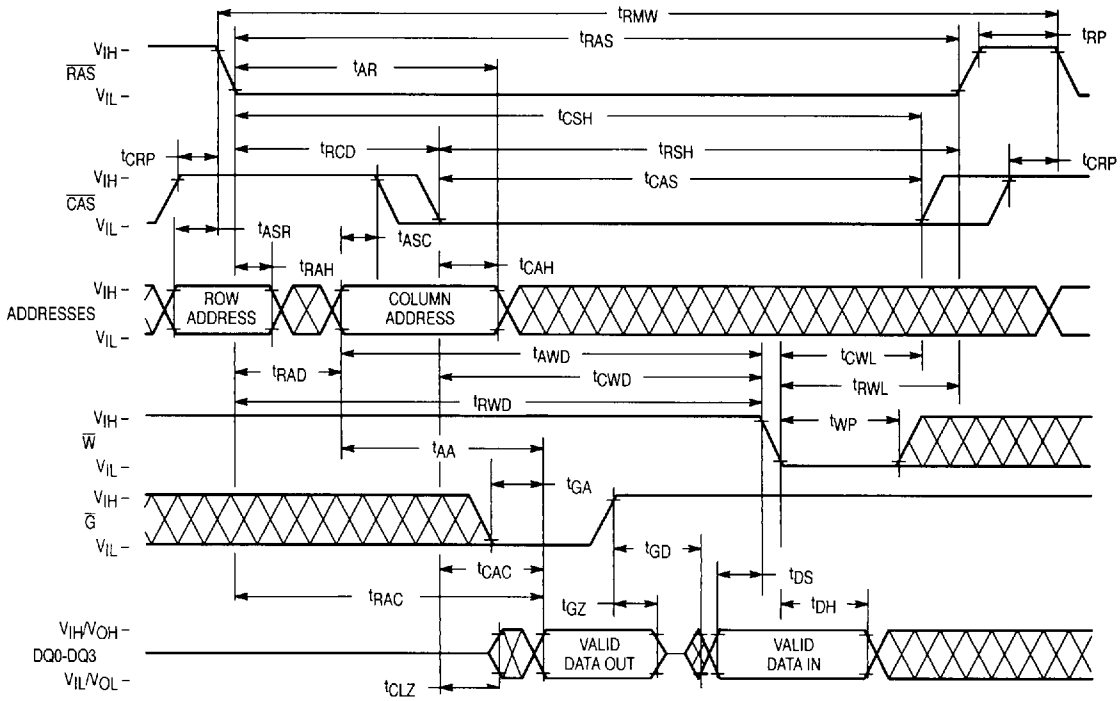
EARLY WRITE CYCLE



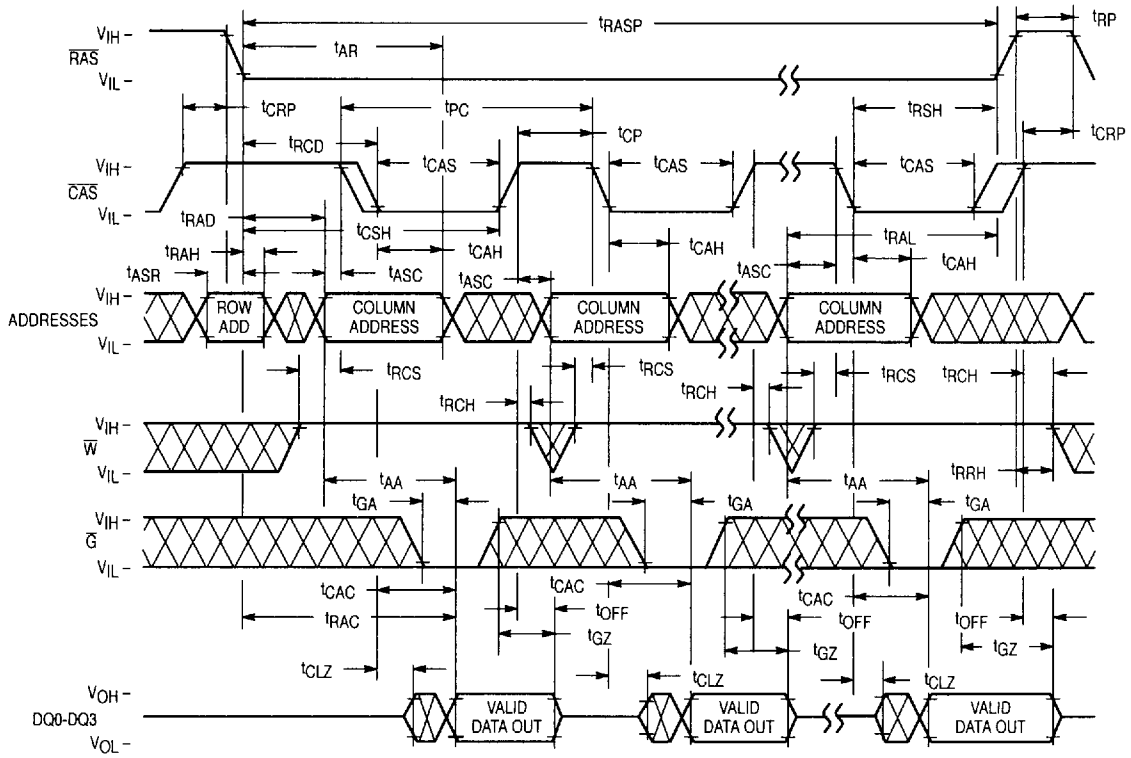
$\overline{G}$ CONTROLLED LATE WRITE CYCLE



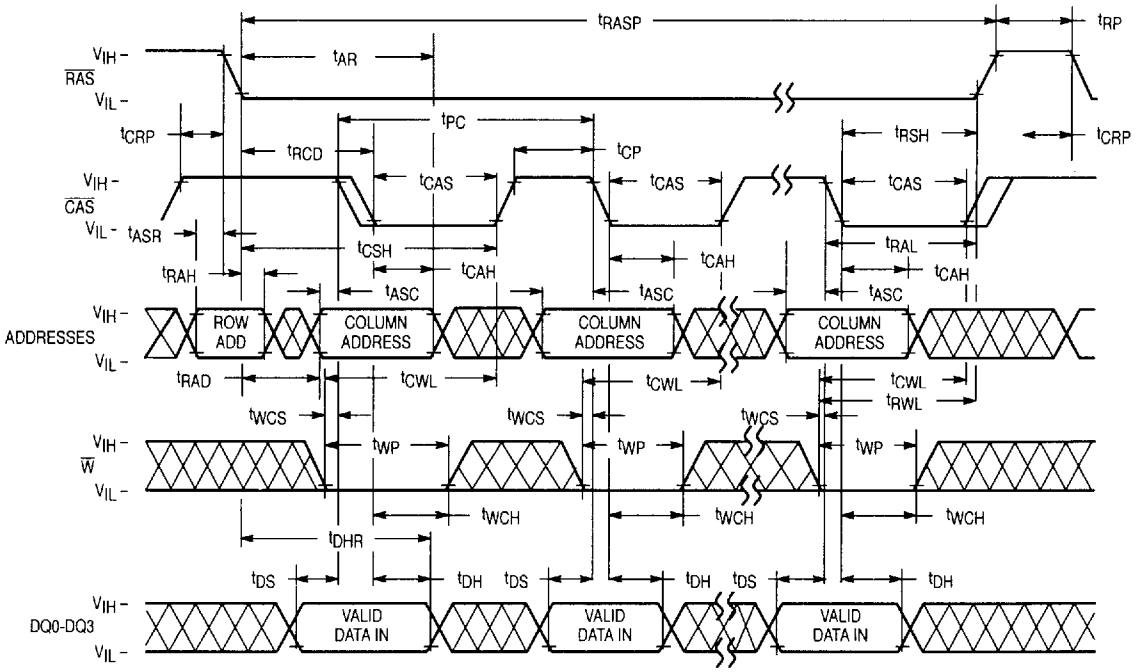
READ-WRITE CYCLE



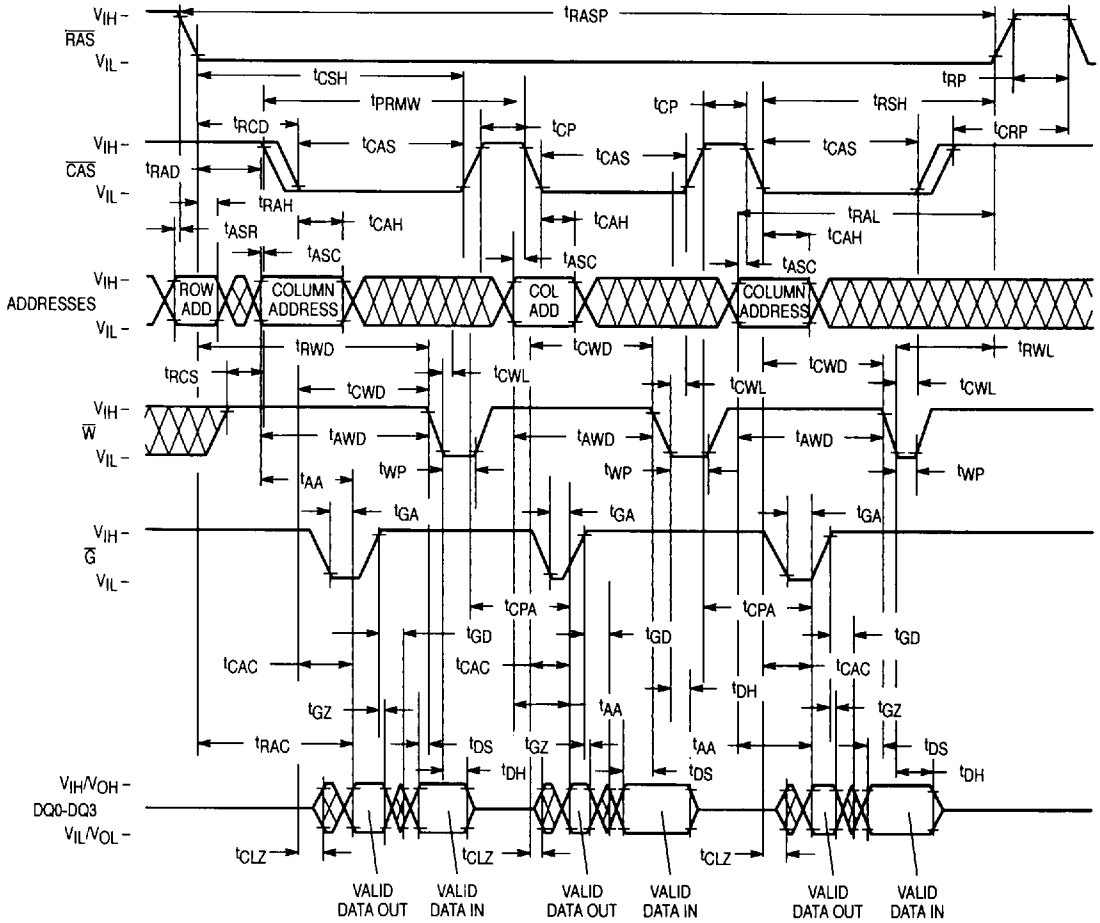
FAST PAGE MODE READ CYCLE



FAST PAGE MODE EARLY WRITE CYCLE

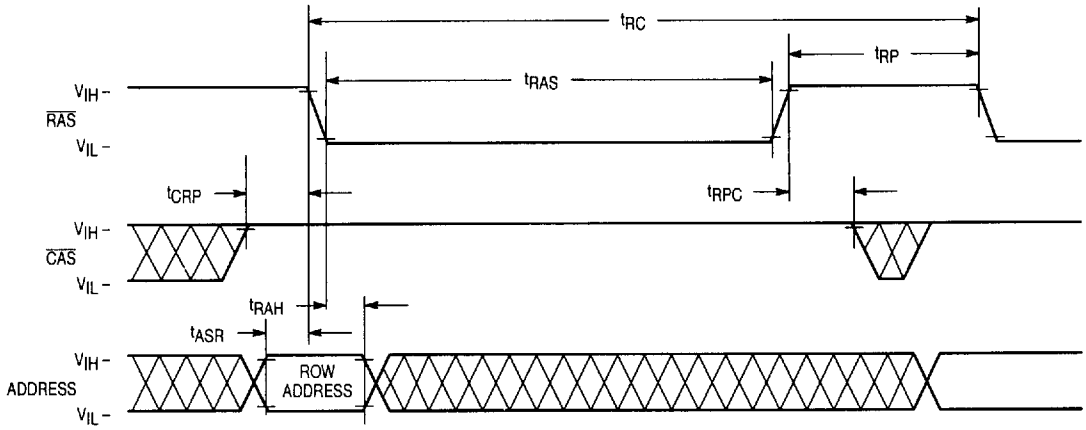


FAST PAGE MODE READ-WRITE CYCLE

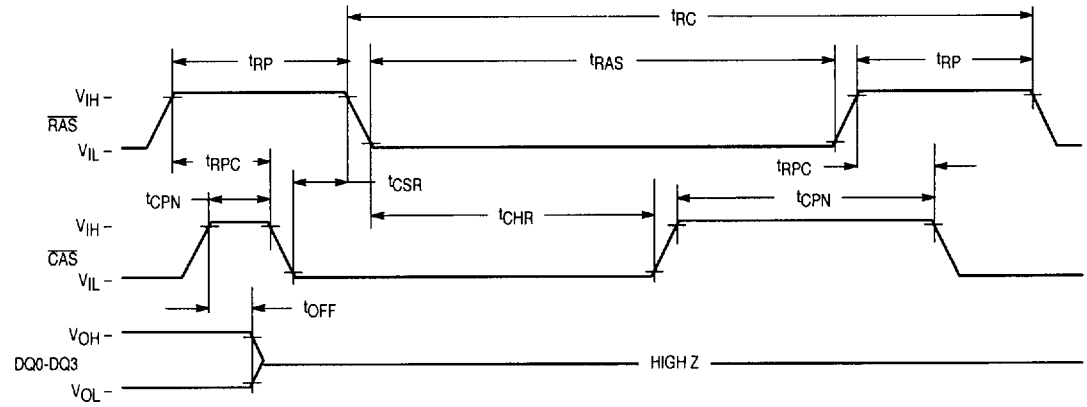


MOTOROLA SC {MEMORY/ASI 65E D

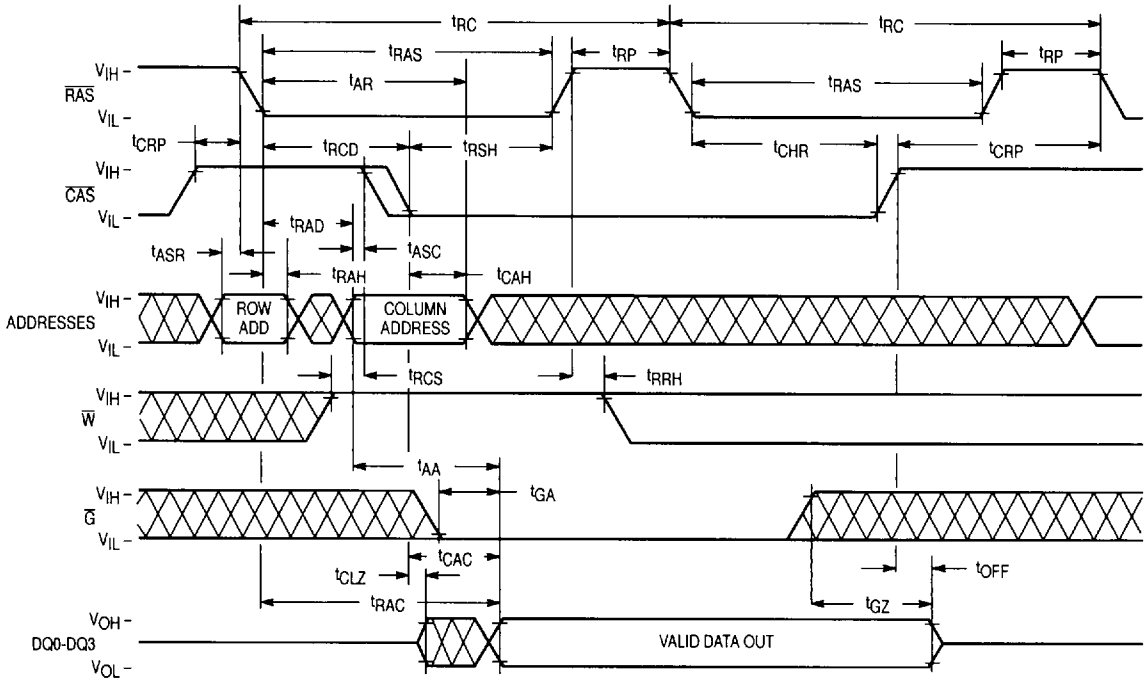
$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{W}$ and $\overline{G}$ are Don't Care)



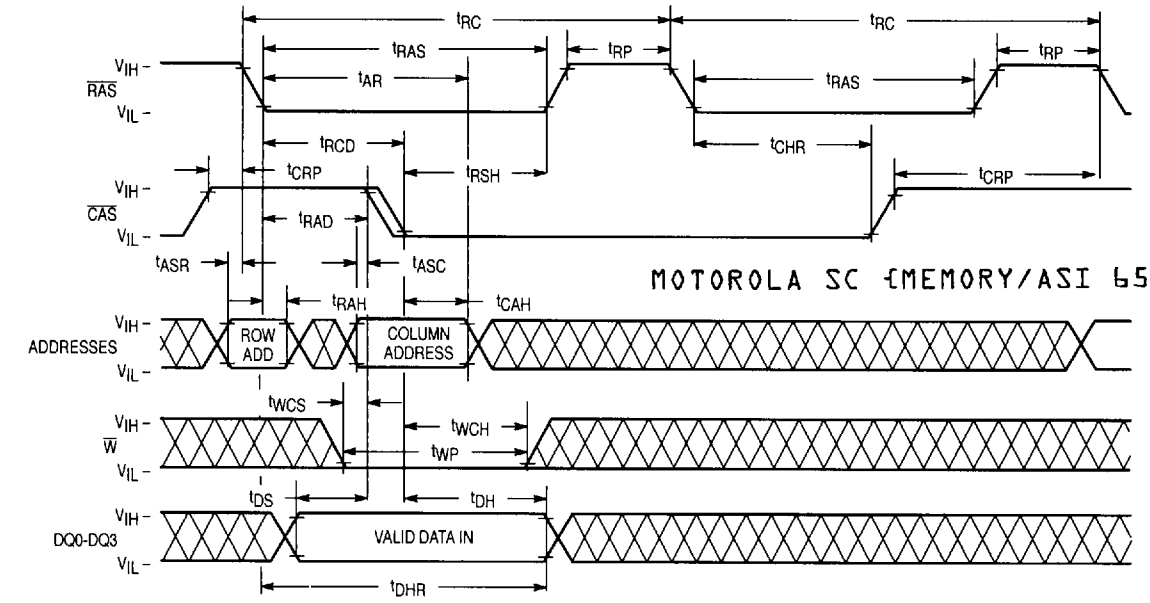
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
($\overline{W}$, $\overline{G}$, and A0-A8 are Don't Care)



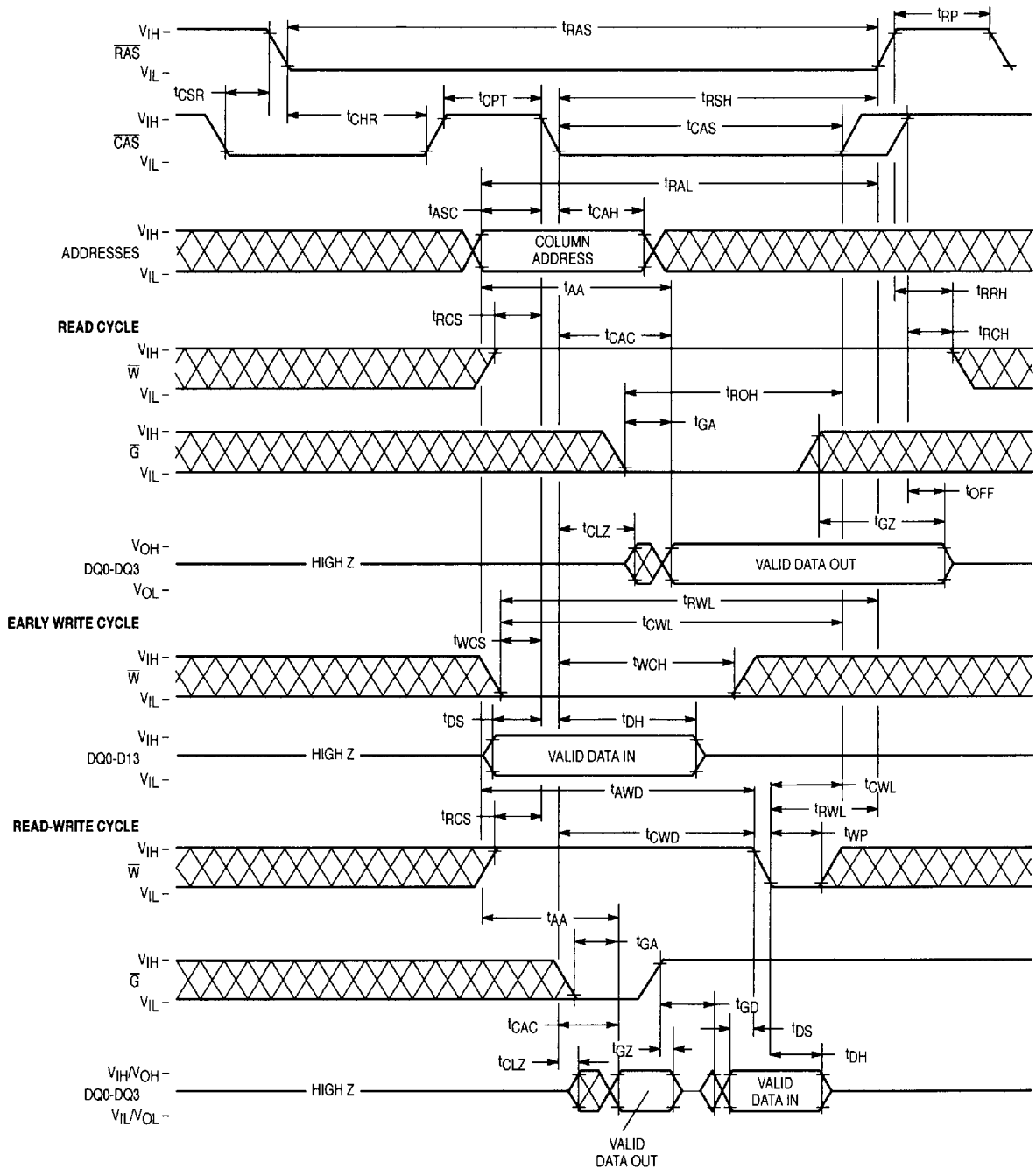
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (EARLY WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This has to be followed by a minimum of eight active cycles of the row address strobe ($\overline{RAS}$) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 8 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to assure proper operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 9-bit address fields. A total of eighteen address bits, nine rows and nine columns, will decode one of the 262,144 bit locations in the device. $\overline{RAS}$ active (V_{IL}) transition is followed by $\overline{CAS}$ active transition (after t_{RCD} minimum delay) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gate feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are two other variations in addressing the 256K x 4 RAM: **$\overline{RAS}$ only refresh cycle** and **$\overline{CAS}$ before $\overline{RAS}$ refresh cycle**. Both are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles; normal random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both $\overline{CAS}$ and output enable ($\overline{G}$) control read access time: $\overline{CAS}$ must be active before or at t_{RCD} maximum and $\overline{G}$ must be active $t_{RAC} - t_{GA}$ (both minimum) after $\overline{RAS}$ active transition to guarantee valid data out (Q) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded and/or $\overline{G}$ active transition does not occur in time, read access time is determined by either the $\overline{CAS}$ or $\overline{G}$ clock active transition (t_{CAC} or t_{GA}).

The $\overline{RAS}$ and $\overline{CAS}$ clocks must remain active for a minimum time or t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CAS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{CAS}$ and $\overline{G}$ clocks are active. When either the $\overline{CAS}$ or $\overline{G}$ clock transitions to inactive, the output will switch to High Z, t_{OFF} or t_{GZ} after inactive transition.

WRITE CYCLE

The DRAM may be written with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in another section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{W}$, with respect to $\overline{CAS}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time tWCS before $\overline{CAS}$ active transition. Date in (D) is referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains High Z throughout an early write cycle because $\overline{W}$ active transition precedes or coincides with $\overline{CAS}$ active transition, keeping data out buffers disable, effectively disabling $\overline{G}$.

A late write cycle (referred to as $\overline{G}$ controlled write) occurs when $\overline{W}$ active transition is made after $\overline{CAS}$ active transition. $\overline{W}$ active transition could be delayed for almost 10 microseconds after $\overline{CAS}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + t_T$) $\leq t_{RAS}$, if timing minimums t_{RCD}, t_{RWL}, and t_T are maintained. D is referenced to $\overline{W}$ active transition in a late write cycle. Output buffers are enabled by $\overline{CAS}$ active transition but Q may be indeterminate — see note 15 of AC operating conditions table. Parameters t_{RWL} and t_{CWL} also apply to late write cycles.

READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{W}$ must remain high for t_{CWD} minimum after the $\overline{CAS}$ active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 512 column locations on a selected row of the 256K x 4 dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first

page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{RAS}$ transitions to inactive, coincident with or following $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge degrades with time and temperature, thus each bit must be periodically refreshed (recharged) to maintain the correct bit state. Bits in the 514256A require refresh every 8 milliseconds.

Refresh is accomplished by cycling through the 512 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the 514256A. Burst refresh, a refresh of all 512 rows consecutively, must be performed every 8 milliseconds.

A normal read, write, or read-write operation to the RAM will refresh all the bits (2048) associated with the particular row decoded. Three other methods of refresh, **$\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh,** and **Hidden refresh** are available on this device for greater system flexibility.

$\overline{RAS}$-ONLY REFRESH

$\overline{RAS}$-only refresh consists of $\overline{RAS}$ transition to active, latching the row address to be refreshed, while $\overline{CAS}$ remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

$\overline{CAS}$ before $\overline{RAS}$ refresh is enabled by bringing $\overline{CAS}$ active before $\overline{RAS}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows cycles to occur while maintaining valid data at the output pin. Holding $\overline{CAS}$ active at the end of a read or write cycle, while $\overline{RAS}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{CAS}$ before $\overline{RAS}$ refresh from a cycle in progress (see Figure 1).

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 512 cycles, as indicated by the check data written in each row. See **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ initialization cycles. Test procedure:

1. Write "0"s into all memory cells with normal write mode.
2. Select a column address, read "0" out and write "1" into the cell by performing the **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read-write cycle**. Repeat this operation 512 times.
3. Read the "1"s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read "1" out and write "0" into cell by performing the **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read-write cycle**. Repeat this operation 512 times.
5. Read "0"s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

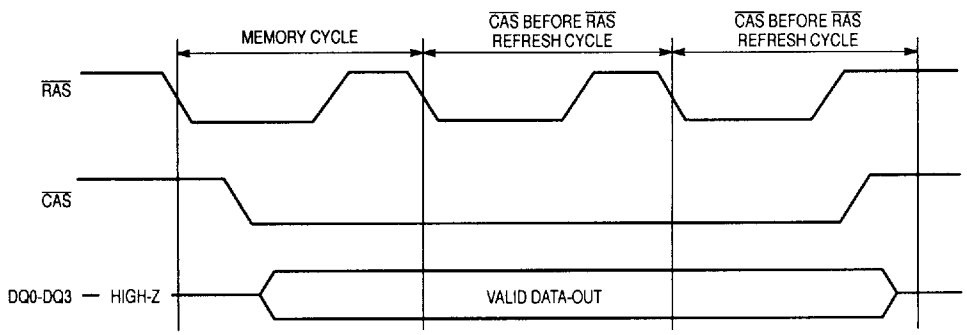


Figure 1. Hidden Refresh Cycle