Preliminary data **SIP 9**

The integrated circuit TDA 4600-3 is designed for driving, controlling, and protecting the switching transistor in self-oscillating flyback converter power supplies. In addition to its application in TV receivers and video tape recorders, this IC can also be used in hifi devices and active loud speakers due to its wide control range and high voltage stability.

- Direct control of the switching transistor
- Low start-up current
- Reversing linear overload characteristic
- Base current drive proportional to collector current

Description of function

This IC is designed for driving a bipolar power transistor and for performing all necessary control and protective functions in self-oscillating flyback converter power supplies. Owing to the IC's outstanding voltage stability, which is maintained even at major load fluctuations, the IC is suited for consumer as well as for industrial applications. The rectified line voltage is applied to the series connection of the power transistor and the primary winding of the flyback transformer. During the on-phase of the transistor, energy is stored in the primary winding and released to the consumer via the secondary winding.

The IC controls the power transistor in such a way that the secondary voltage is kept at a constant value independently of changes in the line voltage or load. The control information required is derived from the rectified line voltage during the on-phase as well as from a secondary winding during the off-phase.

Load differences are compensated by altering the frequency, line voltage fluctuations are additionally counteracted by changing the pulse duty factor. This results in the following load-dependent modes of the SMPS:

– Open-loop or small load:	Secondary voltage slightly above the desired value
– Control:	Load-independent secondary voltage
– Overload:	In case of a secondary overload or short circuit, the secondary voltage is decreased at the point of return as a function of the load current, following a reversing characteristic.

Description of use

A flyback converter designed for color TV sets, applicable between 30 W and 120 W and for line voltages ranging from 160 V to 270 V, is described on one of the following pages. On the subsequent pages the major pulses and diagrams can be found. The line voltage is rectified by bridge rectifier Gr1 and smoothed by C_3. During start-up the IC current is supplied via the combination Gr2+R_{11} while, in the post-transient condition, it is additionally supplied via winding 13/11 and rectifier Gr3. The size of filter capacitor C_9 determines the turn-on behavior.

Switching transistor T1 is a BU 208. Parallel capacitance C_{11} and primary winding 1/7 form a resonant circuit, thus limiting the frequency and amplitude of collector-emitter voltage overshoots upon turn-off of T1. R_{12}, Gr4, C_{10}, R_{15} and Dr2 are elements to improve the switching behavior of T1.

The inductance of the primary winding determines the current increase in T1. This sawtooth-shaped current rise is simulated at network R_5C_8 and applied to pin 4 of the IC. Depending of the dimensions of the primary inductance, timing element R_5C_8 is to be adapted to the current rise angle in T1. Thus, during the on-phase, the IC receives control information at pin 4 in the form of the simulated energy content of the primary winding as a function of the line voltage versus time.

Fluctuations at pin 3 are recognized by control winding 9/15. This measure requires fixed coupling to secondary winding 2/16. The control winding is also used for feedback and permits self-oscillating conditions in parallel circuit C_{11}/primary inductance if power transistor T1 is blocked. In this way the maximum open-loop frequency is determined.

The control voltage required at pin 3 is rectified by diode Gr5 and smoothed by capacitor C_6. Furthermore, resistor R_8 and C_6 form a timing element. Due to these circumstances, fast changes in the control voltage are filtered out, i.e. the controlling element does not respond until several periods have occured. The secondary voltage can be set by means of the voltage divider formed of resistors R_7, R_6, R_3 and R_2. Reason: in the IC the control voltage at pin 3 is compared with a stable, internal reference voltage.

According to the result of this comparison, frequency and pulse duty factor are corrected until the secondary voltage selected by R_7 has established itself.

In the case of overload or short circuit on the secondary side, only a small voltage portion is passed to control winding 9/15; the reference voltage at pin 1 becomes directly active at control input pin 3 and activates an overload amplifier (point of return), which drives power transistor T1 down to a smaller pulse duty factor. The line power output is reduced to 6 VA.

For all operating ranges of the SMPS, the zero passages of the voltage at the control winding contain information on pulse duty factor and switching frequency of switching transistor T1, or on the open-loop frequency. Conditioning of the corresponding signal at pin 2 is performed by series resistor R_4, and by integrated limiter diodes. Timing network R_8C_4 suppresses HF spikes at pin 2.

Before the line voltage drops below its minimum value, the SMPS must be switched off in order to obtain defined on/off conditions. Winding 11/13 is configured in such a way that the voltage at pin 9 changes linearly with the rectified line voltage. The IC goes into on-state if $V_9 \geq 12.3$ V, and into off-state if $V_9 \leq 5.7$ V. The drive of the power transistor will be blocked as soon as $V_9 \leq 6.7$ V.

Pin 5 is connected to pin 9 via resistor R_9, since the IC's output is not enabled until voltages $V_5 \geq 2.7$ V prevail.

On the secondary side start-up voltages from V_{1sec} to V_{4sec} are available. If switch S1 is put into open position, standby is set automatically, with a secondary effective power of approx. 3 W being tapped from winding 12/16. Resistors R_{13} and R_{14} form a basic load of voltages V_{1sec} and V_{2sec}. They contribute to maintaining standby conditions, i.e. V_{sec} rise $\leq$ 20%. Capacitors C_{12} through C_{15} prevent spikes caused by reversing rectifiers Gr6 and Gr9. The secondary voltages are smoothed by the charging electrolytic capacitors C_{16} through C_{19}. After the line voltage has been applied at time t_0, the following voltages start to increase:

- V_9 according to the half-cycle charge via R_{11}.
- V_4 to $V_{4\,max}$ (typ. 6.2 V)
- V_5 to the value determined by R_9

In this case the current consumption of the IC is smaller than 3.2 mA. If V_9 reaches the threshold 12.3 V, the IC will switch on the reference voltage of pin 1. The current consumption rises to typically 80 mA. The primary current voltage transformer adjusts V_4 down to $V_{REF/2}$ and the start pulse generator produces the start pulse. Feedback to pin 2 starts a subsequent pulse and so forth.

The width of all pulses, including the start pulse, is controlled by the control voltage at pin 3. During turn-on the control voltage corresponds to standby conditions, i.e. $V_3 = V_{REF/2} + 50$ mV. The IC begins with narrow pulses, which become wider depending on the feedback control voltage. Instantly, the IC operates in the control mode. The control loop is in a post-transient state. If, during start-up, voltage V_9 drops below the turn-off threshold $V_9 \leq 7.8$ V, the start-up phase will be terminated (pin 8 is switched to Low). Since the IC remains in the on-state, V_9 drops further to $V_9 \leq 5.7$ V. The IC switches to the off-state, V_9 is now able to rise again and a new start-up phase may begin. After the IC has been started, it will operate in the control mode. The voltage at pin 3 is typically $V_{REF/2} + 0.2$ V.

If the output is loaded, the control amplifier allows wider charge pulses to occur (V_8 = H). The peak value of the voltage at pin 4 rises to $V_4 = V_{REF}$. Upon an increase in the secondary load the overload amplifier begins adjusting the pulse width down. Since altering of the pulse width is reversed, this is referred to as the reverse point of the SMPS or point of return. In case of a short circuit on the secondary side, the overload amplifier will adjust the pulse width to typically 1.6 µs and reduces the pulse duty factor to <1:100. The SMPS decreases the line power consumption to typically 6 VA. A small pulse duty factor entails a drop in supply voltage V_9 below the threshold $V_9 \leq 6.7$ V causing a drive interrupt of the switching transistor and a continued drop of supply voltage V_9. If supply voltage $V_9 \leq 5.7$ V, the IC is turned off and enters into a new start-up phase.

This intermittent periodic duty operation is continued until the short circuit on the secondary side has been eliminated.

If the secondary side is unloaded (standby), the control pulse width becomes narrower. The frequency rises. During open-loop operation the approximate natural frequency of the system (75 kHz) is obtained; pulse duty factor 1:11. The rise of the secondary voltages is approx. 20%. If resistors R_{13}/R_{14} were absent, the IC would have to perform adjustment beyond the natural frequency of the system, with the zero passage identification only recognizing every 2nd, 3rd or 4th zero passage as a pulse start, i.e. the frequency would divide down to the 2nd, 3rd or 4th subharmonic. The pulse duty factor is thus diminished to 1:22, 1:33, or 1:44, respectively. The pulse width remains constant at approx. 1.2 µsec. A certain small pulse duty factor causes supply voltage V_9 to drop below the threshold voltage $V_9 \leq 6.7$ V. Then, the interrogation intermittent periodic duty operation begins as already described for the short circuit case. Constant open-loop operation will not continue until resistors R_{13}/R_{14} have been loaded.

Circuit description

Pin 1: Reference voltage output, overload-protected.
$I_{1max} = 5$ mA. All modules, excluding the IC's output stage, are supplied by the internal reference voltage.

Pin 2: The zero passage identification driving the control logic identifies the discharged status of the transformer at the zero passage of voltage V_2 from negative to positive values and enables the logic for pulse start, which is driven by trigger start.

Pin 3: The control voltage supplied to this pin is compared with two stable reference potentials in the control amplifier, in overload identification and during standby. The outputs of these stages operate onto the trigger hold, thus terminating the pulse.

Pin 4: A voltage proportional to the collector current of the switching transistor is generated on the basis of the external RC combination in conjunction with the collector current simulation block. This voltage introduces the beginning of a pulse at a stable voltage via trigger start and determines at a second stable voltage (reverse point) the absolute maximum pulse (with respect to time length) in trigger hold. At the same time the rise angle of the voltage proportional to the collector current of the switching transistor is impressed onto the base current amplifier, and, in accordance with the smallest current amplification B of the switching transistor to be expected, the base of the switching transistor is driven via pin 8.

Pin 5: If a voltage ≥ 2.7 V is applied, the control logic is enabled via the trigger. Pins 7/8 are driven by the coupling capacitor charge circuit and the base current. In case a voltage ≤ 1.8 V prevails, base current switch-off pin 7 is clamped at a voltage $V_7 \leq 1.3$ V; driving of the switching transistor is impossible. The IC will not be enabled again until the voltage at pin 9 has dropped below 5.7 V, the IC has been turned off and the SMPS has entered a new start-up phase.

Pin 6: GND

Pin 7/8: Via the voltage controller and the coupling capacitor charge circuit, the output stage of the IC is dc-adjusted to the switching transistor. The switching transistor is driven via a base current amplifier and pin 8, while it is blocked via the basic current switch-off and pin 7.

Pin 9: Current supply of the IC.

Maximum ratings

		min	max	
Supply voltage	V_9	0	20	V
Voltages				
Reference output	V_1	0	6	V
Identification input	V_2	−0.6	0.6	V
Control amplifier	V_3	0	3	V
Collector current simulation	V_4	0	8	V
Blocking input	V_5	0	8	V
Base current cut-off point	V_7	0	V_9	V
Base current amplifier output	V_8	0	V_9	V
Currents				
Feedback zero passage	$I_{i\,2}$	−5	5	mA
Control amplifier	$I_{i\,3}$	−3	3	mA
Collector current simulation	$I_{i\,4}$	0	5	mA
Base current cut-off point	$I_{q\,7}$	0	1.5	A
Base current amplifier output	$I_{q\,8}$	−1.5	0	A
Junction temperature	T_j		125	°C
Storage temperature range	T_{stg}	−40	125	°C
Thermal resistances				
junction-air	$R_{th\,JA}$		70	K/W
junction-case	$R_{th\,JC}$		15	K/W
Operating range				
Supply voltage	V_9	7.8	18	V
Case temperature	T_c	0	85	°C

Characteristics

$T_A = 25\,°C$; according to measurement circuit 1 and diagram

		min	typ	max	
Start operation					
Current consumption (V_1 not yet switched on)					
$V_9 = 2$ V	I_9			0.5	mA
$V_9 = 5$ V	I_9		1.5	2.0	mA
$V_9 = 10$ V	I_9		2.4	3.2	mA
Switching point for V_1	V_9	11.0	11.8	12.3	V
Normal operation					
$V_9 = 10$ V; $V_{cont} = -10$ V; $V_{clock} = \pm 0.5$ V; $f = 20$ kHz; pulse duty factor 1 : 2 after switch-on					
Current consumption					
$V_{cont} = -10$ V	I_9	110	135	160	mA
$V_{cont} = 0$ V	I_9	50	75	110	mA
Reference voltage					
$I_1 < 0.1$ mA	V_1	4.0	4.2	4.5	V
$I_1 = 5$ mA	V_1	4.0	4.2	4.4	V
Temperature coefficient of reference voltage	TC_1		10^{-3}		1/K
Control voltage $V_{cont} = 0$ V	V_3	2.3	2.6	2.9	V
Collector current simulation voltage					
$V_{cont} = 0$ V	V_4*)	1.8	2.2	2.5	V
$V_{cont} = 0$ V/−10 V	ΔV_4*)	0.3	0.4	0.5	V
Blocking input voltage	V_5	6.0	7.0	8.0	V
Output voltages					
$V_{cont} = 0$ V	V_{q7}*)	2.7	3.3	4.0	V
$V_{cont} = 0$ V	V_{q8}*)	2.7	3.4	4.0	V
$V_{cont} = 0$ V/−10 V	ΔV_{q8}*)	1.6	2.0	2.4	V
Feedback voltage	V_2		0.2		V
Protective operation					
$V_9 = 10$ V; $V_{cont} = -10$ V; $V_{clock} = \pm 0.5$ V; $f = 20$ kHz; pulse duty factor 1 : 2					
Current consumption					
$V_5 < 1.8$ V	I_9	14	22	28	mA
Turn-off voltage					
$V_5 < 1.8$ V	V_{q7}	1.3	1.5	1.8	V
Turn-off voltage					
$V_5 < 1.8$ V	V_4	1.8	2.1	2.5	V
External blocking input					
Enable voltage					
$V_{cont} = 0$ V	V_5		2.4	2.7	V
Blocking voltage					
$V_{cont} = 0$ V	V_5	1.8	2.2		V
Supply voltage blocked for V_8					
$V_{cont} = 0$ V	V_9	6.7	7.4	7.8	V
V_1 turned off (if V_9 is further decreased)	ΔV_9	0.3	0.6	1.0	V

*) DC component only

Characteristics

$T_A = 25\,°C$; according to measurement circuit 2

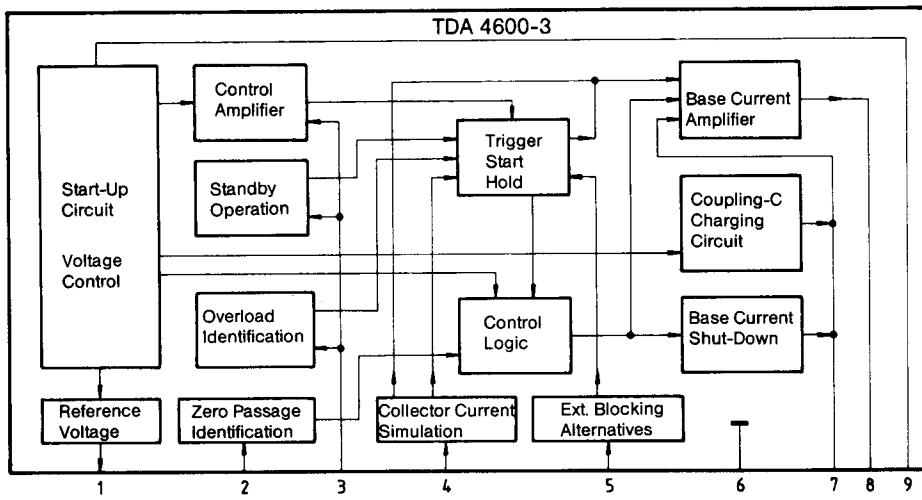
		Test conditions	min	typ	max	
Turn-on time (secondary voltage)	t_{on}			350	450	ms
Voltage change (S3 = closed)	$\Delta V_{2\,sec}$	$\Delta N_3 = 20$ W		100	500	mV
Sound output power (S2 = closed)	$\Delta V_{2\,sec}$	$\Delta N_2 = 15$ W		500	1000	mV
Standby operation (S1 = open)	$\Delta V_{2\,sec}$	Sec. useful load = 3W		20	30	V
	f		70	75		kHz
	$N_{primary}$			10	12	VA

Pin description

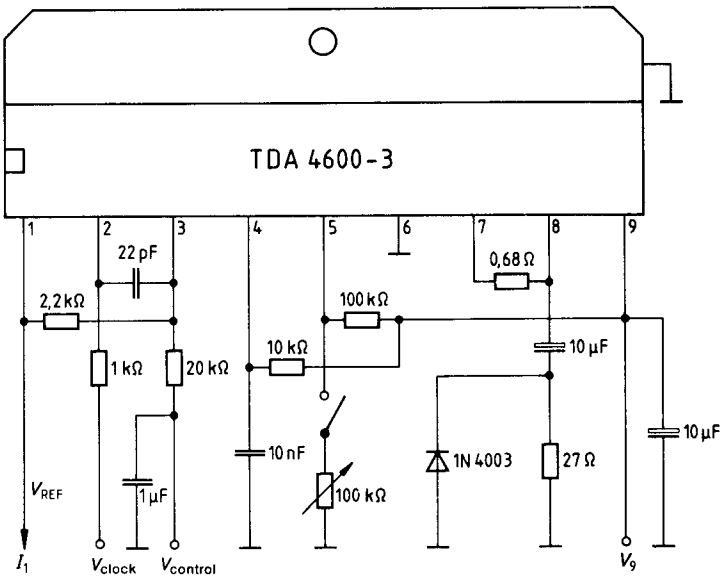
Pin	Designation	Function
1	V_{REF} output	The IC adjusts the secondary voltage of the SMPS to a multiple of the reference voltage V_{REF}.
2	Zero passage identification	Input for oscillator feedback. After build-up, each zero passage of the feedback voltage (rising edge) triggers an output pulse at pin 8. The trigger threshold is typically −30 mV.
3	Control amplifier and overload amplifier input	Information input for secondary voltage. The output pulse width at pin 8 is adapted to the load on the secondary side by comparing the control voltage gained from the control winding of the transformer to the reference voltage (normal, overload, short-circuit, open-loop operation).
4	Collector current simulation	Information input for primary voltage. The rise of the primary current in the primary winding is simulated as voltage increase at pin 4 by means of an external RC element. If a value derived from the control voltage at pin 3 is reached, the compensating pulse at pin 8 is terminated. The RC element serves for setting the maximum power at the point of return. In this point, the amplitude of the sawtooth-shaped voltage at pin 4 rises to the value of V_{REF}.

Pin	Designation	Function
5	Protective input	For response of the oscillator a voltage of at least 2.7 V must be applied at pin 5. In case of disturbance, an additional secondary pulse at pin 8 is prevented if the voltage drops below 1.8 V, which is the protective threshold value.
6	Ground	The capacitor at pin 4 is to be directly connected to pin 6. The primary current of the transformer is not to be routed through this connection.
7	DC voltage output for charging coupling capacitor	Current sink after an output pulse and charging source for the coupling capacitor before an output pulse.
8	Pulse output drive of switching transistor	Current source for output pulse. The output current is adjusted according to the voltage rise at pin 4 with the aid of the resistor between pins 7 and 8. Thus, oversaturation of the external power transistor is prevented.
9	Current supply	For start-up of the SMPS the following conditions must be met: – The reference voltage at pin 1 is turned off – Subsequently, at pin 9, a rise of the supply voltage up to a value exceeding 12.3 V – At pin 5 the voltage is above 2.7 V. During operation the supply voltage is monitored for undervoltage. For values below 6.7 V the output pulses at pin 8 are blocked and for values below 5.7 V the reference voltage is turned off as an additional measure. These are the preconditions for a new oscillator start-up.

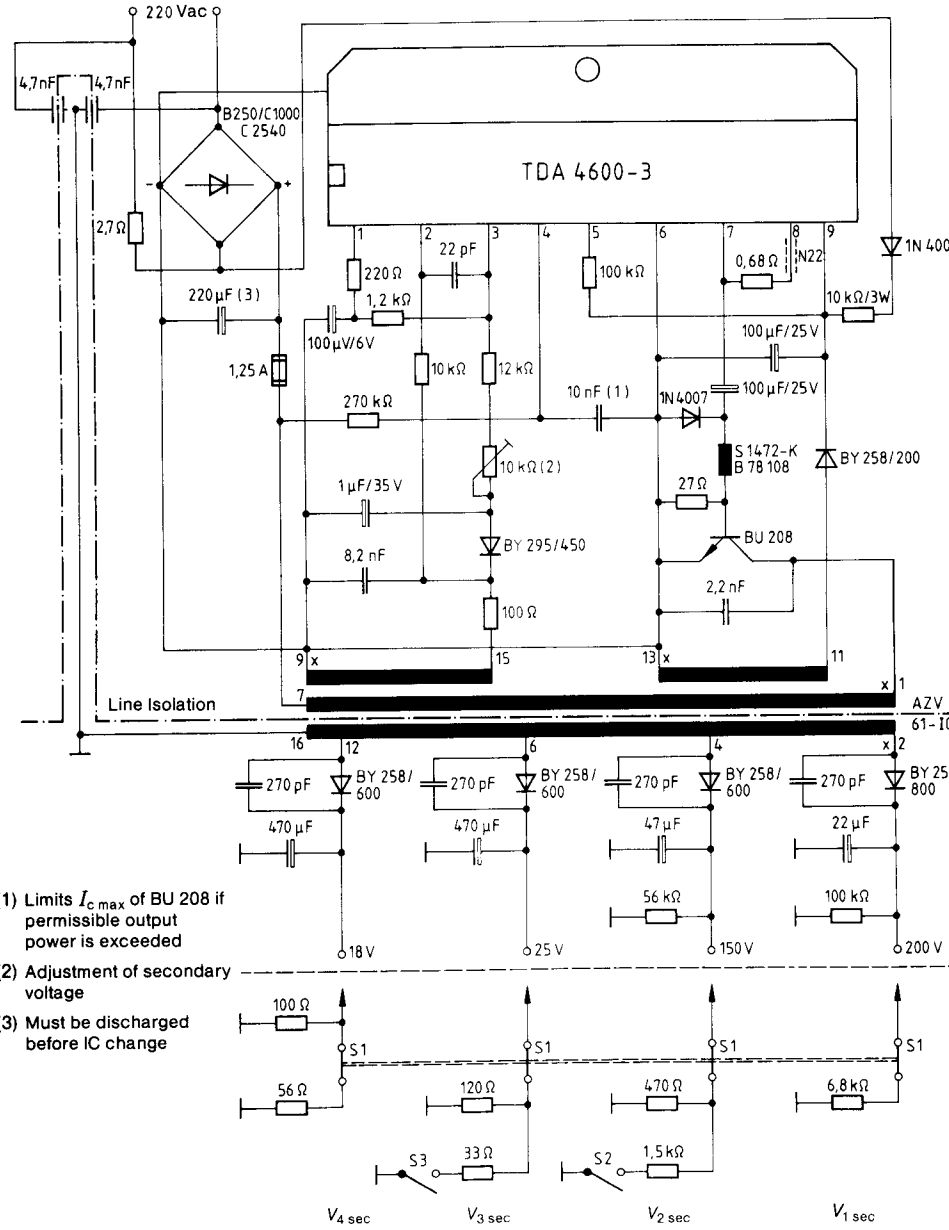
Block diagram



Measurement circuit 1



Measurement circuit 2

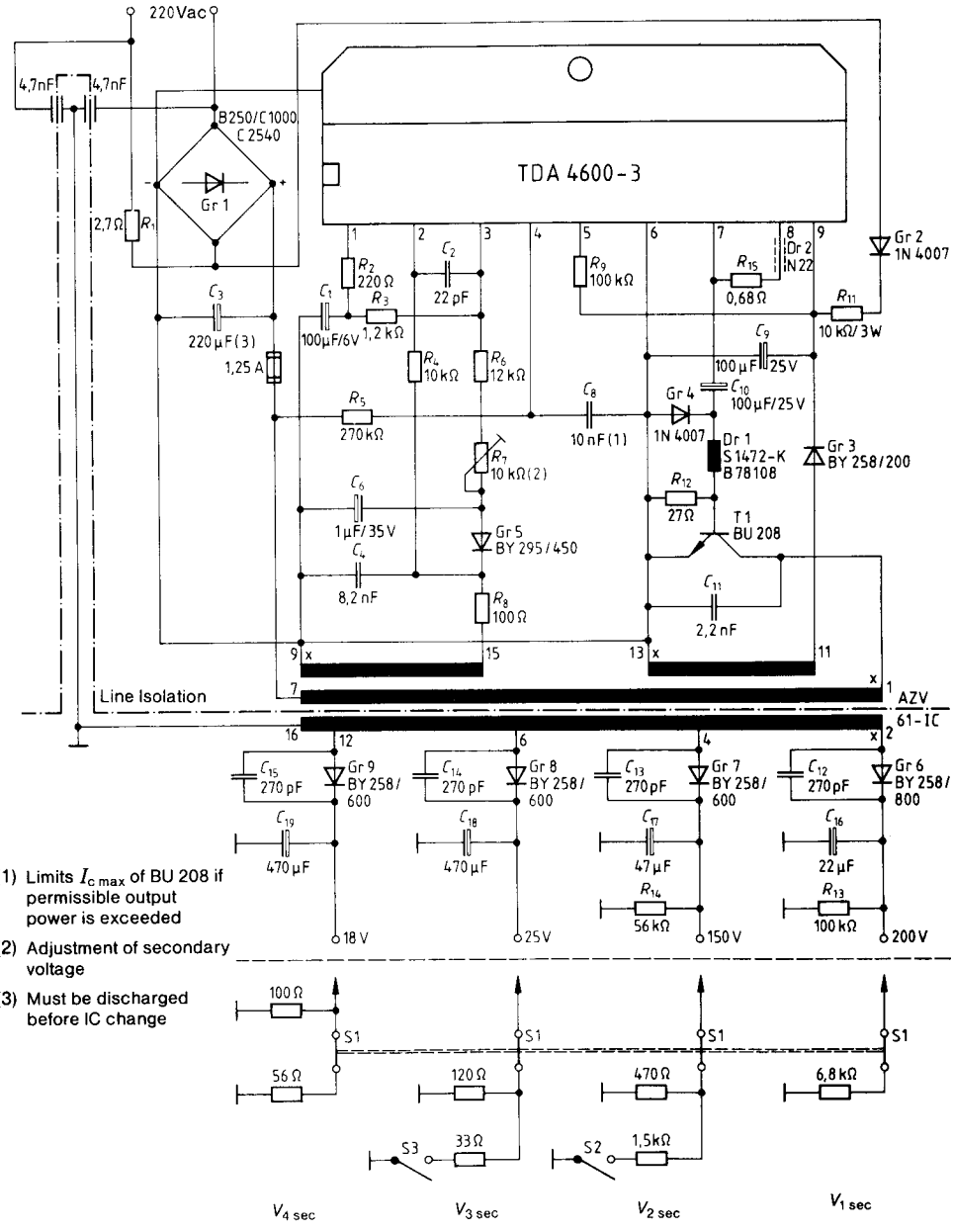


(1) Limits $I_{c\,max}$ of BU 208 if permissible output power is exceeded

(2) Adjustment of secondary voltage

(3) Must be discharged before IC change

Application circuit



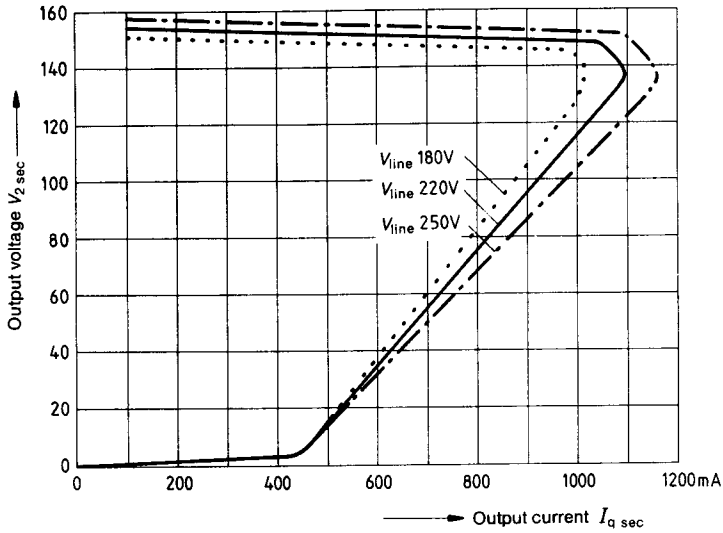
(1) Limits $I_{c\,max}$ of BU 208 if permissible output power is exceeded

(2) Adjustment of secondary voltage

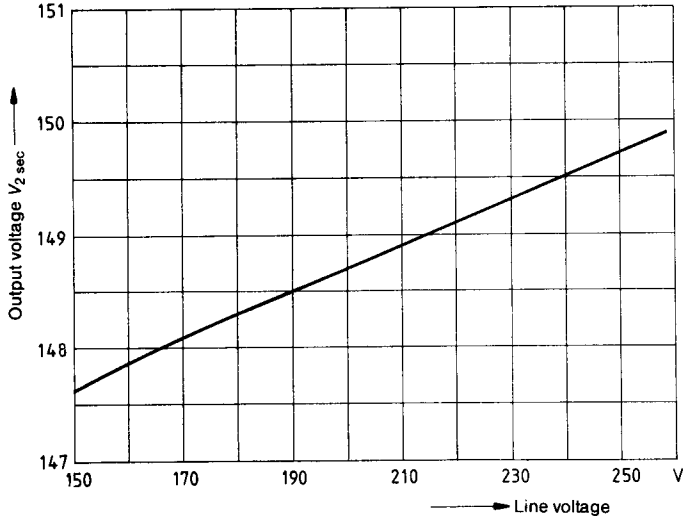
(3) Must be discharged before IC change

Supplements to test and measurement circuit 2

Load characteristic
Output voltage versus output current



Output voltage versus line voltage



Measurement diagram for overload operation, measurement circuit 1