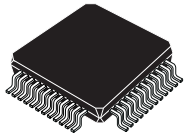
STLC1512

NorthenLite™ G.lite Loop Driver

PRODUCT PREVIEW

- Low power architecture -- Class AB, current drive, output stage through a centre tapped transformer to facilitate power supply switching between 5.0V and a lower voltage. (3.3V in the reference design) This gives a reduction in power consumption.
- 480mW power consumption with a typical G.lite signal.
- 600mA current driving capability
- Positive +5.0V and one lower supply. (3.3V in the reference design)
- Switching power supplies to save power
- Thermal overload shutdown
- Four programmable receive gains
- Opamp for a low pass filter in the receive path
- Undedicated opamp with separate power down control (used as a transmit path filter in the reference design)
- Separate power down control for Tx and Rx path
- 48-pin TQFP (7x7x1.4mm) package

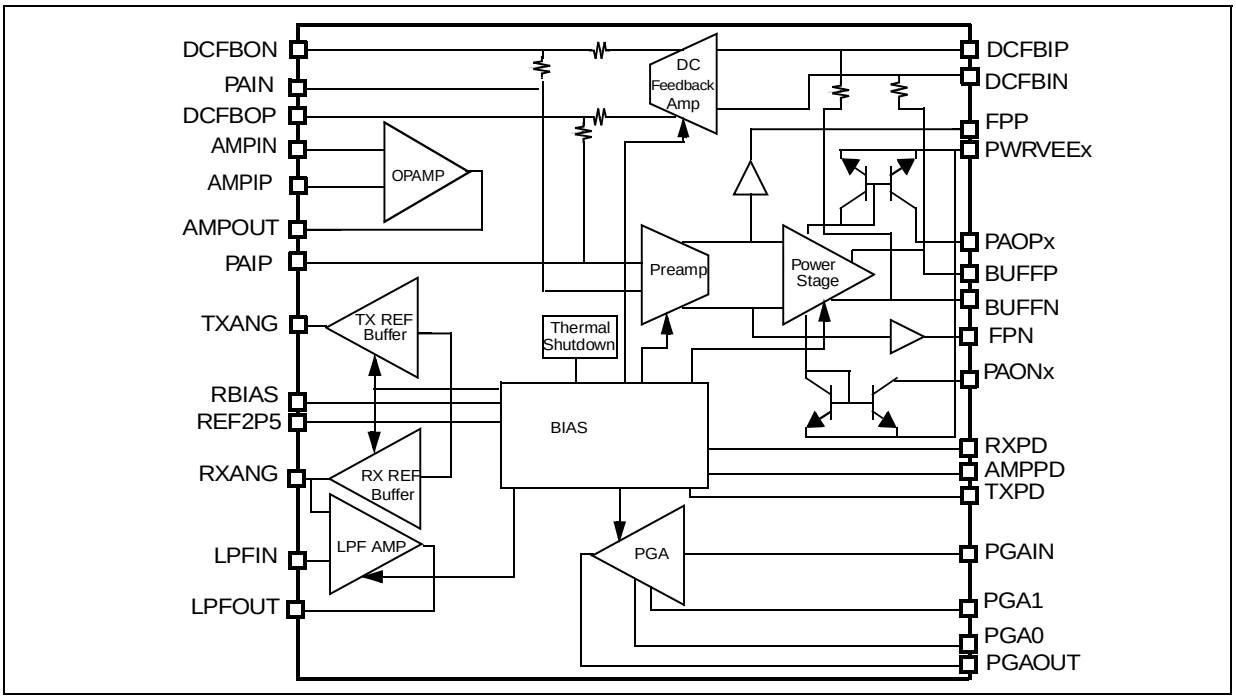


TQFP48 (7x7x1.40)
ORDERING NUMBER: STLC1512

1.0 GENERAL DESCRIPTION

The STLC1512 G.lite line driver chip contains the line driver as well as part of the receive path required in a central office G.lite modem. It provides an interface between the AFE chip (STLC1511) and the telephone line. The line driver chip has been designed with low power consumption, high signal to noise plus distortion ratio and high current driving capability.

Figure 1. Block Diagram



1.0 GENERAL DESCRIPTION

The line driver transmit path contains a preamplifier followed by a power output stage. The power stage has current outputs that directly drive the primary side of a center tapped transformer.

The receive path contains a programmable gain amplifier followed by an opamp which is used with off chip passive components in an active low pass filter. The Programmable Grain Amplifier (PGA) has four steps optimized for the recommended G.lite CO line interface.

There is also an undedicated opamp which can be used for active filtering in either the transmit or receive paths

2.0 PACKAGING AND PIN INFORMATION

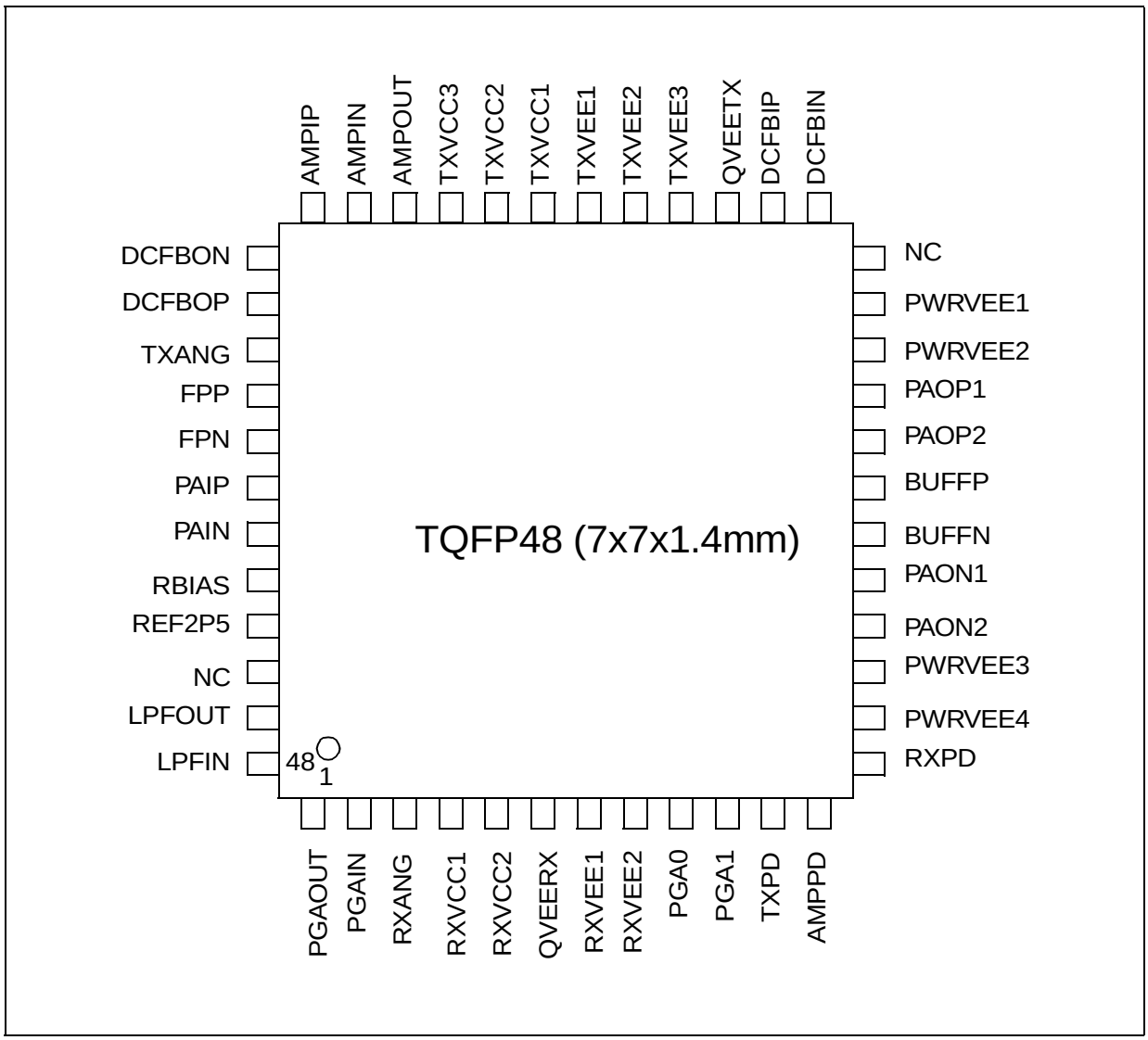
2.1 Package Technology

STLC1512 will be packaged in a TQFP 48 package, according to JEDEC Specification reference MS-026-BBC.

2.2 STLC1512 Pin Allocation

The pin out for the STLC1512 is depicted in the following Figure 2.

Figure 2. STLC1512 pinout



2.3 Pin Description

The pin description for the STLC1512 is given in the following Table 1.

Table 1. Pin Description

Pin #	Pin Name	Pin Type	Pin Description[1]
1	PGAOUT	AO	Rx PGA output (programmable gain amplifier)
2	PGAIN	AI	Rx PGA input
3	RXANG	AO	2.5V Rx buffered reference
4	RXVCC1	VCC	+5.0V supply for Rx path circuitry
5	RXVCC2	VCC	+5.0V supply for Rx path circuitry
6	QVEERX	VEE	Quiet ground for the Rx circuitry
7	RXVEE1	VEE	Ground for Rx path circuitry
8	RXVEE2	VEE	Ground for Rx path circuitry
9	PGA0	DI	PGA gain setting control bit 0
10	PGA1	DI	PGA gain setting control bit 1
11	TXPD	DI	Tx path power down control (Active low)
12	AMPPD[2]	DI	Undedicated opamp power down control (Active low)
13	RXPD	DI	Rx path power down control (Active low)
14	PWRVEE4	VEE	Power stage ground.
15	PWRVEE3	VEE	Power stage ground.
16	PAON2	AO	Tx Power Amplifier Negative output
17	PAON1	AO	Tx Power Amplifier Negative output
18	BUFFN	AO	Current generator buffer negative output
19	BUFFP	AO	Current generator buffer positive output
20	PAOP2	AO	Tx Power Amplifier Positive output
21	PAOP1	AO	Tx Power Amplifier Positive output
22	PWRVEE2	VEE	Power stage ground.
23	PWRVEE1	VEE	Power stage ground.
24	NC		Not connected
25	DCFBIN	AI	Power amp DC feedback amplifier negative input
26	DCFBIP	AI	Power amp DC feedback amplifier positive input
27	QVEETX	VEE	Quiet ground for Tx circuitry
28	TXVEE3	VEE	Ground for Tx path circuitry
29	TXVEE2	VEE	Ground for Tx path circuitry
30	TXVEE1	VEE	Ground for Tx path circuitry
31	TXVCC1	VCC	+5.0V supply for power amp output stage

Table 1. Pin Description

32	TXVCC2	VCC	+5.0V supply for power amp output stage
33	TXVCC3	VCC	+5.0V supply for Tx path circuitry and bias blocks
34	AMPOUT	AO	Undedicated opamp output
35	AMPIN	AI	Undedicated opamp negative input
36	AMPIP	AI	Undedicated opamp positive input
37	DCFBON	AO	Power amp DC feedback amplifier negative output
38	DCFBOP	AO	Power amp DC feedback amplifier positive output
39	TXANG	AO	2.5V Tx buffered reference
40	FPP	AO	Fast path positive output
41	FPN	AO	Fast path negative output
42	PAIP	AI	Tx Power amplifier positive input
43	PAIN	AI	Tx Power amplifier negative input
44	RBIAS	AO	Reference resistor generating bias current
45	REF2P5	AI	Externally supplied 2.5V reference
46	NC		Not connected
47	LPFOUT	AO	LPF (low pass filter) Op Amp output
48	LPFIN	AI	LPF (low pass filter) Op Amp negative input

<1>The values of the components that are connected to the pins are shown in Figure 11.
<2>If the undedicated opamp is used in the transmit path, AMPPD can be connected to TXPD on the board. If the undedicated opamp is used in the receive path, AMPPD can be connected to RXPD on the board. This opamp is powered off of TXVCC3.

3.0 FUNCTIONAL DESCRIPTION

The STLC1512 consists of the following functional blocks:

- Transmit Signal Path
- Receive Signal Path
- Thermal Protection

The transmit signal that comes from the AFE is filtered before it reaches the line driver. STLC1512 contains an opamp that can be utilized as part of this filter. The AMPPD pin allows this op amp to be powered down independently. The line driver consists of a preamp followed by a current drive power stage. The preamplifier provides large open loop gain while the power stage provides open collector current drive to allow for single supply switching. The center tap of the primary side of the transformer is connected to a supply that can be switched between 5.0V and a lower supply to realize power savings on a DMT signal. The reference design sets this supply at 3.3V. The line driver can be powered down by a low at the TXPD pin.

The receive path consists of a Programmable Gain Amplifier (PGA) and an active low pass filter. The PGA is programmable in four steps. The active low pass filter is composed of an on chip op amp and external passive components. The receive signal passes through the PGA, is low pass filtered and then driven off chip to the AFE chip. Both the PGA and the opamp can be powered down by RXPD signal.

A thermal protection circuit has also been implemented on the chip to prevent the chip from overheating under fault conditions.

4.0 SPECIFICATIONS

4.1 Chip Specifications

The cross-talk specifications are based on the assumption that cross-talk should not degrade the SNDR of the receive signal. If there is receive cross-talk into the transmit path, this signal will come back through the hybrid balance and cause noise in the receive path. If the signal is undistorted it will cause a small gain and phase error which will not affect performance. If it is distorted it will cause an increased

noise floor which will degrade the SNDR of the receive signal.

The same is true of the transmit signal. If the signal is undistorted it will show up out of band in the receive path and will not degrade SNDR. However, if the transmit signal is distorted by the cross-talk mechanism it will show up in the receive band and could reduce the SNDR.

The cross-talk numbers are specified from output to output under maximum gain conditions.

Table 2. Chip Performance Specifications

Description	min	nom	max	Units	Comments
Rx Cross-Talk into Tx Undistorted			-55	dB	Measured from the active low pass filter output in the receive path to tip and ring.
Rx Cross-Talk into Tx Distorted			-73	dB	Measured from the active low pass filter output in the receive path to tip and ring.
Tx Cross-talk into Rx Undistorted			-50	dB	Measured from tip and ring to the active low pass filter output with the maximum gain setting in place.
Tx Cross-talk into Rx Distorted			-86	dB	Measured from tip and ring to the active low pass filter output with the maximum gain setting in place.

4.2 Power Amplifier Performance Specifications

The power amplifier must be specified with all of the external components in the application diagram. Without these components the amplifier will not function correctly. Specifications that are measured at the chip are specified as such in the comments.

Table 3 contains the conditions over which the specifications in Table 4 apply. The limits on the specifications in Table are valid over all of the ranges specified in Table 3. The nominal values of the specification occur at the nominal value of all of the conditions in Table 3 unless otherwise specified.

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Table 3. Power Amplifier Performance Limits

Description	min	nom	max	Units	Comments[1,2]
Gain	19.9	20.1	20.3	dB	
Ambient Temperature	-40	27	85	^{o}C	
Line Impedance	80	100	160	W	A nominal chip will have no problem driving 200 Ω or 50 Ω.
Supply voltage for TXVCC	4.75	5.0	5.25	V	

<1>Nominal specifications are for nominal bias and process
<2>Maximum and minimum specifications are for worst case process and bias conditions

Table 4. Power Amplifier Performance Specifications

Unless otherwise specified nom specs apply to the nom conditions in attribute and the max and min conditions are defined by the process and other spec limits that give these worst case corners.						
Description	min	nom	max	Goal	Units	Comments
Quiescent current at PAOP/ PAON[1]	10	15	18		mA	The spec is measured as the sum of the currents at POAP1+PAOP2 or PAON1+PAON2.
Total quiescent current at output stage[2]	20	30	36		mA	Measured at the center tap of the transformer.
Input bias current[3]			15		µA	Measured at pin PAIP/PAIN. This parameter cannot be measured very accurately.
Minimum Voltage at PAOP/ PAON [4] High Current Drive			0.85		Vpeak	Measured at pin PAOP1,2/ PAON1,2
Minimum Voltage at PAOP/ PAON[5] Low Current Drive			0.70		Vpeak	Measured at pin PAOP1,2/ PAON1,2
Common mode input voltage range[6]	1.6		VCC-0.5		V	Measured at pin PAIP/PAIN
Peak output sink current on pin PAOP and PAON[7]	600		1000		mA	This is the sum of the current from PAOP1 and PAOP2 or the sum of the currents from PAON1 and PAON2
Power supply rejection						See Figure 3.
Slew Rate[8]	35				V/µS	Measured across the 100 Ohm line impedance
Output referred noise voltage[9]		78	120		nV/÷√Hz	measured at f=120kHz Simulated to be good from 30kHz to 540kHz.
Signal to distortion ratio Two tone A[10] Im2 @ 200 kHz Im3 @ 100 kHz Two tone B<Superscript>10 Im3 @ 550 kHz Output DS Multi-tone[11] 28kHz < f < 121kHz 151kHz < f < 541kHz	 78 78 59 78 59	 85 66		 86 86 59 86 59	 dB dB dB dB dB	Measured at the line impedance. The 4 to 1 transformer must have total harmonic distortion better than 50dB over 30kHz < f < 550kHz. The multi-tone spec is the important spec. The two tone specs exist because the test equipment may not be able to create a good enough multi-tone input signal.

Table 4. Power Amplifier Performance Specifications

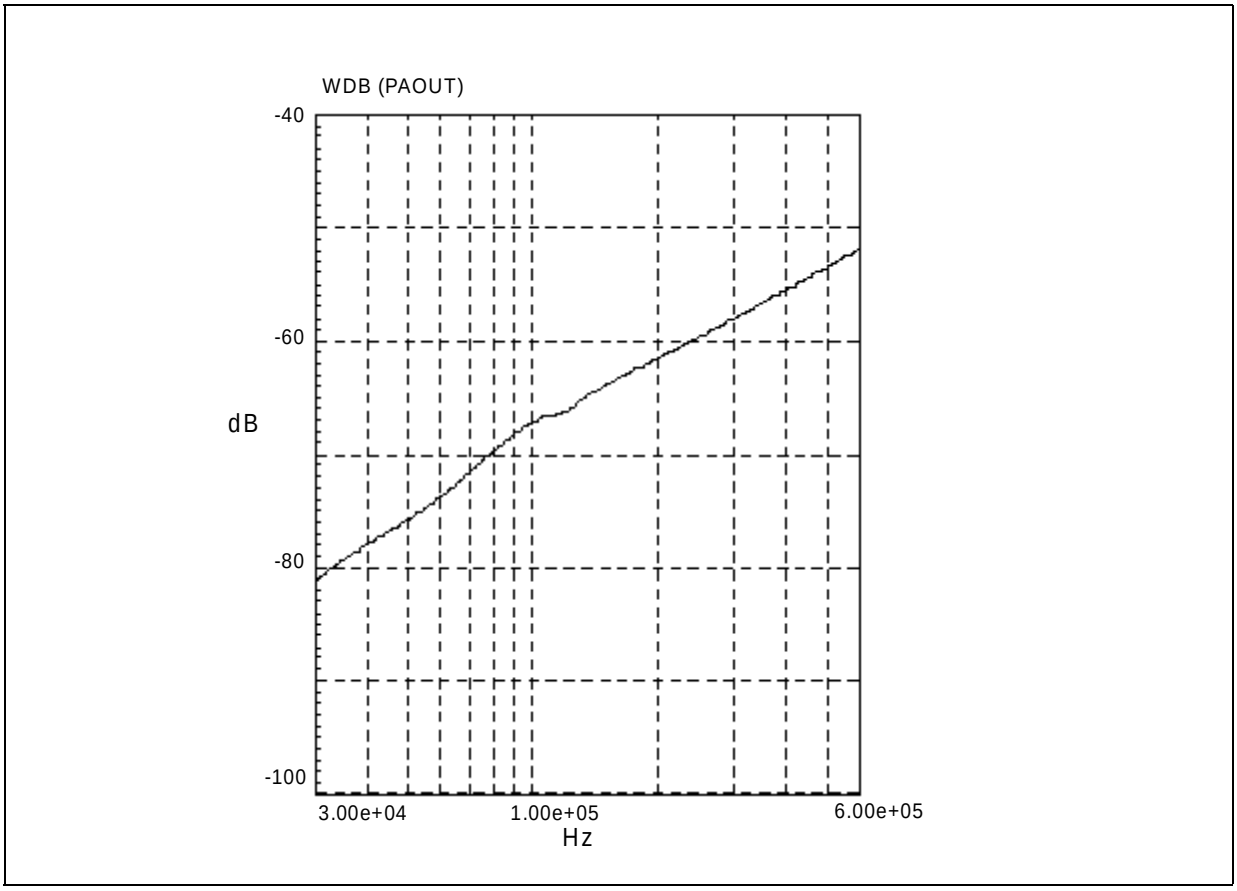
Thermal shutdown junction temperature[12]	130	150	175		^{o}C	Only the power amplifier is shut down under overheat condition

<1> The quiescent current is the current flowing into pin PAOP/PAON when there is no signal.
<2> This is the current drawn from the power supply that is connected to the center tap on the primary side of the transformer.
<3> This is the current flowing into the pin PAIN or PAIP when there is no signal. The nature of the test set up makes this quantity very difficult to measure. It is verified through simulation.
<4> This will allow the distortion specs to be met while driving a 160W line impedance. This applies for a 550mA output current. The worst case impedance for a nominal chip is 200 W.
<5> This spec is meant as an aid in calculating the proper switching point. It applies for a 225mA output current.
<6> This is a requirement on the input signal that allows the distortion spec to be met. It is not a testable parameter. The range has been arrived at from simulations.
<7> The minimum sink current refers to peak signal current in normal operation. This is tested by placing a 80 W load as the line impedance and ensuring that the amplifier still passes the distortion tests. The maximum sink current refers to the current that will be delivered if tip and ring are shorted. A nominal chip can drive a 50W load while a worst case chip will drive 80W.
<8> Slew Rate spec is to guarantee that there is no slewing limit on a maximum amplitude sine wave at 540kHz. A 100 mV step is placed at the power amp input and the slew rate at the output of the amplifier is measured across the 100 Ohm load impedance.
<9> Measured across the 100 Ohm line impedance. This noise spec can be converted to dB/Hz through the following formula,

$$N_{dB} = 10\log\frac{e_n^2 x 1000}{100}$$

The effect of the noise in the receive path can be obtained by subtracting the hybrid balance number.
<10> Two tone distortion is measured with two sine waves with each sine wave at an amplitude of 1/2 full scale (for signal gain of 20.1dB, the full scale signal at power amplifier input is 1.05 Vp). The two tone distortion requirement is measured from the rms voltage of a single signal tone to the rms voltage of the distortion product. For the Two Tone A spec the tones are at f1=500KHz and f2=300KHz giving Im2=200kHz and Im3=100kHz. For the Two tone B the tones are at f1= 500kHz and f2=450kHz so that Im3=550kHz.
<11> A multi-tone sine wave is used for the DS (Down Stream) Multi-tone test. (The multi-tone signal will be 91 sine waves equally spaced from 35x4.3125kHz to 125x4.3125kHz with a peak-to-rms voltage ratio of 5.3 and an rms voltage equal to 208mV. Each tone will have a peak amplitude of 30.8mV) The multi-tone test measures the difference between the power of the test tones and the maximum power of a single distortion product in the given bands.
<12> The thermal shut down can not be directly tested in production. It will be investigated at bench and a correlation will be done hermal shutdown temperature.

Figure 3. Power Supply Rejection of the Power Amplifier[1]



<1>This is a nominal specification. 6 dB of margin should be added to arrive at a worst case spec.

4.3 Programmable Gain Amplifier (PGA) Performance Specifications

It should be noted that the PGA and LPF in the receive path must be AC coupled to avoid problems with amplifying any offsets.

Both the PGA and the amplifiers are specified in terms of the silicon only. This is to allow the system design to be more flexible. The appendices show how to convert some of the silicon specs to system specs.

Table 5. PGA performance Specifications

Unless otherwise specified, NOM specifications apply for VCC=5.0V, temperature range outlined in Table 4.4, nominal process and bias current. MAX and MIN performances with 5% variation on VCC, -40 <= $T_{ambient}$ <=85^{o}C, and worst case process and bias current and a minimum load of 440 W.

DESCRIPTION	MIN	NOM	MAX	UNITS	COMMENTS
Absolute Voltage Gain[1,2] D=00 D=01 D=10 D=11	 11.4 1.4 -5.6 -19.8	 11.8 1.8 -5.2 -19.2	 12.2 2.2 -4.8 -18.8	 dB dB dB dB	Where ‘D’ is the binary value of the control word [PGA1, PGA0] Gain settings are from the pin PGAIN to pin PGAOUT (See ‘application diagram’)

Table 5. PGA performance Specifications

Relative Gain Accuracy[2,3] 11.8<--> 1.8dB step 1.8<--> -5.2 dB step -5.2 <--> -19.2 dB step	 -0.15 -0.17 -0.2	 0 0 0	 0.15 0.17 0.2	 dB dB dB	Assume a fixed Vcc, temperature, and frequency
Gain Variation with Temperature<Superscript>2',<Superscript>3,	-0.1	0	0.1	dB	For a fixed Vcc and frequency (30kHz <=f<=120kHz) relative to 27^{o}
Gain Variation with Supply Voltage<Superscript>2',<Superscript>3,	-0.1	0	0.1	dB	For a fixed frequency (30kHz <=f<=120kHz) and fixed temperature relative to Vcc=5.0V
Gain Variation with Frequency 30KHz <= f <= 120Khz	 -0.1	 -0.001		 dB	For a fixed Vcc and temperature relative to 30kHz
Signal to Distortion Ratio					Measured at pin PGAOUT for a minimum load impedance of 440 Ohm and maximum output signal of 1.1Vp. The important test is the multi tone test. The two tone specs exist because there may be a problem testing a multi tone wave. They will be correlated at bench.
D=00 Two tone[4] IM2 @ 200kHz IM3 @ 100kHz Output DS Multi-tone Echo[5] 30kHz<=f<=120kHz	 86 86 86			 dB dB dB	
D=01 Two tone[4] IM2 @ 200kHz IM3 @ 100kHz Output DS Multi-tone Echo[5] 30kHz<=f<=120kHz	 80 80 80			 dB dB dB	
D=10 Two tone[4] IM2 @ 200kHz IM3 @ 100kHz Output DS Multi-tone Echo[5] 30kHz<=f<=120kHz	 76 76 76			 dB dB dB	
D=11 Two tone[4] IM2 @ 200kHz IM3 @ 100kHz Output DS Multi-tone Echo[5] 30kHz<=f<=120kHz	 76 76 76			 dB dB dB	
Input Referred Noise Voltage[6] at D=00 at D=01 at D=10 at D=11		 5.8 11.6 22.5 95	 7.5 15 30 133	 nV/$\sqrt{Hz}$ nV/$\sqrt{Hz}$ nV/$\sqrt{Hz}$ nV/$\sqrt{Hz}$	Measured at PGAOUT and referred to PGAIN. Tested at f=30kHz,120kHz,150kHz and 500kHz

Table 5. PGA performance Specifications

Input Impedance (over process)[7,8]	4.0	5	6.0	kΩ	Measure at pin PGAIN. For all PGA gains
Input Impedance (over temperature)[7,9]	-10%		10%	kΩ	Measure at pin PGAIN. For all PGA gains
Input Impedance (over process and temperature)[7,10]	3.5	5	6.5	kΩ	Measure at pin PGAIN. For all PGA gains
Input Signal Level @ PGAIN	0		V_{cc}+0.1	V	Single ended input
Maximum Output Signal Level @ PGAOUT[11]			1.1	Vpeak	Referenced to RXANG. For minimum load impedance of 440 Ohms.
Power[12]		19		mW	Active Power

<1> The absolute gain test should be done at 30kHz, 75kHz and 120kHz with maximum output signal level of 1.1Vp.
<2> The calculation to show how to determine the gain from the line is given in Appendix A. This appendix also shows how to cal culate the gain variations in the application
<3> These are chip specs only. The application specs are calculated in Appendix A.
<4> Two tone distortion is measured with two sine waves having an amplitude given in 6. Tone one is at f1=500kHz and tone two is at f2=300kHz, IM2 appears at 200kHz and IM3 appears ar 100kHz.
<5> A multi-tone sine wave is used for the DS (Down Stream) Multi-tone test. (The multi-tone signal will be 91 sine waves equally spaced from 35x4.3125kHz to 125x4.3125kHz with a peak-to-rms ratio of 5.3 and an rms voltage given in Table 6. The multi-tone test measures the difference between the rms voltage of a single tone at the output to the rms voltage of the maximum distortion product at the output in the frequency band between 30kHz to 120kHz.
<6> This is the noise referred to the PGA input pin PGAIN. The input noise can be referenced to tip and ring in dBm/Hz through the formula,

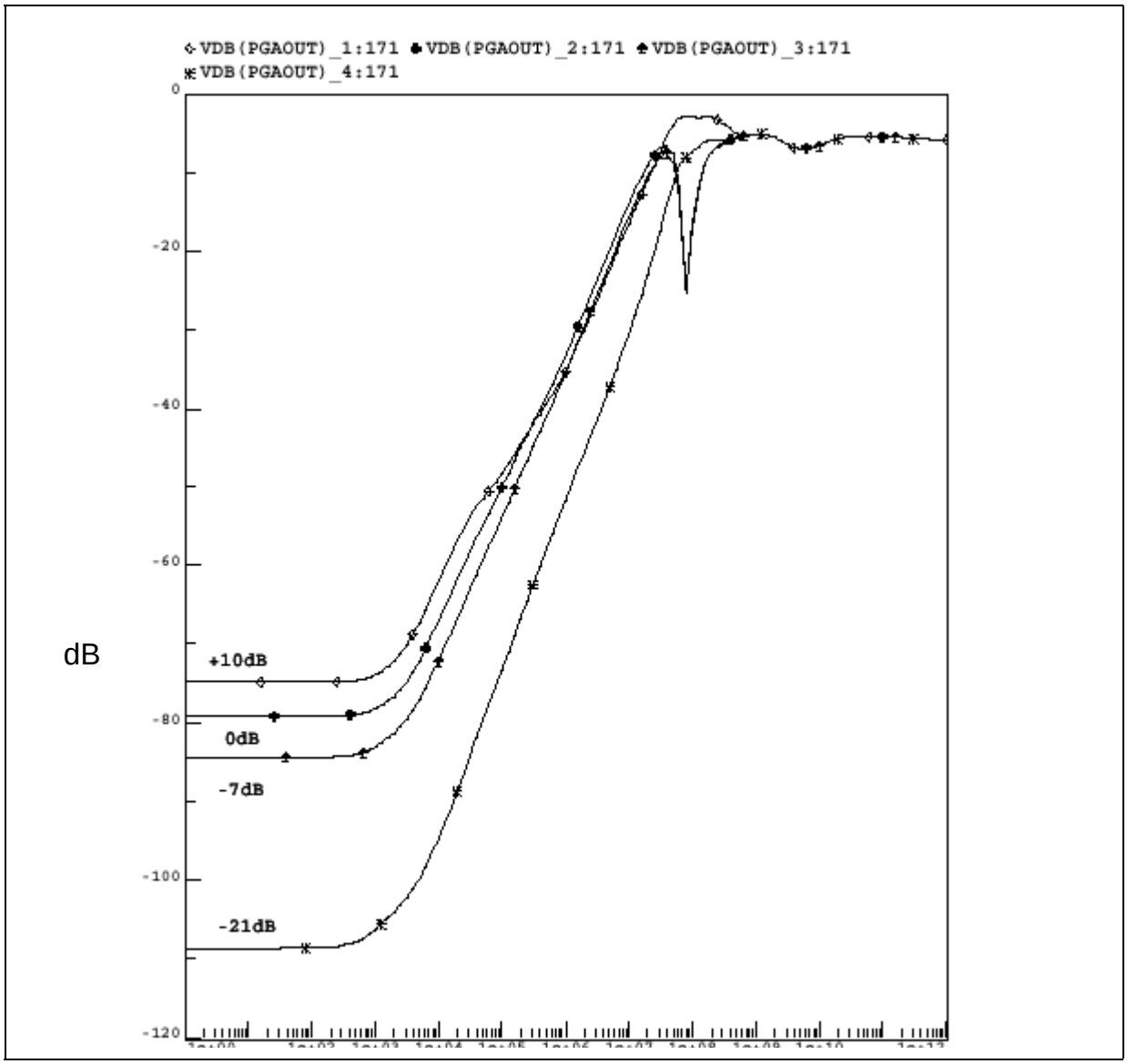
$$N_{dB} = 10\log\left(\frac{100}{1000}V_n^2\right) + G + H$$

where NdB is the line noise in dBm/Hz, Vn is the input referred voltage noise of the PGA, H is the hybrid loss (9.54dB) and G is the gain from the hybrid output to the input of the PGA. See Appendix A for calculation of G. Appendix B shows plots of the noise performance of the entire receive path as shown in Figure 9.
<7> These numbers are required to determine the gain variations in the application.
<8> The input impedance specified here is the nominal value and the variation is due only to processing.
<9> The input impedance specified here is the nominal value and the variation is due only to temperature. This variation is specified from the nominal value at 27°C.
<10> The input impedance specified here is the nominal value with the variation due to both process and temperature.
<11> This spec is guaranteed by the distortion test.
<12> This power can not be verified independently. It can only be measured as part of the power from the RXVCC supply.

Table 6. Multi-tone sine waves

Gain Setting	2 Tone Amplitudes	Multi-tone RMS	Multi-Tone Amplitudes
00	173 mV	66 mV	9.78 mV
01	550 mV	207 mV	30.7 mV
10	1.125 V	414 mV	61.4 mV
11	1.125 V	414 mV	61.4 mV

Figure 4. Power Supply Rejection of the PGA[1]



<1>These curves represent typical performance. 6dB of margin is required for worst case.

4.4 Amplifier Performance Specification

The two amplifiers on the STLC1512 are identical. One of them is used for the second order active low pass filter that follows the PGA in the receive path. The other is an undedicated opamp that can be used either in the transmit or receive paths.

The LPF amplifier is powered from the RXVCC supply and is therefore intended to be used in the receive path. It has its positive terminal tied to the receive AC ground (RXANG) on chip.

The undedicated op amp is powered from TXVCC. It is intended for use in the transmit path but could be used in the receive path. Using it in the receive path may cause receive noise to be coupled into the transmit path. There should not be an issue with transmit noise coupling into the receive path in either configuration.

Table 7. Amplifier Performance Specifications.

Unless otherwise specified, NOM specifications apply for VCC=5V, temperature range outlined in Table 3, nominal process and bias current. MAX and MIN performances with 5% variation on VCC, -40 <= $T_{junction}$ <=115^{o}C, and worst case process and bias current

PARAMETER	MIN	NOM	MAX	UNITS	COMMENTS
Input Offset Voltage			5	mV	
Unity Gain Bandwidth	30	50		MHz	
Phase Margin	50			degrees	
Gain Margin	9			dB	
DC open loop gain	80			dB	
Slew Rate	25			V / us	
Signal to Distortion Ratio in negative unity gain[1] Two Tone A[2] IM2 @ 200 kHz IM3 @ 100 kHz Two Tone B[3] IM3 @ 550 kHz Output DS Multi-tone[4] 30kHz<=f<=120kHz 150kHz<=f<=550kHz	 89 89 59 89 59			 dB dB dB dB dB	Maximum output signal level=1.1Vp The two tone B spec only applies to the undedicated opamp
Signal to Distortion Ratio in positive unity gain. Undedicated opamp only.[1,5] Two Tone A[2] IM2 IM3 Two Tone B[3] IM3 Output DS Multi-tone[4] 30kHz<=f<=120kHz 150kHz<=f<=550kHz	 78 78 59 78 59			 dB dB dB dB dB	Maximum output signal level=1.1Vp
Input referred voltage noise		3.5	5	nV/$\sqrt{Hz}$	
Input referred current noise			2	pA/$\sqrt{Hz}$	

<1>The multi tone spec is the spec which defines system performance. The two tone spec is available because it may not be possible to create an adequate multi-tone signal with the test hardware.

<2>Two tone A distortion is measured with two sine waves with each sine wave at an amplitude of 1/2 full scale. Tone one is at f1=500kHz and tone two is at f2=300kHz.

<3>Two tone B distortion is measured with two sine waves with each sine wave at an amplitude of 1/2 full scale. Tone one is at f1=500kHz and tone two is at f2=450kHz.

<4>A multi-tone sine wave is used for the DS (Down Stream) Multi-tone test. (The multi-tone signal will be 91 sine waves equally spaced from 35x4.3125kHz to 125x4.3125kHz with a peak-to-rms ratio of 5.3, an rms voltage equal to 207mV and a tone amplitude of 30.7mV.) The multi-tone test measures the difference between the rms voltage of a single tone at the output to the rms voltage of the maximum distortion product at the output in the band of interest.

<5>The undedicated op amp specs are available in two configurations since it is undetermined which way the opamp will be used in the application. The distortion specs for the 2 configurations are very different.

Figure 5. Circuit Connection for Measuring Distortion

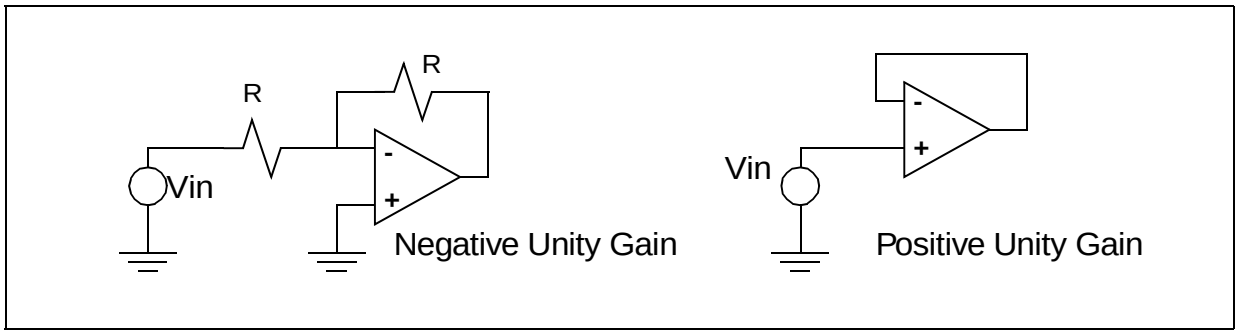
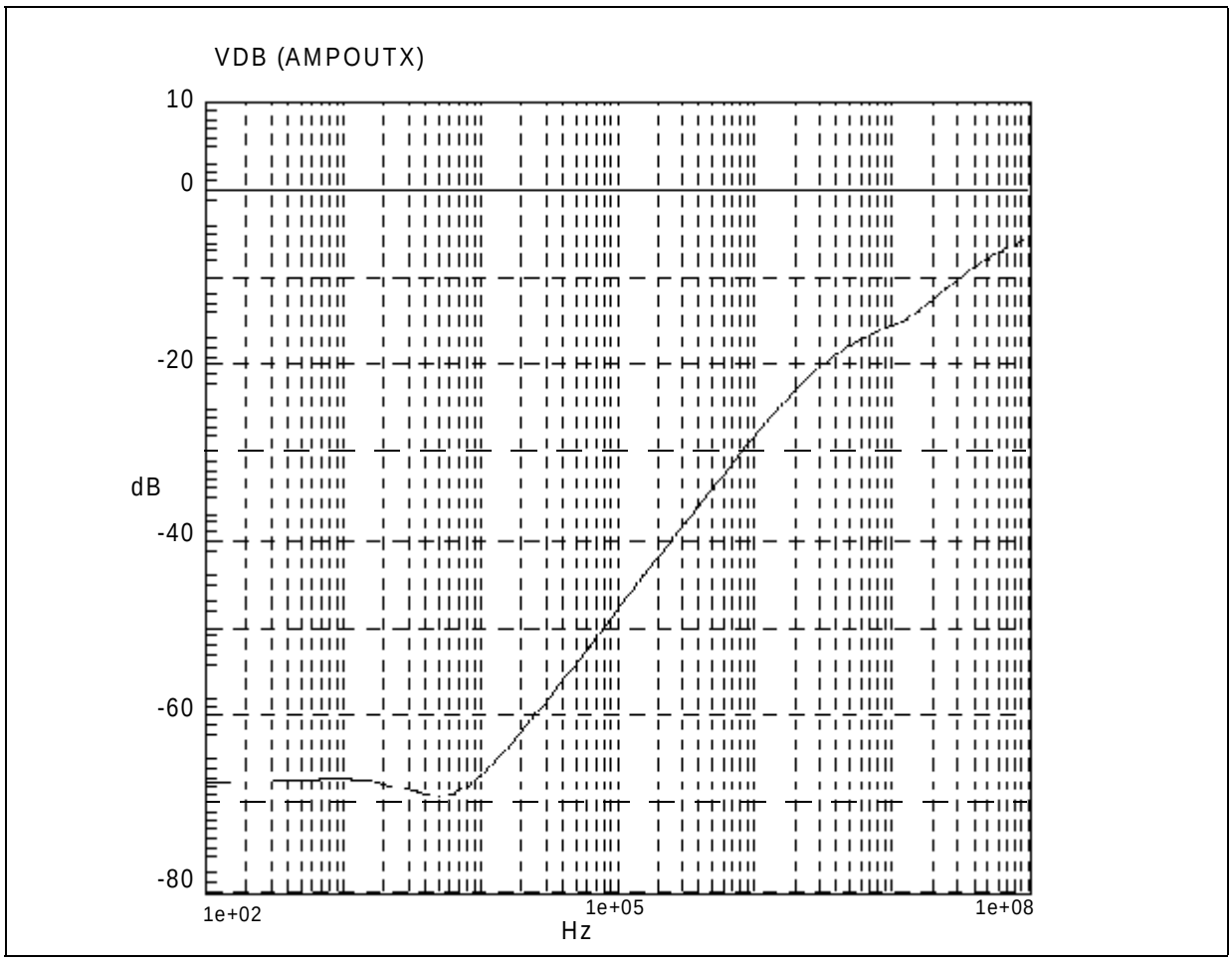


Figure 6. Power Supply Rejection of the Amplifier[1]



<1>This curve is a nominal simulation. 6 dB of margin should be added for worst case.

4.5 Supply Rating and Operating Environment

4.5.1 Environment Conditions

Table 8. Environment conditions

PARAMETER		UNITS	CONDITIONS
Ambient Temperature Range (long-term)	-40 to +80	^{o}C	
Ambient Temperature Range (Short-term)[1]	-40 to +85	°C	

<1>Short-term is defined as no greater than 96 consecutive hours and 15 days per year

4.5.2 Maximum and Minimum Voltage Ratings

Table 9. Maximum and Minimum Voltage Ratings

PINS	Maximum	Minimum
All Vcc pins	6.5V	-0.5V
All other pins	Vcc+0.4V	-0.4V

4.5.3 Power Supplies

Table 10. Power Supply

V/I (PIN NAMES)	Description	MIN	NOM	MAX	UNIT	COMMENTS
V(TXVCC1..2)	Supply voltage for Power Stage	4.75	5.0	5.25	V	
V(TXVCC3)	Supply voltage for TX Path	4.75	5.0	5.25	V	
V(RXVCC1..2)	Supply voltage for RX path	4.75	5.0	5.25	V	
V(PWRVEE1..4)	Ground for PA		0		V	
V(TXVEE1..3))	Ground for Tx path		0		V	
V(RXVEE1..2))	Ground for Rx path		0		V	
P(TXVCC1..2)	Current drawn by TXVCC1..2		36.6		mArms	While passing a full scale signal. [1]
P(TXVCC1..2)	Current drawn by TXVCC1..2	12.8		15.6	mArms	Quiescent Current
P(TXVCC3)	Current drawn by TXVCC3		12		mArms	While passing a full scale signal.<Superscript>1
P(TXVCC3)	Current drawn by TXVCC3	7.5		9.2	mArms	Quiescent Current

Table 10. Power Supply

P(RXVCC1..2)	Current drawn by RXVCC		8.6		mArms	While passing a full scale signal.<Superscript>1
P(RXVCC1..2)	Current drawn by RXVCC	6.6		8.4	mArms	Quiescent Current
P(PAON/PAOP)	Current supplied through the center tap of the transformer.		93		mArms	RMS while driving a DMT signal.<Superscript>1
P(PAON/PAOP)	Current supplied through the center tap of the transformer.	20		36	mArms	Quiescent Current

<1>The nominal power is all that is available for the active power because the power is very dependent on the line impedance.

4.5.4 Power Supply Noise

Table 11. Power Supply Noise

Noise Band	Maximum RXVCC Supply Noise Spectral Density	Maximum TXVCC Supply Noise Spectral Density
30kHz<f<120kHz	0.2uVrms/$\sqrt{Hz}$ @ 120kHz, rising 20dB per decade for decreasing frequency	10uVrms/$\sqrt{Hz}$@120kH,following 10dB per decade for decreasing frequency to 3uVrms/$\sqrt{Hz}$ @ 30kHz
150kHz<f<540kHz	0.1uVrms/$\sqrt{Hz}$@540kHz, rising 20dB per decade for decreasing frequency	1uVrms/$\sqrt{Hz}$@540kHz, rising 20dB per decade for decreasing frequency to 7uVrms/$\sqrt{Hz}$ @150kHz

4.5.5 References

Table 12. References

PIN NAMES	Description	MIN	NOM	MAX	UNIT	COMMENTS
RBIAS	External resistance for bias current generation	12.3	12.4	12.5	KΩ	To create 200uA bias current.
REF2P5	External reference voltage for AC Ground.	2.425	2.5	2.575	V	External reference voltage must be 3% accurate
I(REF2P5)	Current supplied to REF2P5		3.75uA	8.25uA	V	
TXANG/ RXANG	Tx and Rx AC ground current sinking capability	REF2P5* 0.97	REF2P5	REF2P5* 1.03	V	1mA source/sink

4.6 Digital Interface Logic Level

Table 13. Definition of Logic Levels for Digital Control Input Pins

SYMBOL	DESCRIPTION	MIN	NOM	MAX	UNITS	COMMENTS
VIL	Input low voltage			0.8	V	Signal from STLC1510
VIH	Input high voltage	2.0			V	Signal from STLC1510

4.7 ESD and Latch Up

Table 14. ESD and Latch up

Parameter	Conditions	Min	Obj	Max	Unit
Electrostatic Discharge[1]		1	2		kV
Latchup current		100	200		mA

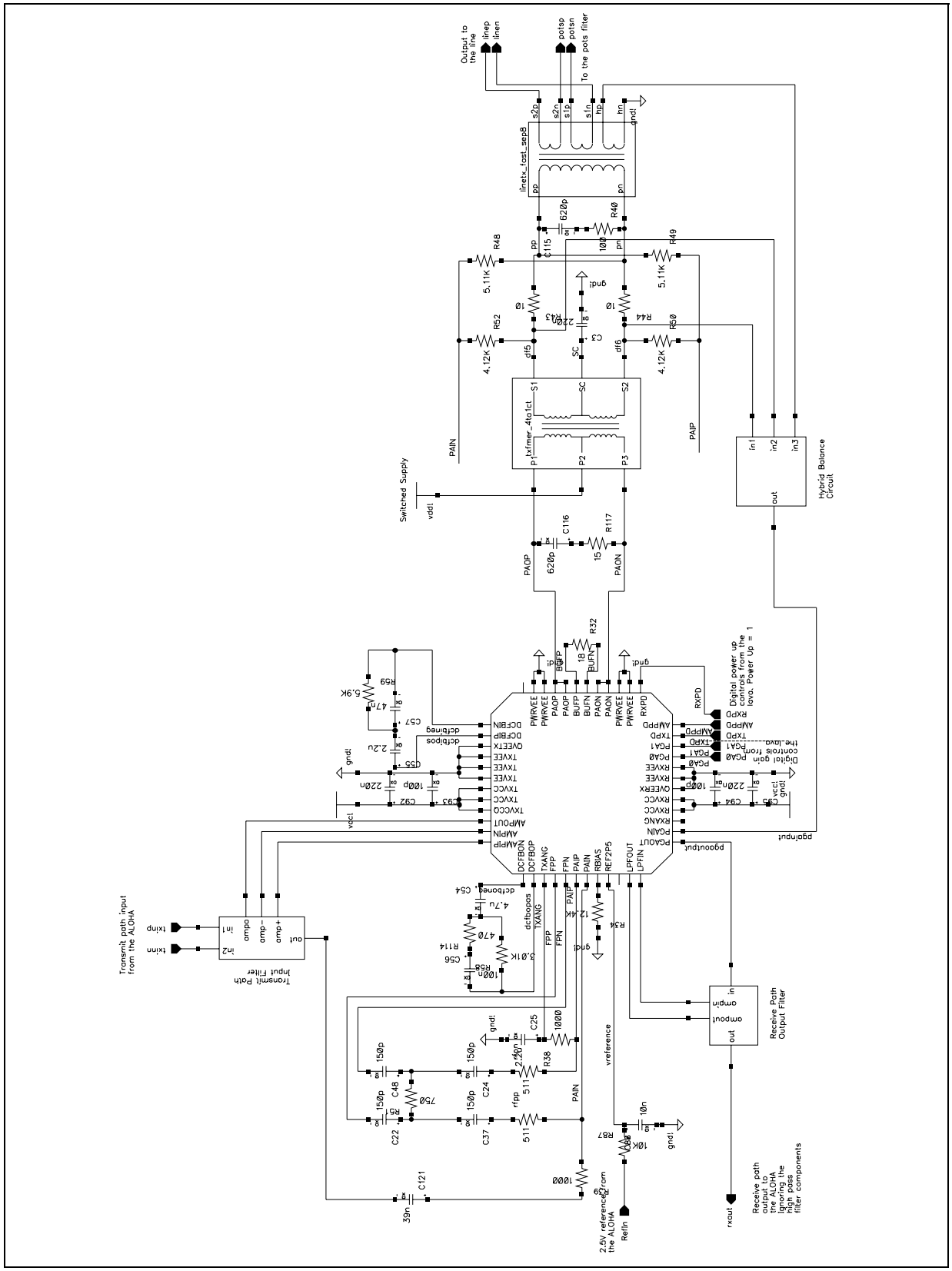
<1>Test assumes standard Human body ESD model. Industry standard requirement is 1kV.

5.0 APPLICATION DIAGRAM

To reduce the power consumption of the power amplifier, the two output power transistors of the power amplifier are powered by a switching power supply at the center tap of the transformer. (See Figure 7.) The switching is controlled by the digital chip (STLC1510) that senses the future signal level.

The stability and offset of the power amplifier are optimized with the feedback scheme and the component values shown in this application diagram. As such, the application of the STLC1512 has to follow the topology and component values in the diagram to avoid stability and offset problems.

Figure 7. Application Diagram



Appendix A - PGA Gain Calculations

The application requires some drop from the output of the hybrid balance to the input of the PGA in order to keep the signal level at an acceptable level. (see Table 5) The input is reduced by placing a resistor between the output of the hybrid balance network and PGAIN. This resistor (R_{ext}) serves two purposes. First, it creates a resistor divider between the hybrid balance and the input. Second, it allows a capacitor to be placed across the input of the PGA to create a first order low pass filter. This further reduces the signal in long loop cases.

The resistor divider is formed by the external resistor and the input impedance of the PGA. The gain from the hybrid balance to the output of the PGA is therefore given by

$$20\log\left(\frac{R_{input}}{R_{input}+R_{ext}}\right)+G_{table}$$

where G_{table} is the gain number given in Table ,
R_{input} is the input impedance of the PGA given in Table
R_{ext} is the resistance placed between the hybrid balance and PGAIN.

Equation can also be used to determine variations over process and temperature. To accomplish this just determine the max and min values using the input resistance variation given in Table .

To convert the noise numbers in Table to line referred noise numbers use

$$N_{dB} = 10\log\left(\frac{1000}{100}V_n^2\right)+G+H$$

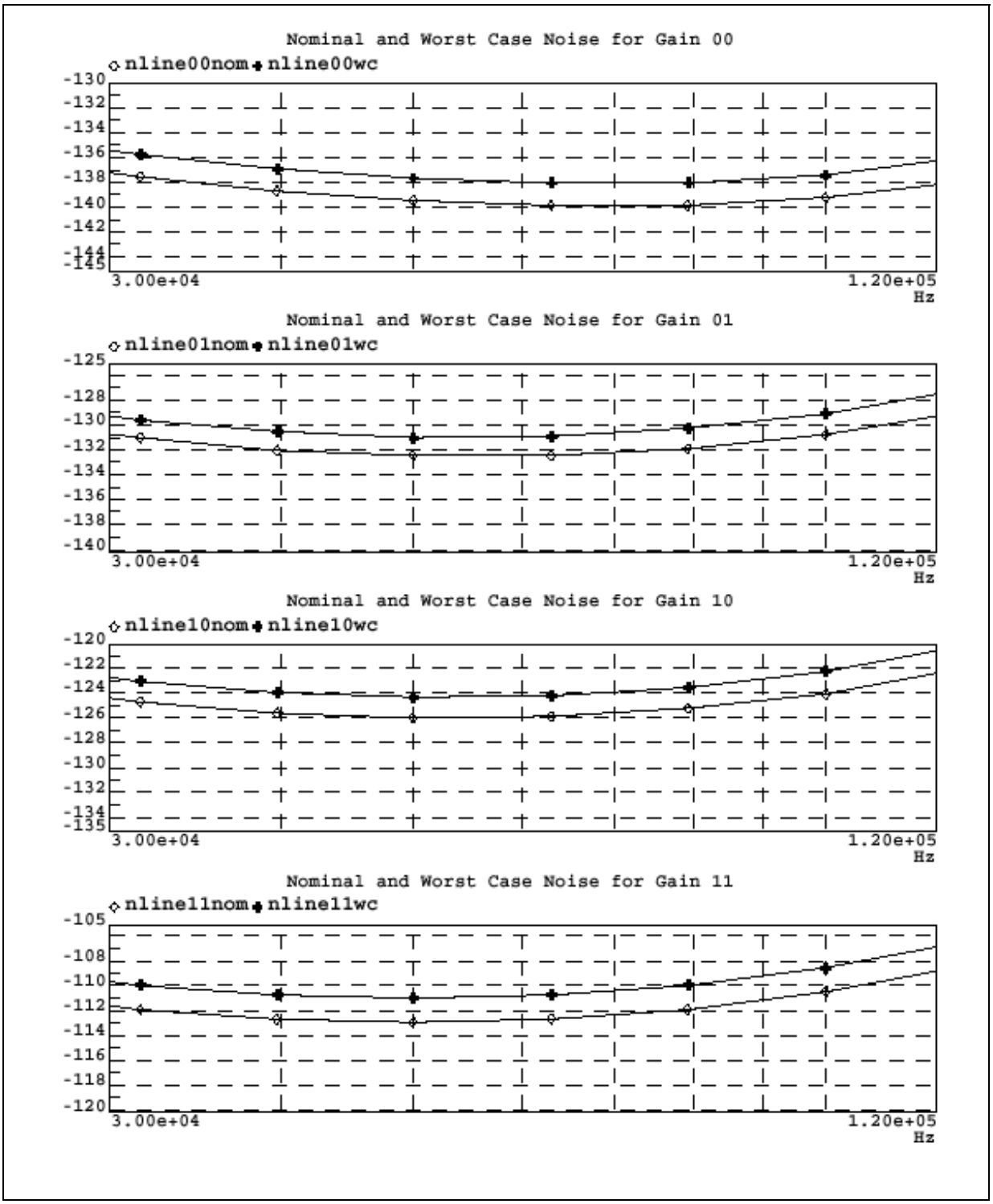
Where N_{db} is the noise on the line in dBm/Hz,
V_n is the input referred noise from Table ,
H is the hybrid loss (9.54dB in the reference design),
and G is given by

$$G = 20\log\left(\frac{R_{input}+R_{ext}}{R_{input}}\right)$$

Appendix B - Rx Path Noise Performance

The following plots show the noise performance of the receive path as it is shown in Figure 7. They show the effects of different gain settings as well as typical and worst case performance of the receiver. These noise numbers are referred to the line.

Figure 8. Noise for Various Gain Settings



Appendix C - Transmit Path Noise Performance

The following plots show the noise performance of the transmit path as it is connected in Figure 7.

Figure 9. Transmit Filter Noise Performance at he Filter Output (nV/$\sqrt{Hz}$)

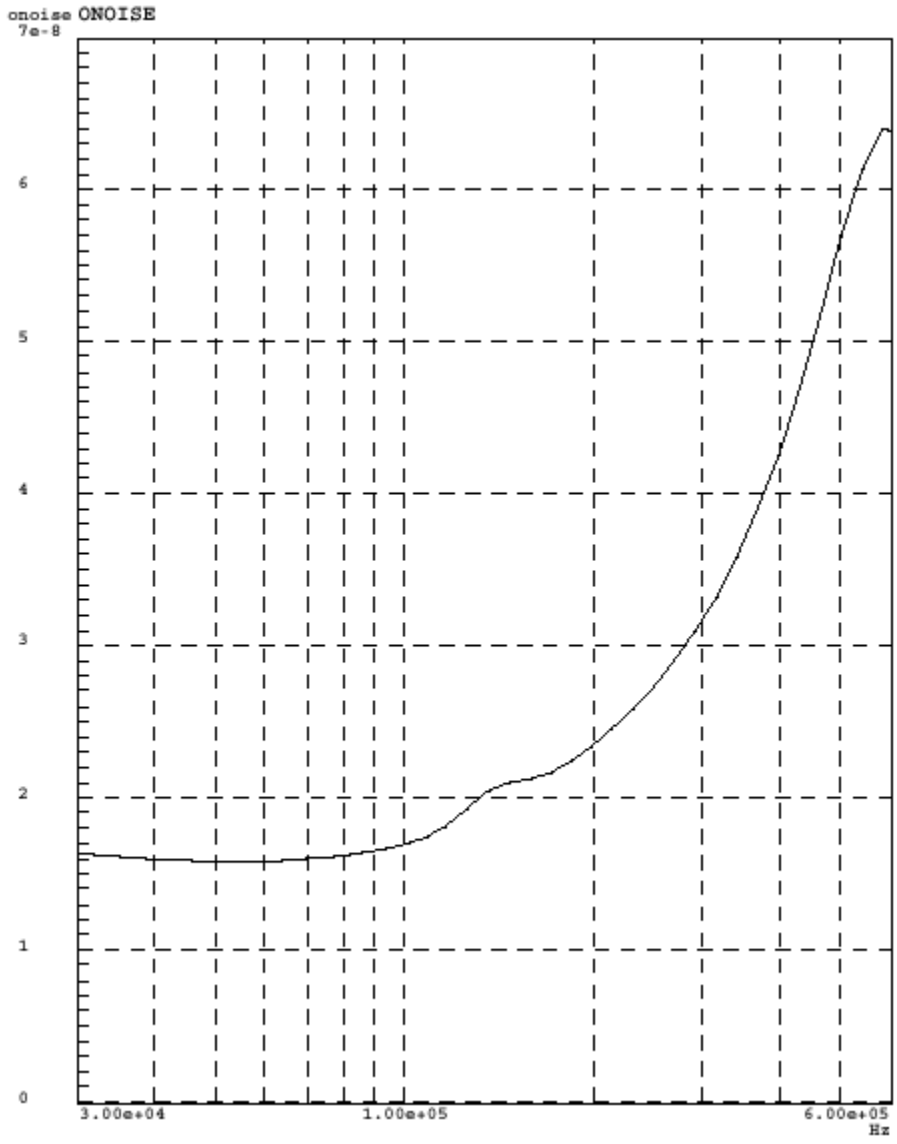


Figure 10. Power Amp Noise Performance at the Line (nV/$\sqrt{Hz}$)

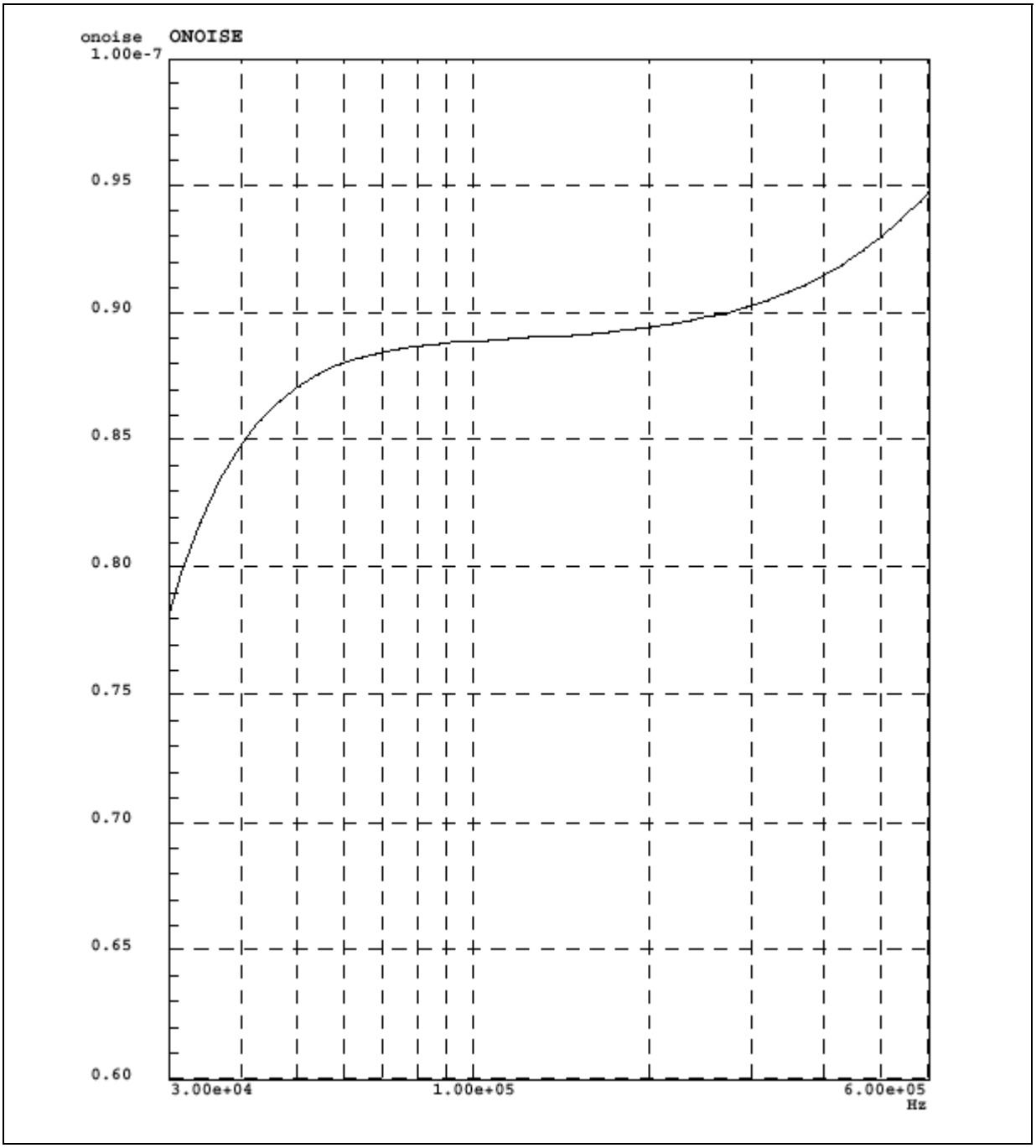
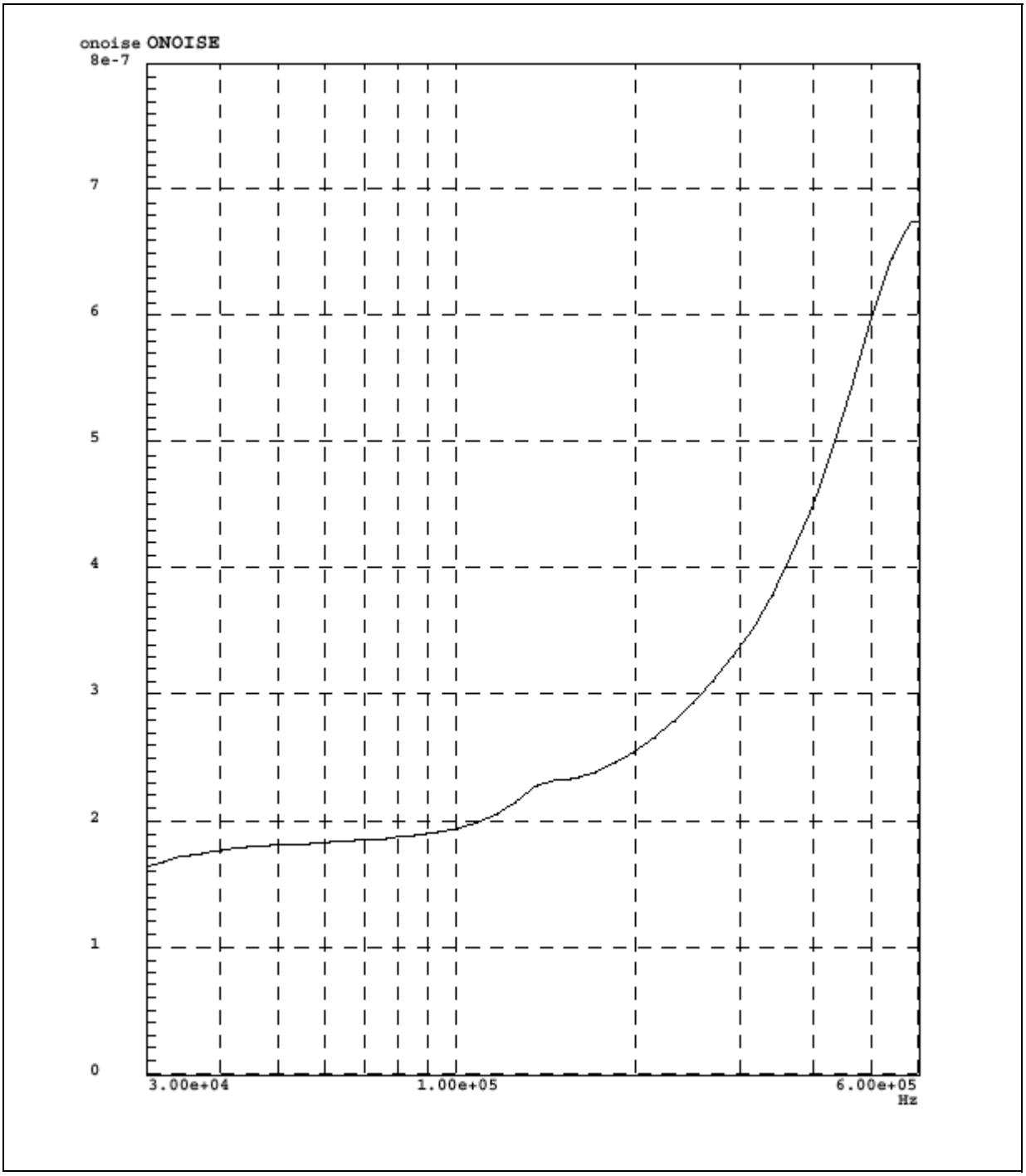


Figure 11. Total Transmit Path Noise Performance at the Line (nV/$\sqrt{Hz}$)



Appendix D - Headroom Calculation for Switching

The headroom for switching can be determined from the numbers in Table 4. The switching headroom is 0.70 V at low currents (i.e. while on the low supply rail) and 0.85 V at high currents (i.e. while on the high supply rail). The most difficult number to arrive at is the voltage that will appear at the pins PAOP1,2 and PAON1,2. This is a combination of the input voltage, the line impedance and the losses in the transformers.
For a 100Ω load the maximum signal on the line will be 10.7 V. Since we are generating an active 100Ω output impedance the voltage on the line for any other load is given by:

$$V_{line} = 2(10.7)\left(\frac{Z_o}{100 + Z_o}\right) \quad \text{(EQ D.1)}$$

where Z_o is the line impedance and V_{line} is the voltage on the line.
There are various losses in the transformers that can be modeled as resistors. To calculate the effect of these losses we must know the current through the load which is given by:

$$I_{load} = \frac{V_{line}}{Z_o} \quad \text{(EQ D.2)}$$

The loss through the line transformer can be modeled as a 2.6Ω resistor. There is also a drop across the two 10Ω reference resistors. Therefore to determine the voltage at the output of the switched transformer we have:

$$V_{swtxout} = V_{line} + (20 + 2.6)I_{load} \quad \text{(EQ D.3)}$$

At this point there is some additional current that flows through the hybrid balance network. This current flows through a resistance that is equivalent to 1270Ω. Therefore the current flowing out of the switched transformer is:

$$I_{swtxout} = I_{load} + \frac{V_{swtxout}}{1270} \quad \text{(EQ D.4)}$$

The switched transformer has losses that can be modeled as a 3.6Ω resistor and has a 4:1 turns ratio. Therefore the voltage at the primary side of the transformer is given by:

$$V_{PAOx} = \frac{V_{swtxout} + 3.6(I_{swtxout})}{4} \quad \text{(EQ D.5)}$$

Where V_{PAOx} is the voltage at the output pins of the power amp. This is essentially the amount of headroom required to drive a full scale signal into the desired line impedance (Z_o). Equation D.1 to Equation D.5 can be combined to calculate the required headroom to drive a certain impedance.

$$V_{PAOx} = \frac{V_n}{2}\left(\frac{Z_o + 20 + 2.6 + 3.6\left(\frac{Z_o + 20 + 2.6}{1270} + 1\right)}{Z_o + 100}\right) \quad \text{(EQ D.6)}$$

Where V_{PAOx} is the required headroom to drive V_n volts out onto a line with the impedance Z_o. This equation can be rearranged to calculate the switching threshold. The headroom can be determined from the drop across the diode from the low supply and the low current drive capability of the amplifier given in Table (0.70V).

$$V_{headroom} = V_{supplymin} - 0.70 - V_{diode} \quad \text{(EQ D.7)}$$

Where $V_{supplymin}$ is the minimum value for the lower supply, $V_{headroom}$ is the headroom available on the low supply and V_{diode} is the voltage drop across the diode when it has the appropriate amount of current flowing through it.
Substituting $V_{headroom}$ in for V_{PAOx} in Equation D.7 you can determine the allowable output voltage V_n. This can be scaled to the nominal value of 10.7V (full scale) to determine a switching threshold based on the full scale level of the signal.
The headroom calculation is worst at maximum line impedance. There is also a supply rail requirement for the high (5.0V) supply which is based on being able to supply enough current to drive an 80 Ω line impedance. This is not a trivial calculation and has been based on simulations. The possibility exists that the requirements on the minimum supply voltage may be able to be reduced in the future.

Appendix E - Board Issues for Heat Dissipation

The internal temperature of the device must remain below 125^{o}C. There are a number of ways to ensure that this happens.

There are various combinations of maximum ambient temperature and board issues that can contribute to the junction temperature of the devices on the chip. Different layout techniques can be used to enhance the thermal coefficient of the package. The following conditions must be true to ensure reliable operation of the line driver.

$$T_{ambient} + R_j(P_D) < 125^{o}C \quad \text{(EQ E.1)}$$

Where $T_{ambient}$ is the maximum ambient temperature that will be experienced by the device, R_j is the thermal coefficient as described below and P_D is the power dissipation of the chip which is 480mW.

The thermal coefficient is determined by the board layout characteristics and the rate that air is being forced across the board. The board layout is defined in 2 ways. One is a 2 layer board with signal layers on the top and bottom. The signal layer has a heat spreading copper plane that spreads from the corner pins of the chip. There are also thermal vias directly under the chip. The second layout is an 8 layer board with signal layers on the top an bottom, 4 copper lattice planes (80% 1 ounce copper) and 2 copper ground planes (solid 1 ounce copper). This layout also has a heat spreading copper plane on the signal layer and thermal vias under the die and in the copper plane.

The thermal coefficients for these two different boards are given in Table 15. These coefficients are modified based on the amount of air flow over the board..

Table 15. Thermal Coefficients for Different Board Conditions

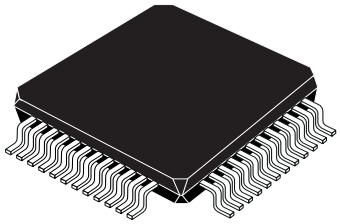
Board Type	R_j No Air Flow (^{o}C/W)	R_j 1m/s Air Flow (^{o}C/W)	R_j 3m/s Air Flow (^{o}C/W)	R_j 5m/s Air Flow (^{o}C/W)
2 Layer	87.2	75.6	63.6	59.4
8 Layer	54.7	50.6	48.0	46.1

6.0 MECHANICAL SPECIFICATIONS

The STLC1512 is packaged in a 48 pin 7x7x1.4mm Lowprofile Quad Flat Pack (LQFP) package.

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.006	0.008	0.010
C	0.09		0.20	0.004		0.008
D		9.00			0.354	
D1		7.00			0.276	
D3		5.50			0.217	
e		0.50			0.020	
E		9.00			0.354	
E1		7.00			0.276	
E3		5.50			0.217	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0°(min.), 3.5°(typ.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



Body: 7 x 7 x 1.40mm

TQFP48