4Mx32 SDRAM
90FBGA
(VDD/VDDQ 3.0V/3.0V & 3.3V/3.3V)

Revision 0.8

November 2001

Revision History

Revision 0.0 (March 26. 2001, Preliminary)
- First generation for 4Mx32 3.0V SDRAM FBGA.

Revision 0.1 (May 3. 2001, Preliminary)
- Change of IOH and IOL from -0.1mA and 0.1mA to -2mA and 2mA.

Revision 0.2 (May 18. 2001, Preliminary)
- Change of ball configuration in order to be compatible with JEDEC standard package in case of sequential operatin.
- Ball location of A3, A11 and A7 is different from JEDEC standard.

Revision 0.3 (June 11. 2001, Target)
- Change of ball configuration in order to be compatible with JEDEC standard package perfectly.

Revision 0.4 (June 22. 2001, Target)
- Changed device name from low power sdram to mobile sdram.

Revision 0.5 (June 26. 2001, Target)
- Integration to K4S283233F-MXXX of 3.0V and 3.3V part.
- Integration to -1L code of -1L and -15 code.

Revision 0.6 (July 12. 2001, Target)
- Addition of -1H part specification.
- Change tSH for 100MHz, CL3 part from 1.5ns to 1ns.

Revision 0.7 (July 12. 2001, Preliminary)
- Reduction of DC Current.

Revision 0.8 (November 1. 2001, Final)
- 4Mx32 Final Specification.

1M x 32Bit x 4 Banks SDRAM in 90FBGA

FEATURES

- 3.0V & 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS latency (1 & 2 & 3)
  - -. Burst length (1, 2, 4, 8 & Full page)
  - -. Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle).
- Extended Temperature Operation (-25°C ~ 85°C).
- 90Balls FBGA based on 2 pcs of 4Mx16 SDRAM.

GENERAL DESCRIPTION

The K4S283233F is 134,217,728 bits synchronous high data rate Dynamic RAM organized as 4 x 1,048,576 words by 32 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock and I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

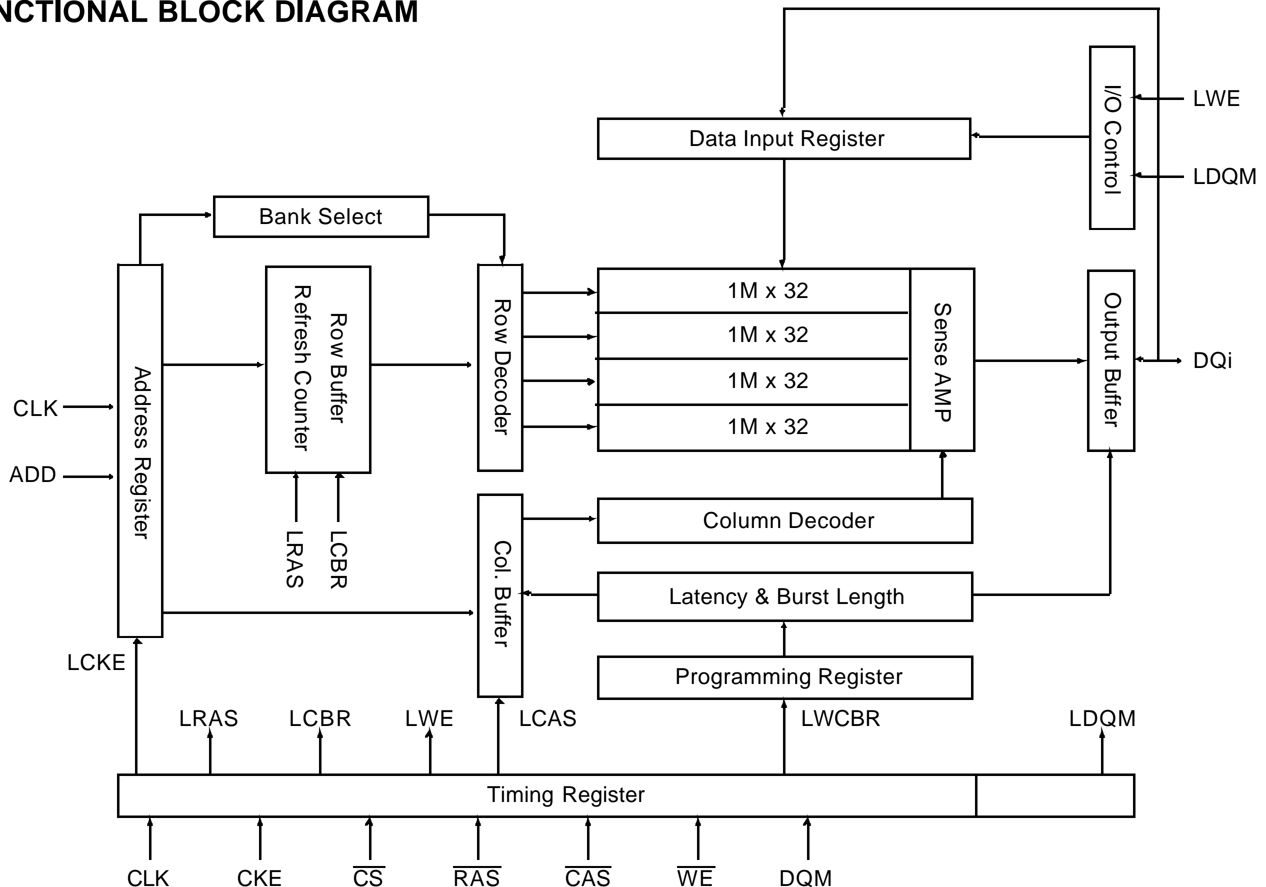
ORDERING INFORMATION

Part No.	Max Freq.	Interface	Package
K4S283233F-ME/N75	133MHz(CL=3) 100MHz(CL=2)	LVTTL	90 Balls FBGA
K4S283233F-ME/N1H	100MHz(CL=2)		
K4S283233F-ME/N1L	100MHz(CL=3)*1		

- ME ; Normal Power, Extended Temperature.
- MN ; Low Power, Extended Temperature.

Note :1. In case of 40MHz Frequency, CL1 can be supported.

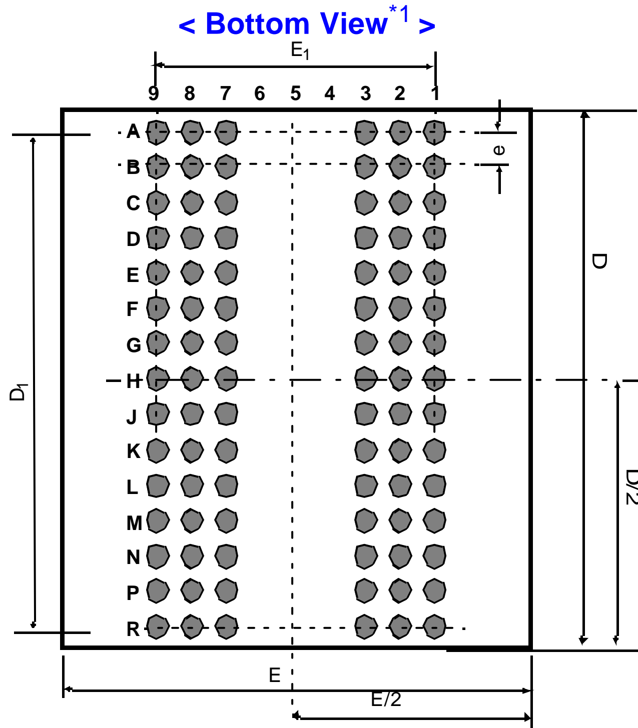
FUNCTIONAL BLOCK DIAGRAM



* Samsung Electronics reserves the right to change products or specification without notice.

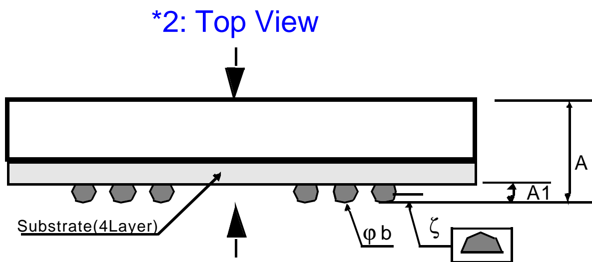
Package Dimension and Pin Configuration

< Bottom View*1 >



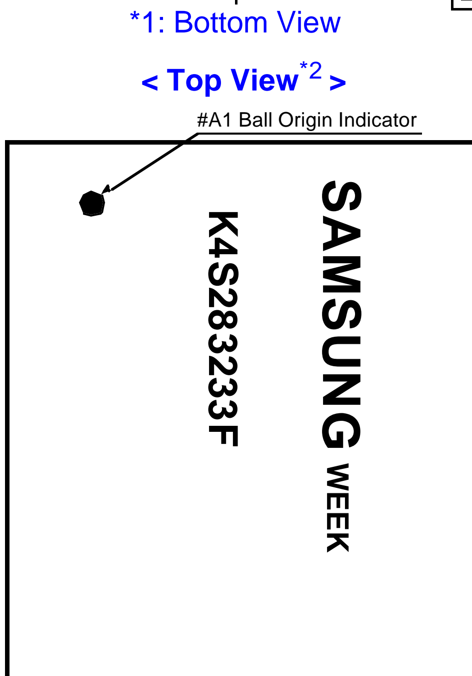
< Top View*2 >

90Ball(6x15) CSP						
	1	2	3	7	8	9
A	DQ26	DQ24	VSS	VDD	DQ23	DQ21
B	DQ28	VDDQ	VSSQ	VDDQ	VSSQ	DQ19
C	VSSQ	DQ27	DQ25	DQ22	DQ20	VDDQ
D	VSSQ	DQ29	DQ30	DQ17	DQ18	VDDQ
E	VDDQ	DQ31	NC	NC	DQ16	VSSQ
F	VSS	DQM3	A3	A2	DQM2	VDD
G	A4	A5	A6	A10	A0	A1
H	A7	A8	NC	NC	BA1	A11
J	CLK	CKE	A9	BA0	$\overline{CS}$	$\overline{RAS}$
K	DQM1	NC	NC	$\overline{CAS}$	$\overline{WE}$	DQM0
L	VDDQ	DQ8	VSS	VDD	DQ7	VSSQ
M	VSSQ	DQ10	DQ9	DQ6	DQ5	VDDQ
N	VSSQ	DQ12	DQ14	DQ1	DQ3	VDDQ
P	DQ11	VDDQ	VSSQ	VDDQ	VSSQ	DQ4
R	DQ13	DQ15	VSS	VDD	DQ0	DQ2



Pin Name	Pin Function
CLK	*System Clock*
$\overline{CS}$	*Chip Select*
CKE	*Clock Enable*
A0 ~ A11	*Address*
BA0 ~ BA1	*Bank Select Address*
$\overline{RAS}$	*Row Address Strobe*
$\overline{CAS}$	*Column Address Strobe*
$\overline{WE}$	*Write Enable*
DQM0 ~ DQM3	*Data Input/Output Mask*
DQ0 ~ 31	*Data Input/Output*
VDD/VSS	*Power Supply/Ground*
VDDQ/VSSQ	*Data Output Power/Ground*

< Top View*2 >



[Unit:mm]

Symbol	Min	Typ	Max
A	1.35	1.40	1.45
A_1	0.30	0.35	0.40
E	-	11.00	-
E_1	-	6.40	-
D	-	13.00	-
D_1	-	11.20	-
e	-	0.80	-
φb	0.40	0.45	0.50
ζ	-	-	0.10

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = -25 to 85°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	2.7	3.0	3.6	V	
	V_{DDQ}	2.7	3.0	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Note :
1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is $\leq$ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is $\leq$ 3ns.
3. Any input 0V $\leq V_{IN} \leq V_{DDQ}$.
   Input leakage currents include HI-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V $\leq V_{OUT} \leq V_{DDQ}$.

CAPACITANCE (VDD = 3.0V, TA = 23°C, f = 1MHz, VREF =0.9V ± 50 mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	C_{CLK}	4.0	8.0	pF	
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM	C_{IN}	4.0	8.0	pF	
Address	C_{ADD}	4.0	8.0	pF	
DQ_0 ~ DQ_{31}	C_{OUT}	3.0	6.5	pF	

DC CHARACTERISTICS

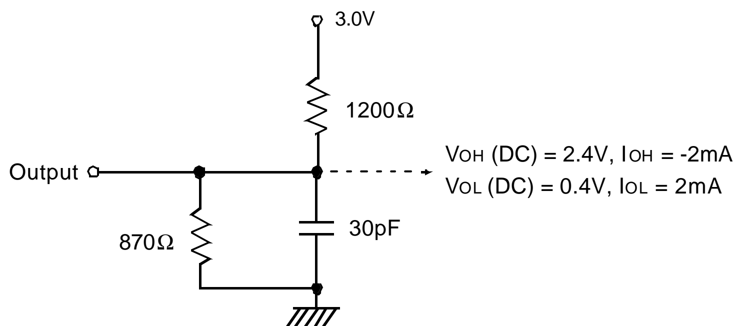
Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = -25 to 85°C)

Parameter	Symbol	Test Condition		Version			Unit	Note
				-75	-1H	-1L		
Operating Current (One Bank Active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA		150	140	130	mA	1
Precharge Standby Current in power-down mode	$I_{CC2}P$	CKE $\leq V_{IL}$(max), t_{CC} = 10ns		2			mA	
	$I_{CC2}PS$	CKE & CLK $\leq V_{IL}$(max), $t_{CC} = \infty$		2				
Precharge Standby Current in non power-down mode	$I_{CC2}N$	CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), t_{CC} = 10ns Input signals are changed one time during 20ns		30			mA	
	$I_{CC2}NS$	CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), $t_{CC} = \infty$ Input signals are stable		12				
Active Standby Current in power-down mode	$I_{CC3}P$	CKE $\leq V_{IL}$(max), t_{CC} = 10ns		6			mA	
	$I_{CC3}PS$	CKE & CLK $\leq V_{IL}$(max), $t_{CC} = \infty$		6				
Active Standby Current in non power-down mode (One Bank Active)	$I_{CC3}N$	CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), t_{CC} = 10ns Input signals are changed one time during 20ns		50			mA	
	$I_{CC3}NS$	CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), $t_{CC} = \infty$ Input signals are stable		30			mA	
Operating Current (Burst Mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks Activated t_{CCD} = 2CLKs		220	180	170	mA	1
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		250	220	210	mA	2
Self Refresh Current	I_{CC6}	CKE $\leq$ 0.2V	-ME	2			mA	3
			-MN	800			uA	4

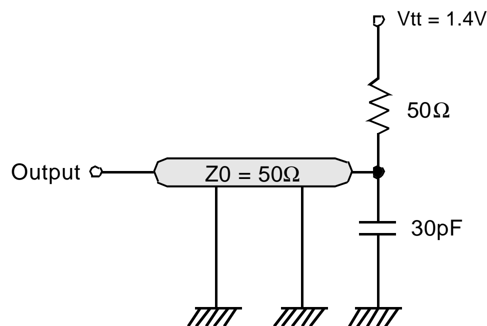
Notes :
1. Measured with outputs open.
2. Refresh period is 64ms.
3. K4S283233F-ME**
4. K4S283233F-MN**
5. Unless otherwise noted, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ})

AC OPERATING TEST CONDITIONS (V_{DD} = 2.7V ~ 3.6V, T_A = -25 to 85°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			- 75	-1H	-1L		
Row active to row active delay		t_{RRD}(min)	15	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		t_{RCD}(min)	20	20	24	ns	1
Row precharge time		t_{RP}(min)	20	20	24	ns	1
Row active time		t_{RAS}(min)	45	50	60	ns	1
		t_{RAS}(max)	100			us	
Row cycle time		t_{RC}(min)	65	70	84	ns	1
Last data in to row precharge		t_{RDL}(min)	2			CLK	2
Last data in to Active delay		t_{DAL}(min)	2 CLK + tRP			-	
Last data in to new col. address delay		t_{CDL}(min)	1			CLK	2
Last data in to burst stop		t_{BDL}(min)	1			CLK	2
Col. address to col. address delay		t_{CCD}(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1				
	CAS latency=1		-	0			

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	- 75		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	7.5	1000	10	1000	10	1000	ns	1
	CAS latency=2		10		10		12			
	CAS latency=1		-		-		25			
CLK to valid output delay	CAS latency=3	t_{SAC}		5.5		6		6	ns	1,2
	CAS latency=2			6		6		6		
	CAS latency=1			-		-		18		
Output data hold time	CAS latency=3	t_{OH}	2		2		2		ns	2
	CAS latency=2		2		2		2			
	CAS latency=1		-		-		2			
CLK high pulse width		t_{CH}	2.5		3		3		ns	3
CLK low pulse width		t_{CL}	2.5		3		3		ns	3
Input setup time		t_{SS}	2.5		3		3		ns	3
Input hold time		t_{SH}	1		1		1		ns	3
CLK to output in Low-Z		t_{SLZ}	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		5.5		6		6	ns	
	CAS latency=2			6		6		6		
	CAS latency=1			-		-		18		

Notes :
1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A_0~ A_7)	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A_0~ A_7)	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code
A_0 ~ A_{11} & BA_0 ~ BA_1 : Program keys. (@MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. BA_0 ~ BA_1 : Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at the positive going edge of CLK masks the data-in at that same CLK in write operation (Write DQM latency is 0), but in read operation makes the data-out Hi-Z state after 2 CLK cycles. (Read DQM latency is 2).

Note : Samsung shall not offer for sale or sell either directly or through and third-party proxy, and DRAM memory products that include "Multi-Die Plastic DRAM" for use as components in general and scientific computers such as, by way of example, mainframes, servers, work stations or desk top computers for the first three years of five year term of this license. Nothing herein limits the rights of Samsung to use Multi-Die Plastic DRAM in other products or other applications under paragrangh such as mobile, telecom or non-computer application(which include by way of example laptop or notebook computers, cell phones, televisions or visual monitors)

Violation may subject the customer to legal claims and also excludes any warranty against infringement from Samsung."