1.25Gbps Fiber-Optic VCSEL/Laser Driver

GENERAL DESCRIPTION

The CS6706 is a high-speed fiber optic VCSEL driver suited for applications up to 1.25Gbps. The CS6706 accepts differential PECL inputs, and includes a CMOS disable pin for bias and modulation current control. Further, the bias and modulation current can be set independently via two external resistors, and the rise/fall time can also be adjusted using external resistors.

A monitor photodiode can be incorporated in the application circuit to ensure a stable laser power source. Any failure of the laser is detected using the two on-chip window comparators. Once a failure is detected, the laser power safety switch will be triggered and can only be reset by a power off condition.

The slow start feature allows bias current to settle before modulation current output begins, to protect the laser.

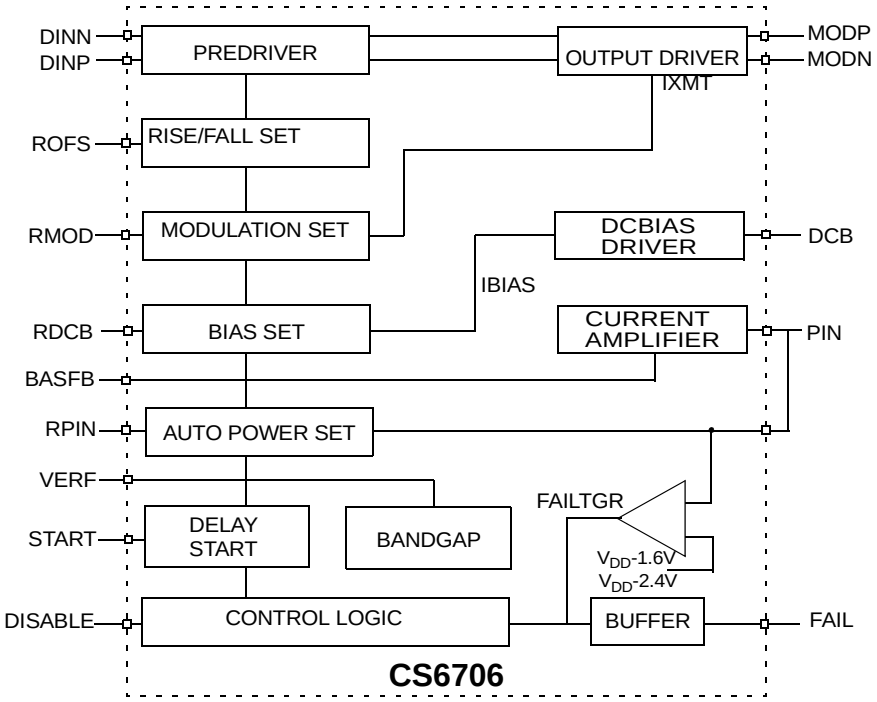
FEATURES

- Rise/fall time < 200ps, ideally suited for application up to 1.25Gbps.
- Independently programmable laser bias and modulation current: bias current to 60mA and modulation current to 45mA.
- Differential PECL inputs.
- Automatic laser power control with monitor circuit.
- Slow start and safety switch.
- Laser failure indication.
- Programmable rise/fall time.
- Supports both 3.3 and 5 Volt operation.
- Available as die or TSSOP-20 package.

APPLICATIONS

- FDDI
- Fiber Channel 100
- SONET OC-12/OC-24
- Fast Ethernet
- Gigabit Ethernet
- VCSEL Driver Transmitters

BLOCK DIAGRAM



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DIE CONNECTION DIAGRAM

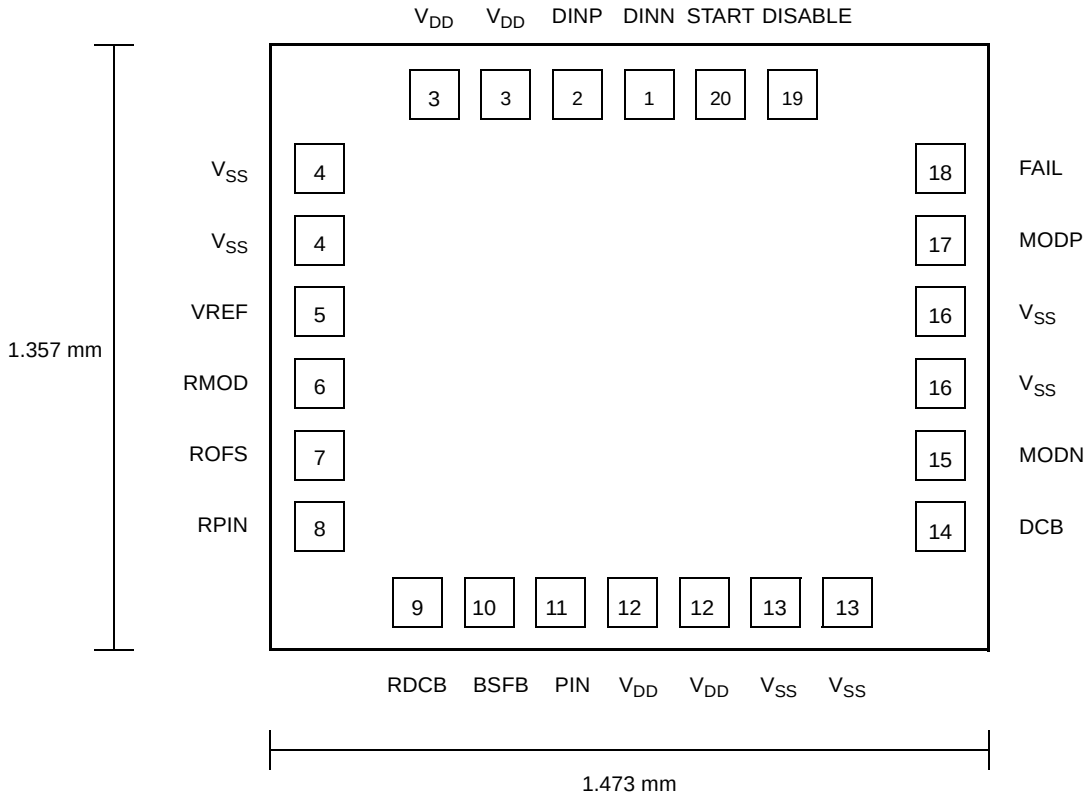


Figure-1

PIN CONNECTION DIAGRAM (TSSOP-20)

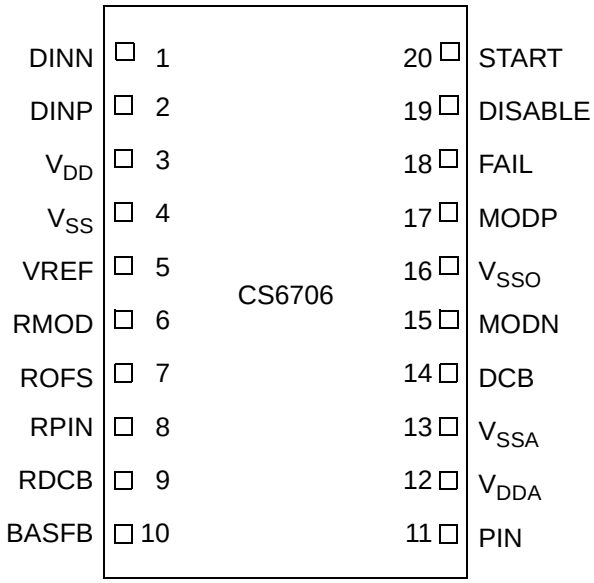


Figure-2 TSSOP-20

PIN DESCRIPTION

Name	Pin	Description
DINN	1	Inverse differential data input pin. AC-couple or direct couple to differential PECL source.
DINP	2	Differential data input pin. AC-couple or direct couple to differential PECL source.
V_{DD}	3	Input section power pin. Connect to most positive supply voltage.
V_{SS}	4	Input section ground pin. Connect to most negative supply voltage.
VREF	5	Reference voltage output pin (about 1.8V). Connect a capacitor between this pin and ground.
RMOD	6	Modulation current set point input pin. Connect a resistor between this pin and ground.
ROFS	7	Rise/fall time set point input pin. Connect a resistor between this pin and ground.
RPIN	8	Input pin for automatic power control circuit. Connect a resistor between this pin and ground.
RDCB	9	Bias current set point pin. Connect a resistor between this pin and ground.
BASFB	10	Bias current set point pin. Connect this pin to RDCB for automatic power control. Disconnecting BASFB and RDCB will disable the automatic power control function.
PIN	11	Monitor diode current control input pin. Connect a capacitor between this pin and ground.
V_{DDA}	12	Output section power pin. Connect to most positive supply voltage.
V_{SSA}	13	Output section ground pin. Connect to most negative supply voltage.
DCB	14	Laser DC bias current pin.
MODN	15	Inverse driver output stage pin. See application circuit schematic.
V_{SSO}	16	Output section ground pin. Connect to most negative supply voltage.
MODP	17	Driver output stage pin. See application circuit schematic.
FAIL	18	Laser failure indication pin.
DISABLE	19	Disable input pin (CMOS logic). Logic high to disable laser and modulation current. On-chip pull-down.
START	20	Slow start for laser drive pin. Connect a capacitor between this pin and ground.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
V_{CC}	Power supply (V_{CC} - Gnd)	6	V
T_a	Operating ambient temperature	-40 to +85	°C
T_{stg}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Rating	Unit
V_{CC}	Power supply (V_{CC} - Gnd)	3 to 5.5	V
T_a	Operating ambient temperature	-40 to +85	°C

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
Ibias	Range of programmable Laser bias current	-	-	60	mA
Imod	Range of programmable modulation current	-	-	45	mA
Vih	PECL input high	-	V_{CC} - 0.95	-	V
Vil	PECL input low	-	V_{CC} -1.75	-	V
I_{CC}	Supply current	-	Imod+Ibias +15	-	mA
Tr/Tf	Rise/fall time	-	200	-	ps

Product description

The CS6706 consists of a laser bias generator with automatic power control, a modulation current driver, and slow start and safety circuits which shut down laser drive current when a fault is detected.

Laser bias driver and APC

The laser power control function is realized by a feedback loop which sets the average photo-current of a monitor diode equal to the reference sink current at pin PIN. The precise value is controlled by a resistor, R_{pinset} which is connected between pin RPIN and ground.

Setting procedure to APC control loop

Two external resistors R_{pinset} and R_{dcb} should be set as following procedures.

(I). Find out desired photo-current (I_{pd}) generated from monitor diode and associated Bias current (I_{bias}) from I_{bias} V.S. I_{pd} curve. See **Figure 3**.

(II). Then R_{pinset} can be decided as $R_{pinset} = 1.06 / I_{pd}$.

(III). And R_{dcb} can be decided as $R_{dcb} = 1.06 / [(I_{bias}/214) - 130\mu A]$

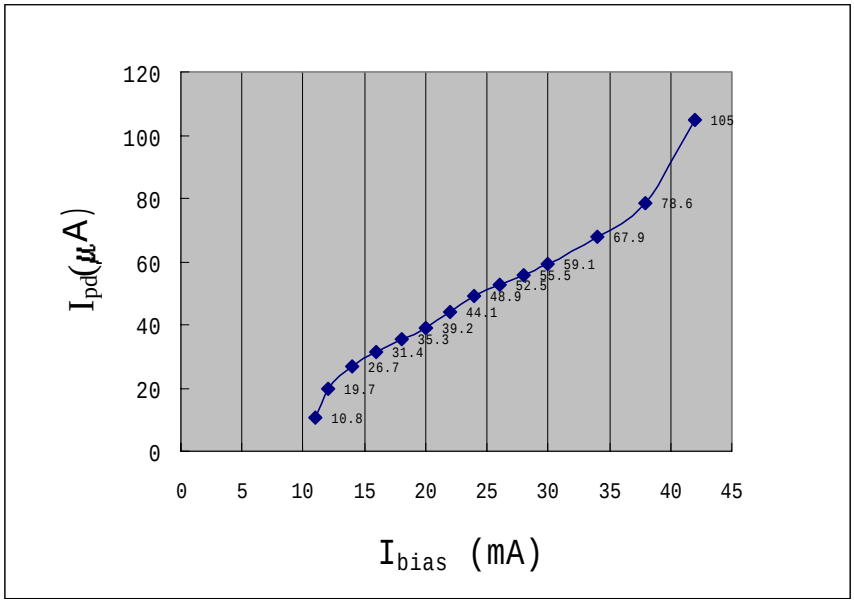


Figure-3 Example of I_{bias} V.S. I_{pd} curve

Setting without APC control loop

If the automatic power control function is not desired, for example in a VCSEL application, simply replace the monitor diode by a 18kΩ resistor and disconnect pin RDCB and pin BASFB (please refer to application circuit schematic). The laser bias current will be

$I_{bias} = 214 / R_{dcbset}$ (5V)

$I_{bias} = 210 / R_{dcbset}$ (3.3V)

Modulation Current driver

The modulation current is adjusted by a resistor R_{modset} which is connected between pin RMOD and ground.

I_{mod} = 408 / R_{modset} (5V)

I_{mod} = 394 / R_{modset} (3.3V)

Rise/fall time adjustment

The rise/fall time of the CS6706 can be adjusted by a resistor R_{ofsset} connected between pin ROFS and ground.

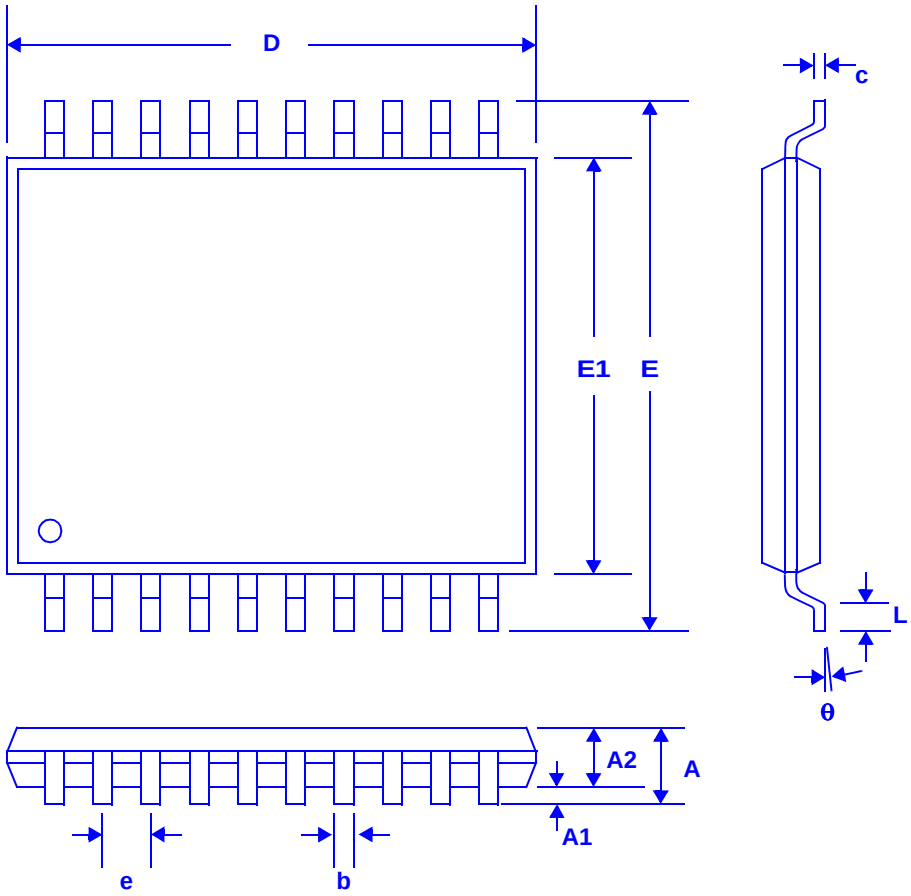
Safety circuits

Two window comparators are used to determine if the laser bias current is correct. If an abnormal condition is detected, the laser bias and modulation current will be shut down. In addition, the FAIL pin will output a logic high (CMOS level) indicating a laser bias error has occurred. This error condition can only be reset by powering the CS6706 off.

Slow Start

During power up, the voltage on pin START reaches the supply voltage in a time determined by a time constant set by an on-chip resistor (25kΩ) and an off-chip capacitor. Bias and modulation current can only begin when the voltage at the START pin exceeds $1/3V_{DD}$ and $2/3V_{DD}$ respectively.

PACKAGE OUTLINE (TSSOP-20)



Symbol	Dimensions in Millimeters			Dimensions in Inches		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.2	-	-	0.48
A1	0.05	-	0.15	0.002	-	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	-	0.30	0.007	-	0.012
c	0.09	-	0.20	0.004	-	0.008
D	6.40	6.50	6.60	0.252	0.256	0.260
E	-	6.40	-	-	0.252	-
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	-	0.65	-	-	0.026	-
L	0.45	0.60	0.75	0.018	-	0.030
θ	0°	-	8°	0°	-	8°

APPLICATION CIRCUIT SCHEMATIC

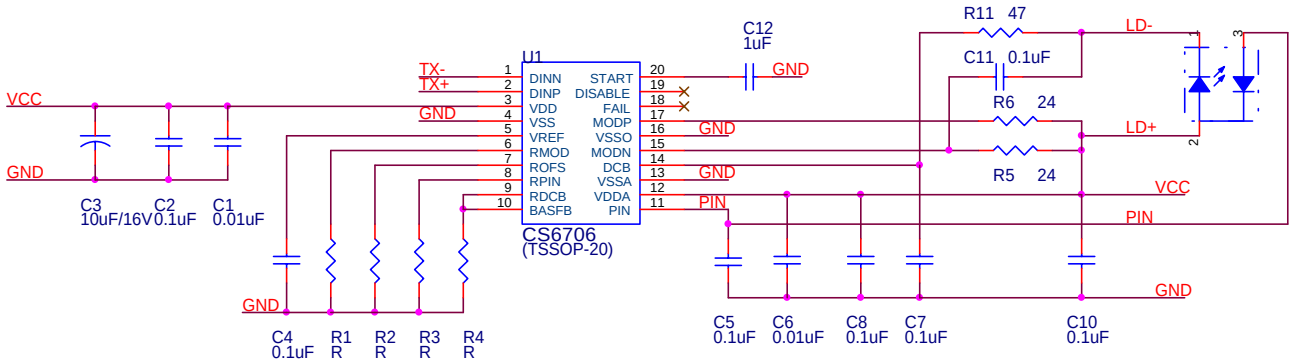


Figure-4 Using TSSOP-20 package