MC10E136, MC100E136

5V ECL 6-Bit Universal Up/Down Counter

The MC10E/100E136 is a 6-bit synchronous, presettable, cascadable universal counter. The device generates a look-ahead-carry output and accepts a look-ahead-carry input. These two features allow for the cascading of multiple E136's for wider bit width counters that operate at very nearly the same frequency as the stand alone counter.

The $\overline{\text{CLOUT}}$ output will pulse LOW for one clock cycle one count before the E136 reaches terminal count. The $\overline{\text{COUT}}$ output will pulse LOW for one clock cycle when the counter reaches terminal count. For more information on utilizing the look-ahead-carry features of the device please refer to the applications section of this data sheet. The differential COUT output facilitates the E136's use in programmable divider and self-stopping counter applications.

Unlike the H136 and other similar universal counter designs the E136 carry out and look-ahead-carry out signals are registered on chip.

This design alleviates the glitch problem seen on many counters where the carry out signals are merely gated. Because of this architecture there are some minor functional differences between the E136 and H136 counters. The user, regardless of familiarity with the H136, should read this data sheet carefully. Note specifically (see logic diagram) the operation of the carry out outputs and the look-ahead-carry in input when utilizing the master reset.

When left open all of the input pins will be pulled LOW via an input pulldown resistor. The master reset is an asynchronous signal which when asserted will force the Q outputs LOW.

The Q outputs need not be terminated for the E136 to function properly, in fact if these outputs will not be used in a system it is recommended to save power and minimize noise that they be left open. This practice will minimize switching noise which can reduce the maximum count frequency of the device or significantly reduce margins against other noise in the system.

The 100 Series contains temperature compensation.

- 550 MHz Count Frequency
- Fully Synchronous Up and Down Counting
- Look-Ahead-Carry Input and Output
- Asynchronous Master Reset
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 100 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 506 devices

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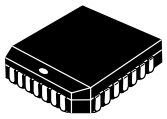
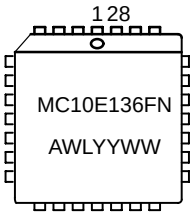
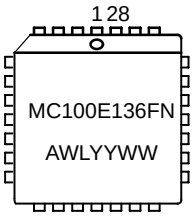
MARKING DIAGRAMS



PLCC–28
FN SUFFIX
CASE 776



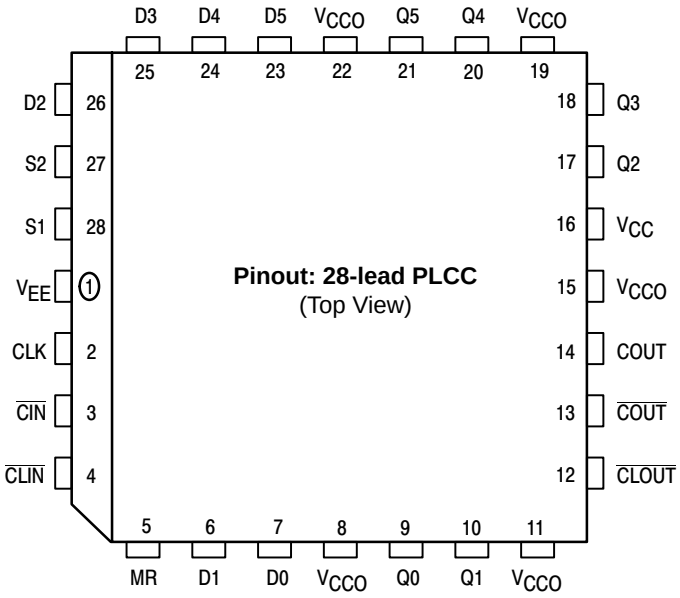


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E136FN	PLCC–28	37 Units/Rail
MC10E136FNR2	PLCC–28	500 Units/Reel
MC100E136FN	PLCC–28	37 Units/Rail
MC100E136FNR2	PLCC–28	500 Units/Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

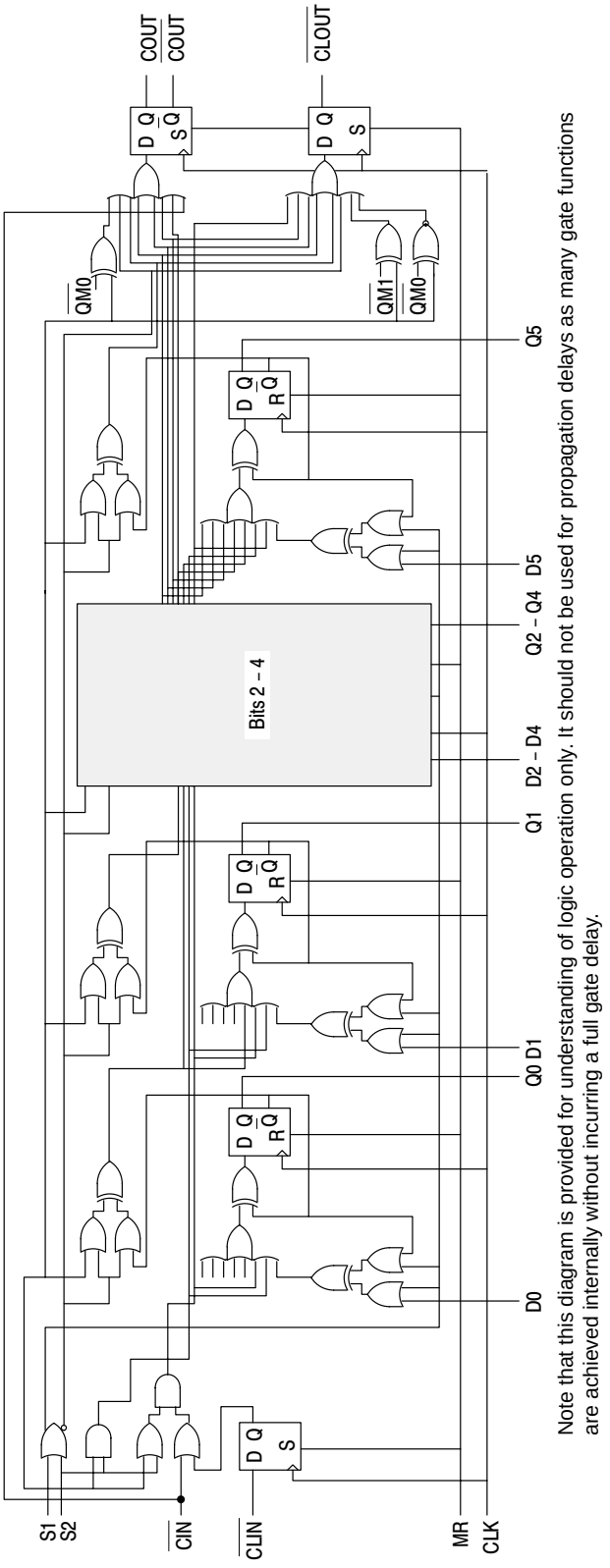
Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN NAMES

PIN	FUNCTION
$D_0 - D_5$	ECL Preset Data Inputs
$Q_0 - Q_5$	ECL Data Outputs
S1, S2	Mode Control Pins
MR	Master Reset
CLK	ECL Clock Input
$\overline{COUT}$, COUT	ECL Differential Carry-Out Output (Active LOW)
$\overline{CLOUT}$	ECL Look-Ahead-Carry Out (Active LOW)
$\overline{CIN}$	ECL Carry-In Input (Active LOW)
$\overline{CLIN}$	ECL Look-Ahead-Carry In Input (Active LOW)
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply

FUNCTION TABLE (Expanded truth table on page 5)

S1	S2	$\overline{CIN}$	MR	CLK	Function
L	L	X	L	Z	Preset Parallel Data
L	H	L	L	Z	Increment (Count Up)
L	H	H	L	Z	Hold Count
H	L	L	L	Z	Decrement (Count Down)
H	L	H	L	Z	Hold Count
H	H	X	L	Z	Hold Count
X	X	X	H	X	Reset (Qn = LOW)



Note that this diagram is provided for understanding of logic operation only. It should not be used for propagation delays as many gate functions are achieved internally without incurring a full gate delay.

E136 Universal Up/Down Counter Logic Diagram

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		125	150		125	150		125	150	mA
V_{OH}	Output HIGH Voltage (Note 2)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		125	150		125	150		125	150	mA
V_{OH}	Output HIGH Voltage (Note 2)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		125	150		125	150		140	170	mA
V_{OH}	Output HIGH Voltage (Note 2)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		125	150		125	150		140	170	mA
V_{OH}	Output HIGH Voltage (Note 2)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{COUNT}	Maximum Count Frequency	550	650	—	550	650	—	550	650	—	MHz
t_{PLH} t_{PHL}	Propagation Delay to Output										ps
	CLK to Q	850	1150	1450	850	1150	1450	850	1150	1450	
	MR to Q	850	1150	1450	850	1150	1450	850	1150	1450	
	CLK to $\overline{COUT}$	800	1150	1300	800	1150	1300	800	1150	1300	
	CLK to $\overline{CLOUT}$	825	1150	1400	825	1150	1400	825	1150	1400	
t_S	Setup Time										ps
	S1, S2	1000	650	—	1000	650	—	1000	650	—	
	D	800	400	—	800	400	—	800	400	—	
	$\overline{CLIN}$	150	0	—	150	0	—	150	0	—	
	$\overline{CIN}$	800	400	—	800	400	—	800	400	—	
t_h	Hold Time										ps
	S1, S2	150	–200	—	150	–200	—	150	–200	—	
	D	150	–250	—	150	–250	—	150	–250	—	
	$\overline{CLIN}$	300	0	—	300	0	—	300	0	—	
	$\overline{CIN}$	150	–250	—	150	–250	—	150	–250	—	
t_{RR}	Reset Recovery Time	1000	700	—	1000	700	—	1000	700	—	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_{PW}	Minimum Pulse Width										ps
	CLK, MR	700	400	—	700	400	—	700	400	—	
t_r t_f	Rise/Fall Times 20% - 80%										ps
	$\overline{COUT}$	275	—	600	275	—	600	275	—	600	
	Other	300	—	700	300	—	700	300	—	700	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.

EXPANDED TRUTH TABLE

Function	S1	S2	MR	$\overline{CIN}$	$\overline{CLIN}$	CLK	D5	D4	D3	D2	D1	D0	Q5	Q4	Q3	Q2	Q1	Q0	$\overline{COUT}$	$\overline{CLOUT}$
Preset	L	L	L	X	X	Z	L	L	L	L	H	H	L	L	L	L	H	H	H	H
Down	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	L
	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
	H	L	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	H	H
Preset	L	L	L	X	X	Z	H	H	H	H	L	L	H	H	H	H	L	L	H	H
Up	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	L	H	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	L	H	L
	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	L	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
Hold	H	H	L	X	X	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
	H	H	L	X	X	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
Down	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	L
Hold	H	L	L	H	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	H
Down	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
Hold	H	L	L	H	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
	H	L	L	H	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
	H	L	L	H	H	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
Hold	H	L	L	L	H	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
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Hold	H	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
Preset	L	L	L	X	X	Z	H	H	H	H	L	L	H	H	H	H	L	L	H	H
Up	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	L	H	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	L	H	L
Hold	L	H	L	H	L	Z	X	X	X	X	X	X	H	H	H	H	H	L	H	H
Up	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	L	H
Hold	L	H	L	H	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	H	H
	L	H	L	H	H	Z	X	X	X	X	X	X	H	H	H	H	H	H	H	H
Hold	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	L	H
Up	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	H	H	H	H
Reset	X	X	H	X	X	X	X	X	X	X	X	X	L	L	L	L	L	L	H	H

Z = Low to High Transition

APPLICATIONS INFORMATION

Overview

The MC10E/100E136 is a 6-bit synchronous, presettable, cascadable universal counter. Using the S1 and S2 control pins the user can select between preset, count up, count down and hold count. The master reset pin will reset the internal counter, and set the $\overline{\text{COUT}}$, $\overline{\text{CLOUT}}$, and $\overline{\text{CLIN}}$ flip-flops. Unlike previous 136 type counters the carry out outputs will go to a high state during the preset operation. In addition since the carry out outputs are registered they will not go low if terminal count is loaded into the register. The look-ahead-carry out output functions similarly.

Note from the schematic the use of the master information from the least significant bits for control of the two carry out functions. This architecture not only reduces the carry out delay, but is essential to incorporate the registered carry out functions. In addition to being faster, because these functions are registered the resulting carry out signals are stable and glitch free.

Cascading Multiple E136 Devices

Many applications require counters significantly larger than the 6 bits available with the E136. For these applications several E136 devices can be cascaded to increase the bit width of the counter to meet the needs of the application.

In the past cascading several 136 type universal counters necessarily impacted the maximum count frequency of the resulting counter chain. This performance impact was the result of the terminal count signal of the lower order counters having to ripple through the entire counter chain. As a result past counters of this type were not widely used in large bit counter applications.

An alternative counter architecture similar to the E016 binary counter was implemented to alleviate the need to ripple propagate the terminal count signal. Unfortunately these types of counters require external gating for cascading designs of more than two devices. In addition to requiring additional components, these external gates limit the cascaded count frequency to a value less than the free running count frequency of a single counter. Although there is a performance impact with this type of architecture it is minor compared to the impact of the ripple propagate designs. As a result the E016 type counters have been used extensively in applications requiring very high speed, wide bit width synchronous counters.

ON Semiconductor has incorporated several improvements to past universal counter designs in the E136 universal counter. These enhancements make the E136 the unparalleled leader in its class. With the addition of look-ahead-carry features on the terminal count signal, very large counter chains can be designed which function at very nearly the same clock frequency as a single free running device. More importantly these counter chains require no external gating. Figure 1 below illustrates the interconnect scheme for using the look-ahead-carry features of the E136 counter.

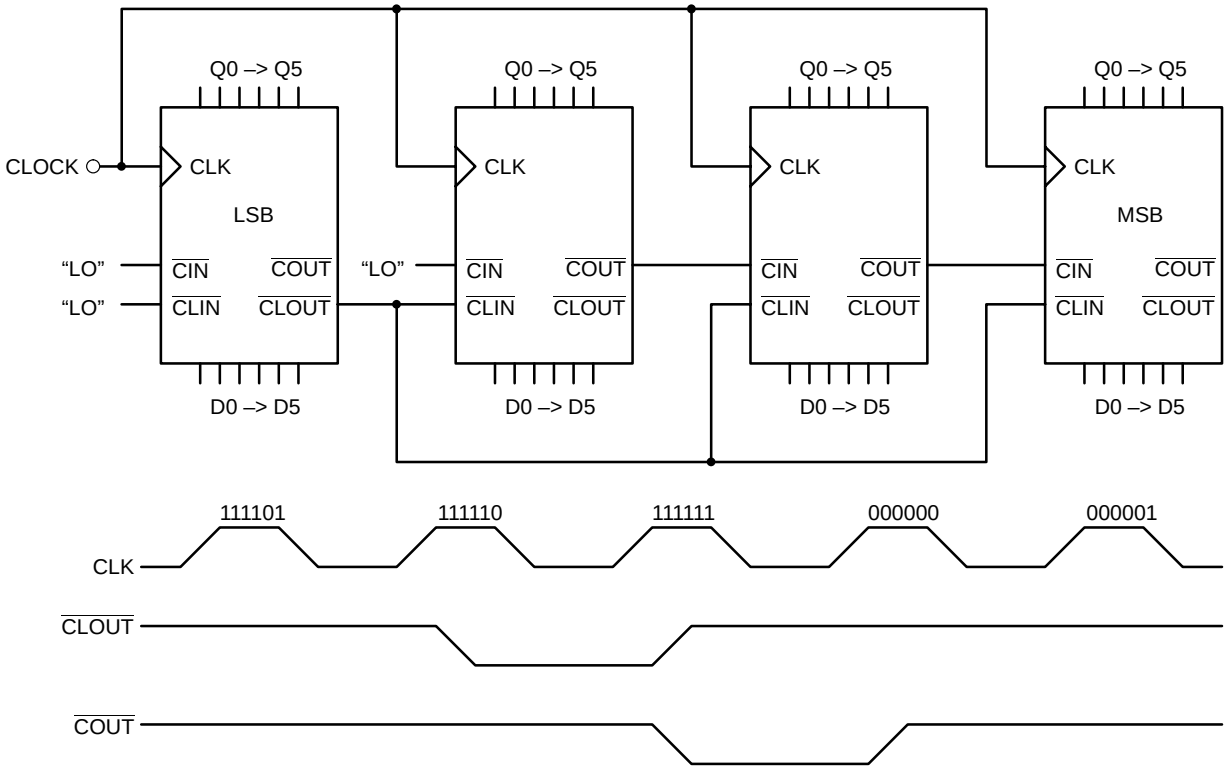

Figure 1. 24-bit Cascaded E136 Counter

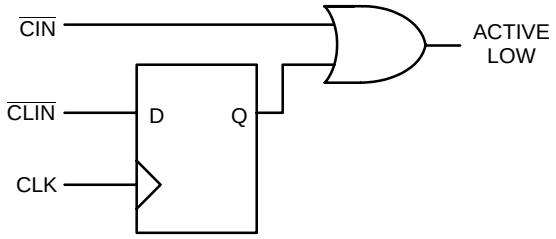

Figure 2. Look-Ahead-Carry Input Structure

Note from the waveforms that the look-ahead-carry output ($\overline{\text{CLOUT}}$) pulses low one clock pulse before the counter reaches terminal count. Also note that both $\overline{\text{CLOUT}}$ and the carry out pin ($\overline{\text{COUT}}$) of the device pulse low for only one clock period. The input structure for look-ahead-carry in ($\overline{\text{CLIN}}$) and carry in ($\overline{\text{CIN}}$) is pictured in Figure 2.

The $\overline{\text{CLIN}}$ input is registered and then ORed with the $\overline{\text{CIN}}$ input. From the truth table one can see that both the $\overline{\text{CIN}}$ and the $\overline{\text{CLIN}}$ inputs must be in a LOW state for the E136 to be enabled to count (either count up or count down). The $\overline{\text{CLIN}}$ inputs are driven by the $\overline{\text{CLOUT}}$ output of the lowest order E136 and therefore are only asserted for a single clock period. Since the $\overline{\text{CLIN}}$ input is registered it must be asserted one clock period prior to the $\overline{\text{CIN}}$ input.

If the counter previous to a given counter is at terminal count its $\overline{\text{COUT}}$ output and thus the $\overline{\text{CIN}}$ input of the given counter will be in the "LOW" state. This signals the given counter that it will need to count one upon the next terminal count of the least significant counter (LSC). The $\overline{\text{CLOUT}}$ output of the LSC will pulse low one clock period before it reaches terminal count. This $\overline{\text{CLOUT}}$ signal will be clocked into the $\overline{\text{CLIN}}$ input of the higher order counters on the following positive clock transition. Since both $\overline{\text{CIN}}$ and $\overline{\text{CLIN}}$ are in the LOW state the next clock pulse will cause the least significant counter to roll over and all higher order counters, if signaled by their $\overline{\text{CIN}}$ inputs, to count by one.

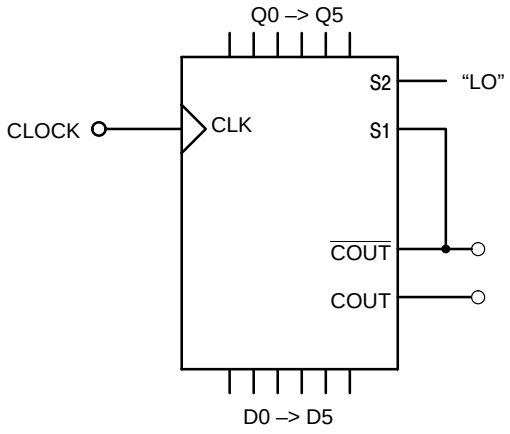

Figure 3. 6-bit Programmable Divider

During the clock pulse in which the higher order counter is counting by one the $\overline{\text{CLIN}}$ is clocking in the high signal presented by the $\overline{\text{CLOUT}}$ of the LSC. The $\overline{\text{CIN}}$'s in the higher order counter will ripple propagate through the chain to update the count status for the next occurrence of terminal count on the LSC. This ripple propagation will not affect the count frequency as it has 2^6–1 or 63 clock pulses to ripple through without affecting the count operation of the chain.

The only limiting factor which could reduce the count frequency of the chain as compared to a free running single device will be the setup time of the $\overline{\text{CLIN}}$ input. This limit will consist of the CLK to $\overline{\text{CLOUT}}$ delay of the E136 plus the $\overline{\text{CLIN}}$ setup time plus any path length differences between the $\overline{\text{CLOUT}}$ output and the clock.

Programmable Divider

Using external feedback of the $\overline{\text{COUT}}$ pin, the E136 can be configured as a programmable divider. Figure 3 illustrates the configuration for a 6-bit count down programmable divider. If for some reason a count up divider is preferred the $\overline{\text{COUT}}$ signal is simply fed back to S2 rather than S1. Examination of the truth table for the E136 shows that when both S1 and S2 are LOW the counter will parallel load on the next positive transition of the clock. If the S2 input is low and the S1 input is high the counter will be in the count down mode and will count towards an all zero state upon successive clock pulses. Knowing this and the operation of the $\overline{\text{COUT}}$ output it becomes a trivial matter to build programmable dividers.

For a programmable divider one wants to load a predesignated number into the counter and count to terminal count. Upon terminal count the counter should automatically reload the divide number. With the architecture shown in Figure 3 when the counter reaches terminal count the $\overline{\text{COUT}}$ output and thus the S1 input will go LOW, this combined with the low on S2 will cause the counter to load the inputs present on D0-D5. Upon loading the divide value into the counter $\overline{\text{COUT}}$ will go HIGH as the counter is no longer at terminal count thereby placing the counter back into the count mode.

Table 1. Preset Inputs Versus Divide Ratio

Divide Ratio	Preset Data Inputs					
	D5	D4	D3	D2	D1	D0
2	L	L	L	L	L	H
3	L	L	L	L	H	L
4	L	L	L	L	H	H
5	L	L	L	H	L	L
•	•	•	•	•	•	•
•	•	•	•	•	•	•
36	H	L	L	L	H	H
37	H	L	L	H	L	L
38	H	L	L	H	L	H
•	•	•	•	•	•	•
•	•	•	•	•	•	•
62	H	H	H	H	L	H
63	H	H	H	H	H	L
64	H	H	H	H	H	H

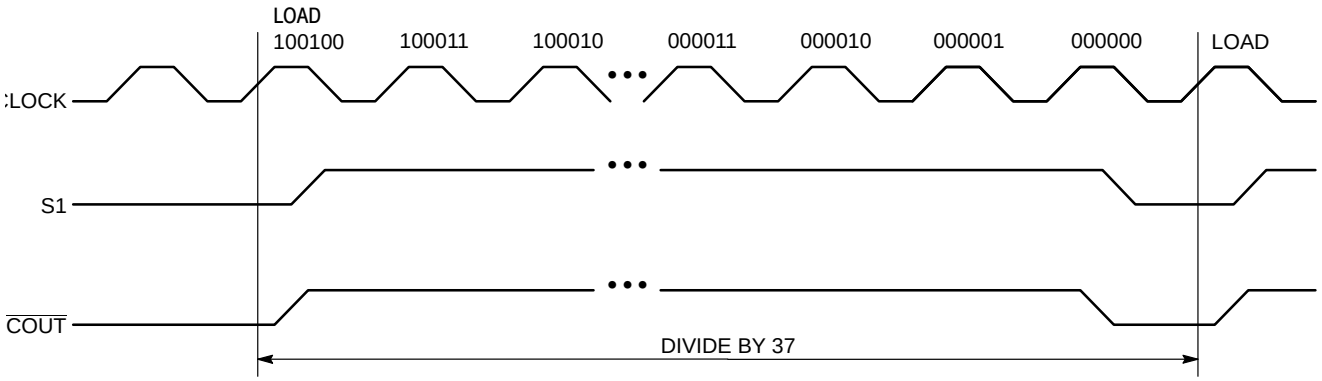

Figure 4. Programmable Divider Waveforms

The exercise of building a programmable divider then becomes simply determining what value to load into the counter to accomplish the desired division. Since the load operation requires a clock pulse, to divide by N, N–1 must be loaded into the counter. A single E136 device is capable of divide ratios of 2 to 64 inclusive, Table 1 outlines the load values for the various divide ratios. Figure 4 presents the waveforms resulting from a divide by 37 operation. Note that the availability of the COUT complimentary output $\overline{\text{COUT}}$ allows the user to choose the polarity of the divide by output.

For single device programmable counters the E016 counter is probably a better choice than the E136. The E016 has an internal feedback to control the reloading of the counter, this not only simplifies board design but also will result in a faster maximum count frequency.

For programmable dividers of larger than 8 bits the superiority of the E016 diminishes, and in fact for very wide dividers the E136 will provide the capability of a faster count frequency. This potential is a result of the cascading features mentioned previously in this document. Figure 5 shows the architecture of a 24-bit programmable divider implemented using E136 counters. Note the need for one external gate to control the loading of the entire counter chain. An ideal device for the external gating of this architecture would be the 4-input OR function in the 8-lead SOIC ECLinPS Lite™ family. However the final decision as to what device to use for the external gating requires a balancing of performance needs, cost and available board space. Note that because of the need for external gating the maximum count frequency of a given sized programmable divider will be less than that of a single cascaded counter.

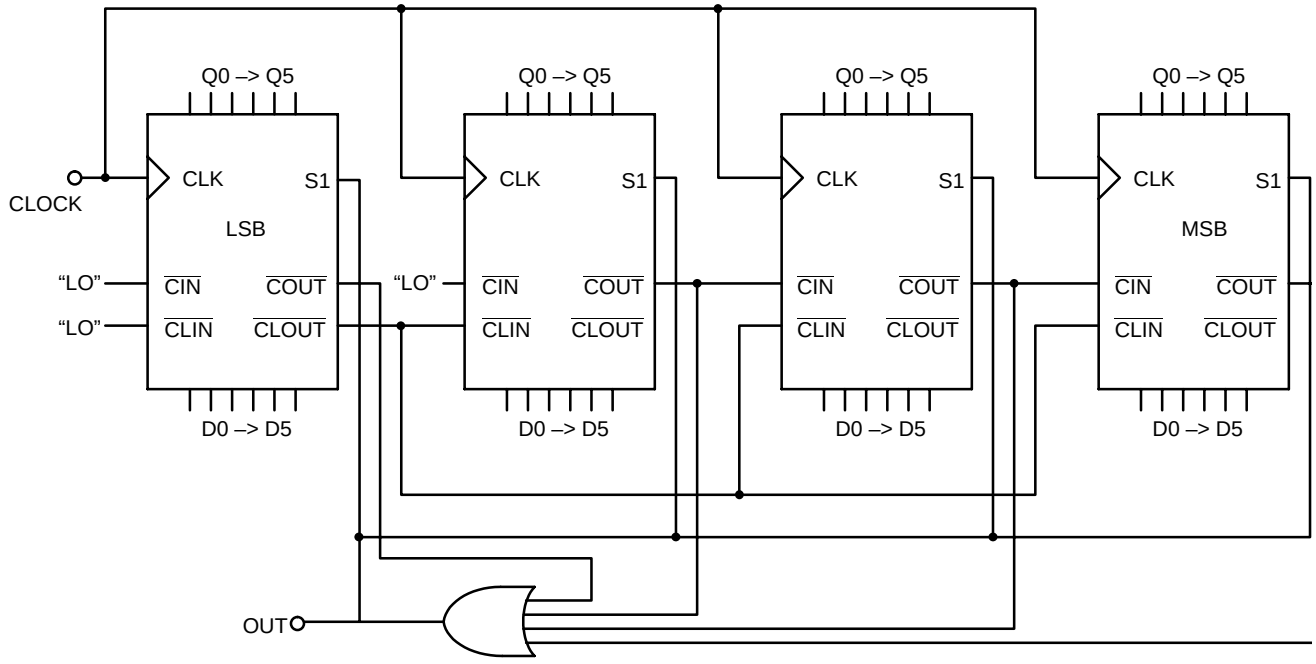

Figure 5. 24-bit Programmable Divider Architecture

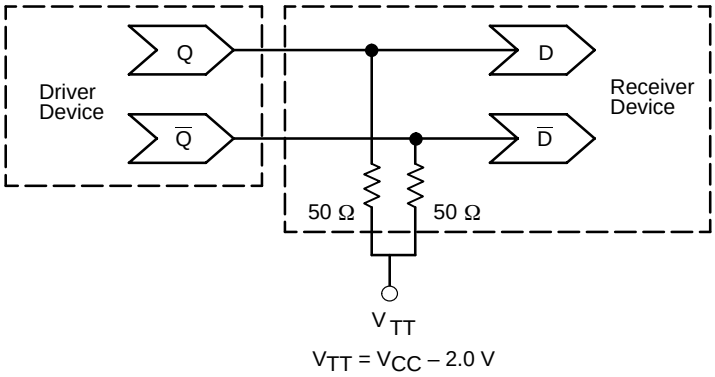

Figure 6. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

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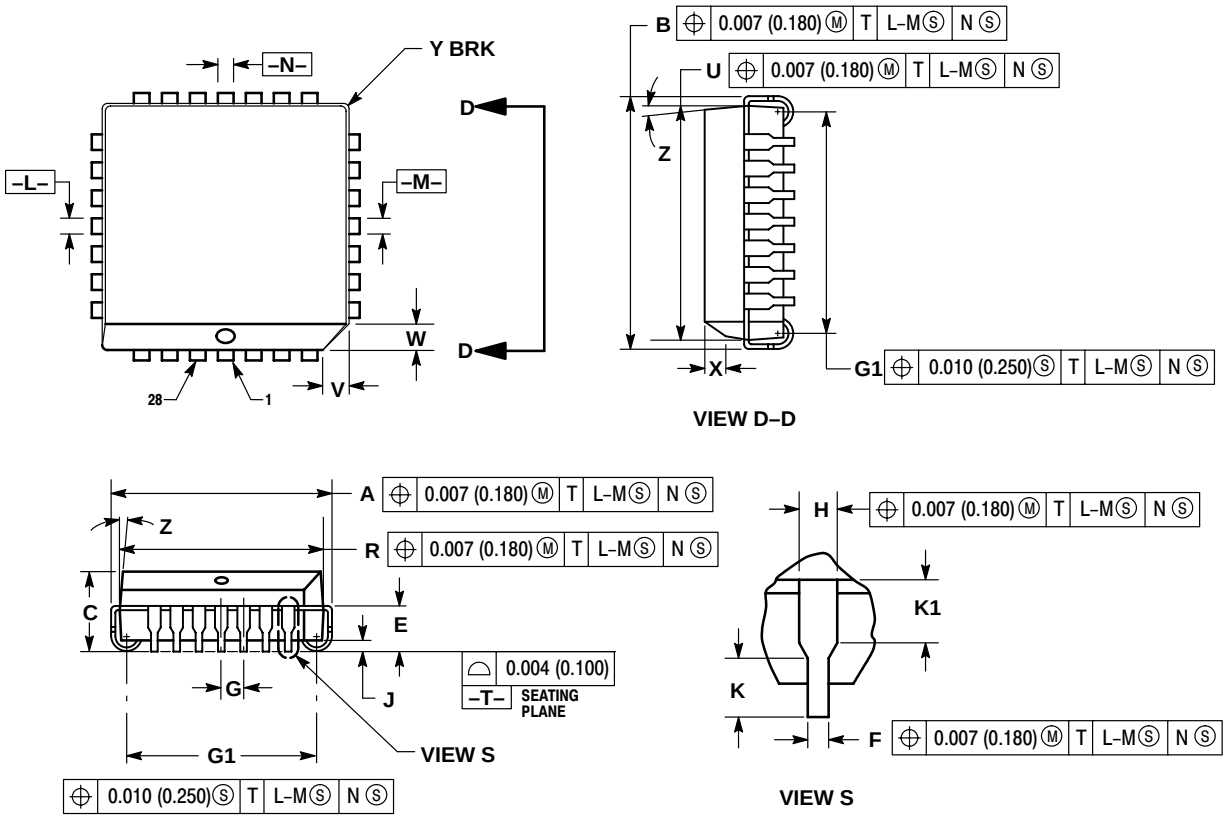

NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

Notes

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