OCTAL T1/E1 SHORT HAUL ANALOG FRONT END

IDT82V2048L

FEATURES

- Octal T1/E1 short haul analog front end which supports 100Ω T1 twisted pair, 120Ω E1 twisted pair and 75Ω E1 coaxial applications
- Built-in transmit pre-equalization meets G.703 & T1.102
- Digital/analog LOS detector meets ITU G.775, ETS 300 233 and T1.231
- ITU G.772 non-intrusive monitoring for in-service testing for any one of channel1 to channel7
- Low impedance transmit drivers with High-Z
- Selectable hardware and parallel/serial host interface
- Hitless Protection Switching (HPS) for 1 to 1 protection without relays
- JTAG boundary scan for board test
- 3.3V supply with 5V tolerant I/O
- Low power consumption
- Operating Temperature Range: -40°C to +85°C
- Available in 144-pin Thin Quad Flat Pack (TQFP_144_DA) and 160-pin Plastic Ball Grid Array (PBGA) packages

FUNCTIONAL BLOCK DIAGRAM

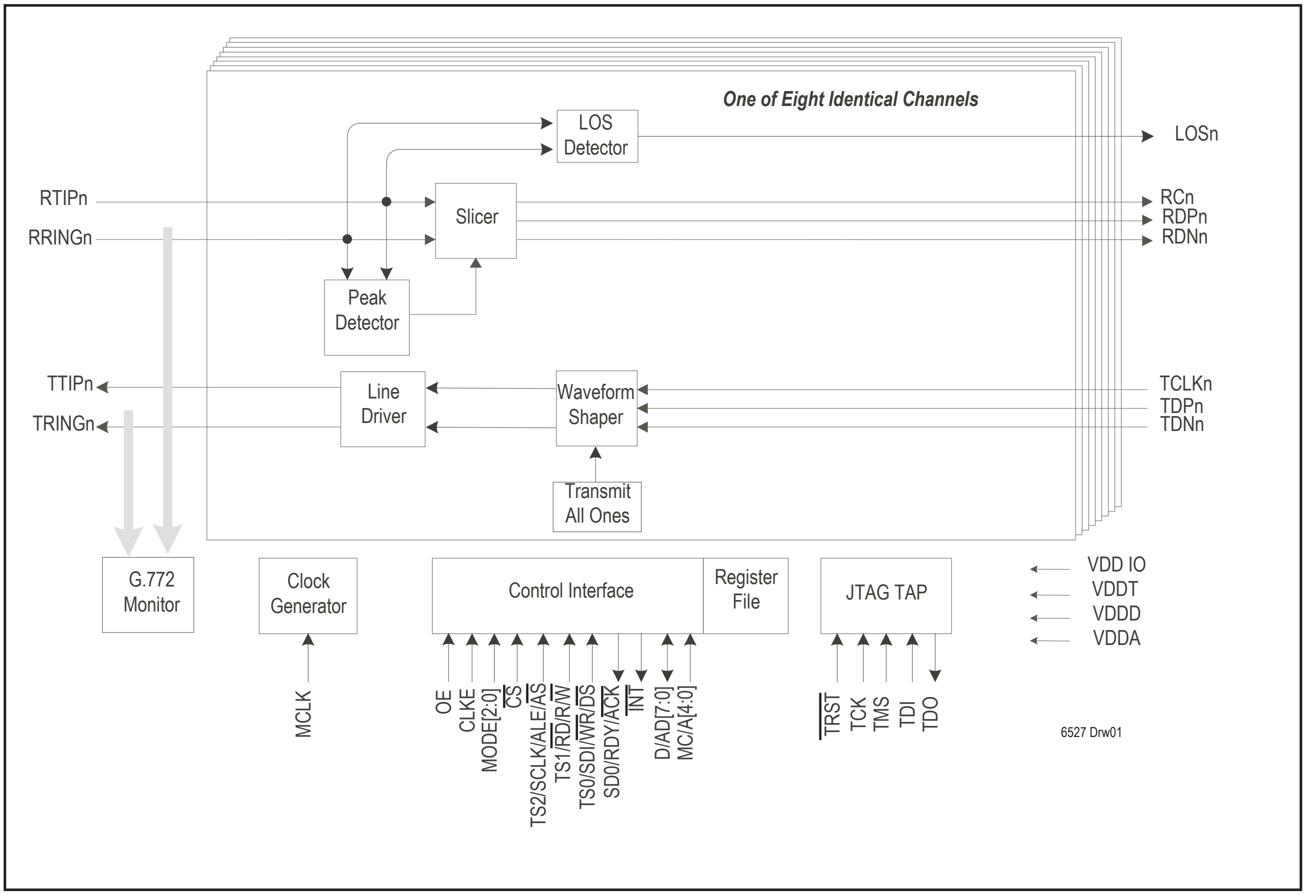


Figure - 1. Block Diagram

PIN CONFIGURATIONS

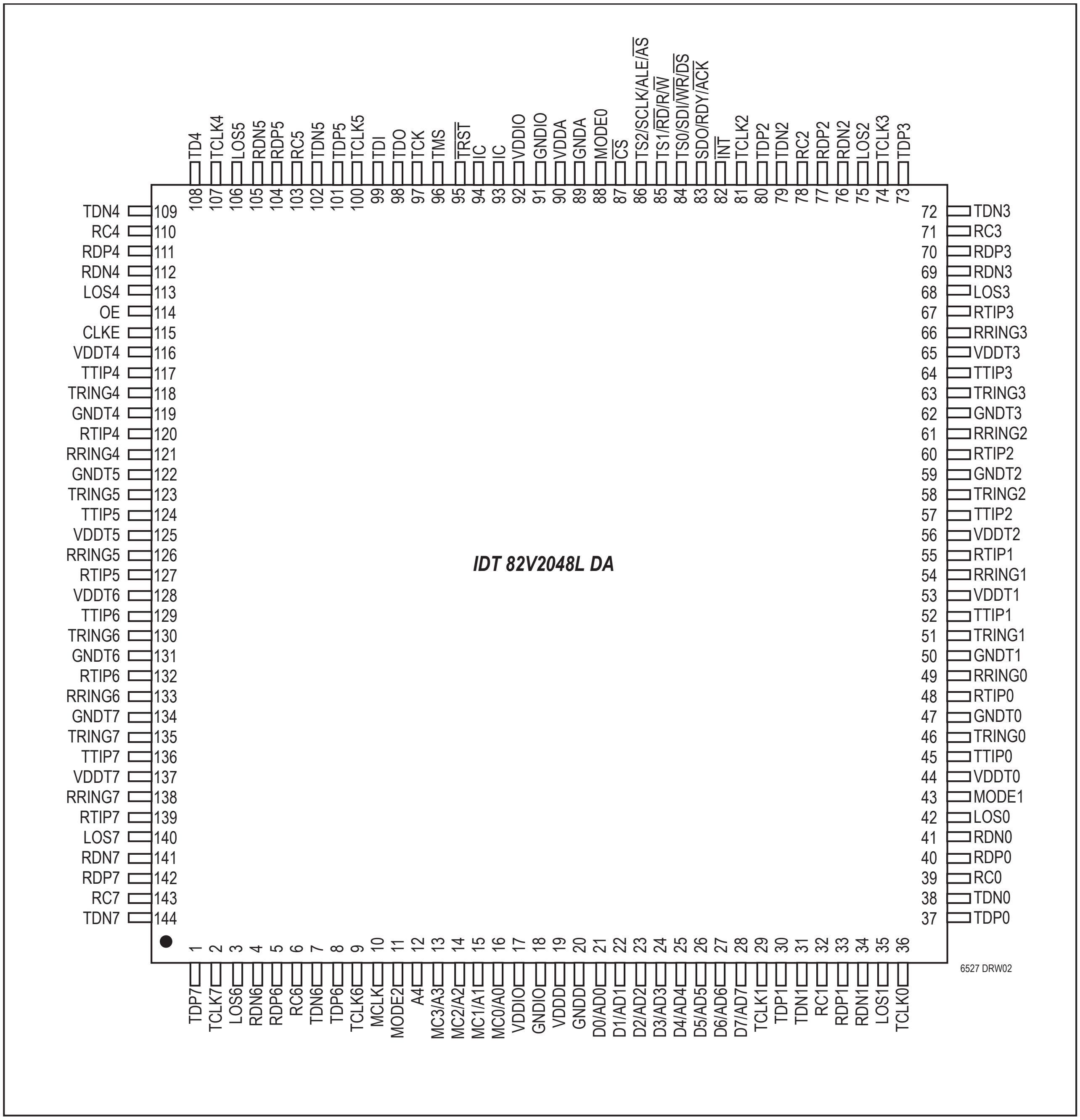
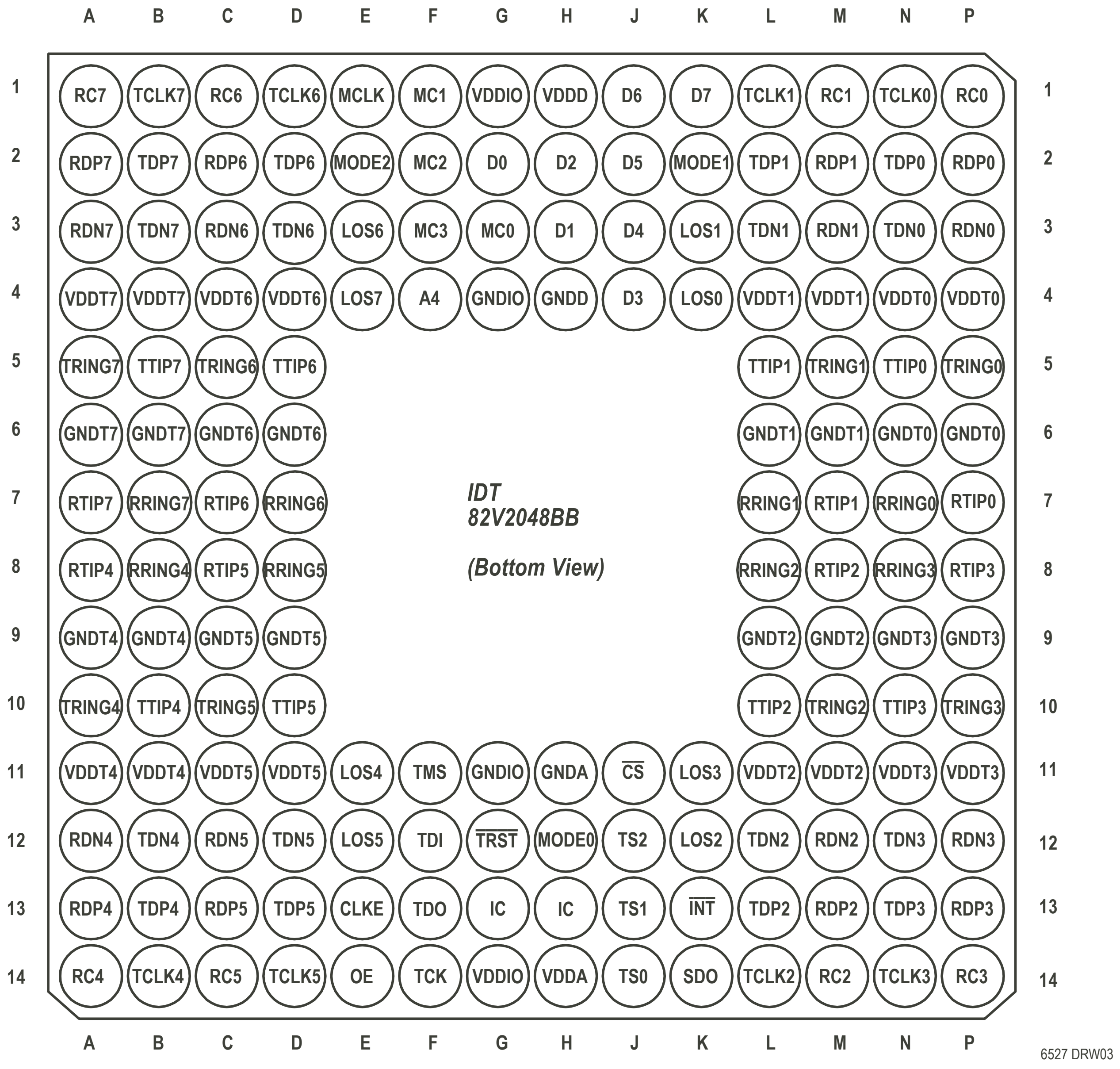


Figure - 2a. TQFP Package Pin Assignment

PIN CONFIGURATIONS (CONTINUED)



	A	B	C	D	E	F	G	H	J	K	L	M	N	P
1	RC7	TCLK7	RC6	TCLK6	MCLK	MC1	VDDIO	VDDD	D6	D7	TCLK1	RC1	TCLK0	RC0
2	RDP7	TDP7	RDP6	TDP6	MODE2	MC2	D0	D2	D5	MODE1	TDP1	RDP1	TDP0	RDP0
3	RDN7	TDN7	RDN6	TDN6	LOS6	MC3	MC0	D1	D4	LOS1	TDN1	RDN1	TDN0	RDN0
4	VDDT7	VDDT7	VDDT6	VDDT6	LOS7	A4	GNDIO	GNDD	D3	LOS0	VDDT1	VDDT1	VDDT0	VDDT0
5	TRING7	TTIP7	TRING6	TTIP6							TTIP1	TRING1	TTIP0	TRING0
6	GNDT7	GNDT7	GNDT6	GNDT6							GNDT1	GNDT1	GNDT0	GNDT0
7	RTIP7	RRING7	RTIP6	RRING6							RRING1	RTIP1	RRING0	RTIP0
8	RTIP4	RRING4	RTIP5	RRING5							RRING2	RTIP2	RRING3	RTIP3
9	GNDT4	GNDT4	GNDT5	GNDT5							GNDT2	GNDT2	GNDT3	GNDT3
10	TRING4	TTIP4	TRING5	TTIP5							TTIP2	TRING2	TTIP3	TRING3
11	VDDT4	VDDT4	VDDT5	VDDT5	LOS4	TMS	GNDIO	GNDA	$\overline{CS}$	LOS3	VDDT2	VDDT2	VDDT3	VDDT3
12	RDN4	TDN4	RDN5	TDN5	LOS5	TDI	$\overline{TRST}$	MODE0	TS2	LOS2	TDN2	RDN2	TDN3	RDN3
13	RDP4	TDP4	RDP5	TDP5	CLKE	TDO	IC	IC	TS1	$\overline{INT}$	TDP2	RDP2	TDP3	RDP3
14	RC4	TCLK4	RC5	TCLK5	OE	TCK	VDDIO	VDDA	TS0	SDO	TCLK2	RC2	TCLK3	RC3

Figure - 2b. PBGA160 Package Pin Assignment

PIN DESCRIPTION:

NAME	TYPE	PIN NO		DESCRIPTION
		QFP144	BGA160	
Transmit and Receive Line Interface				
TTIP0	Analog Output	45	N5	**TTIPn/TRINGn: Transmit Bipolar Tip/Ring for Channel 0-7** These pins are the differential line driver outputs. They will be in high impedance state if pin OE is low or the corresponding pin TCLKn is low (pin OE is globe control, while pin TCLKn is per-channel control). In host mode, each pin can be in high impedance state by programming a "1" to the corresponding bit in Register **OE**[1].
TTIP1		52	L5	
TTIP2		57	L10	
TTIP3		64	N10	
TTIP4		117	B10	
TTIP5		124	D10	
TTIP6		129	D5	
TTIP7		136	B5	
TRING0		46	P5	
TRING1		51	M5	
TRING2		58	M10	
TRING3		63	P10	
TRING4		118	A10	
TRING5		123	C10	
TRING6		130	C5	
TRING7		135	A5	
RTIP0	Analog Input	48	P7	**RTIPn/RRINGn: Receive Bipolar Tip/Ring for Channel 0-7** These pins are the differential line receiver inputs.
RTIP1		55	M7	
RTIP2		60	M8	
RTIP3		67	P8	
RTIP4		120	A8	
RTIP5		127	C8	
RTIP6		132	C7	
RTIP7		139	A7	
RRING0		49	N7	
RRING1		54	L7	
RRING2		61	L8	
RRING3		66	N8	
RRING4		121	B8	
RRING5		126	D8	
RRING6		133	D7	
RRING7		138	B7	

[1] Register name is indicated by bold capital letters. **OE**: Output Enable Register.

PIN DESCRIPTION (CONTINUED):

NAME	TYPE	PIN NO		DESCRIPTION
		QFP144	BGA160	
TDP0	I	37	N2	**TDPn/TDn: Positive/Negative Transmit Data for Channel 0-7** The NRZ data to be transmitted for positive /negative pulse is input on this pin. Data on TDPn/ TDNn are active high and sampled on failling edge of TCLKn.
TDP1		30	L2	
TDP2		80	L13	
TDP3		73	N13	
TDP4		108	B13	
TDP5		101	D13	
TDP6		8	D2	
TDP7		1	B2	
TDN0		38	N3	
TDN1		31	L3	
TDN2		79	L12	
TDN3		72	N12	
TDN4		109	B12	
TDN5		102	D12	
TDN6		7	D3	
TDN7		144	B3	
TCLK0	I	36	N1	**TCLKn: Transmit Clock for Channel 0-7** The clock of 1.544MHz (for T1 mode) or 2.048 MHz (for E1 mode) for transmit is input on this pin. The transmit data at TDPn or TDNn is sampled into the device on falling edge of TCLKn. Different combinations of TCLKn and MCLK result in different modes. It is summarized in section in Table 1 - System Interface Configuration.
TCLK1		29	L1	
TCLK2		81	L14	
TCLK3		74	N14	
TCLK4		107	B14	
TCLK5		100	D14	
TCLK6		9	D1	
TCLK7		2	B1	

TDPn	TDNn	Output Pulse
0	0	Space
0	1	Negative Pulse
1	0	Postivie Pulse
1	1	Space

PIN DESCRIPTION (CONTINUED):

NAME	TYPE	PIN NO		DESCRIPTION
		QFP144	BGA160	
RDP0	O	40	P2	**RDPn/RDn: Positive/Negative Receive Data for Channel 0-7** These pins output the raw RZ sliced data. The active polarity of RDPn/RDNn is determined by pin CLKE. When pin CLK is Low, RDPn/RDNn is active low. When pin CLKE is High, RPDn/RDNn is active high. RDPn/RDNn will remain active during LOS. RDPn/RDNn is set into high impedance when the corresponding receiver is power down.
RDP1		33	M2	
RDP2	High-Z	77	M13	
RDP3		70	P13	
RDP4		111	A13	
RDP5		104	C13	
RDP6		5	C2	
RDP7		142	A2	
RDN0		41	P3	
RDN1		34	M3	
RDN2		76	M12	
RDN3		69	P12	
RDN4		112	A12	
RDN5		105	C12	
RDN6		4	C3	
RDN7		141	A3	
RC0	O	39	P1	**RCn: Recieve Pulse for Channel 0-7** In data recovery mode, RCn is the output of an internal exclusive OR (XOR) which is connected with RDPn and RDNn. The clock is recovered from the signal on RCn externally. If receiver n is power down, the corresponding RCn is in high impedance.
RC1		32	M1	
RC2	High-Z	78	M14	
RC3		71	P14	
RC4		110	A14	
RC5		103	C14	
RC6		6	C1	
RC7		143	A1	
MCLK	I	10	E1	**MCLK: Master Clock** This is the idependent, free running reference dock. A clock of 1.544 MHz (for T1 mode) or 2.048 MHz (for E1 mode) is supplied to this pin as the clock reference of the device for normal operation. When MCLK is low, all the receivers are power down, and the output pins RCn, RDPn, and RDNn are switched to high impedance. In transmit path, the operation mode is decided by the combination of MCLK and TCLKn (it is summarized in Table 1 - System Interface Configuration). Note that wait state generation via RDY/$\overline{\text{ACK}}$ is not available if MCLK is not provided.
LOS0	O	42	K4	**LOSn: Loss of Signal Output for Channel 0-7** A high level on this pin indicates the loss of signal when there is not transition over a specific period of time and not enough ones desity in the received signal. The transition will return to low automatically when there is enough transition over a specific period of time with a certain ones desity in the received signal. The LOS assertion and desertion criteria are described in the ***Functional Description.***
LOS1		35	K3	
LOS2		75	K12	
LOS3		68	K11	
LOS4		113	E11	
LOS5		106	E12	
LOS6		3	E13	
LOS7		140	E4	

PIN DESCRIPTION (CONTINUED):

<table>
<tr><th rowspan="2">NAME</th><th rowspan="2">TYPE</th><th colspan="2">PIN NO</th><th rowspan="2">DESCRIPTION</th></tr>
<tr><th>QFP144</th><th>BGA160</th></tr>
<tr><td></td><td colspan="4">**Hardware/Host Control Mode**</td></tr>
<tr><td>MODE2</td><td>I
(Pulled to VDDIO / 2)</td><td>11</td><td>E2</td><td>**MODE2: Control Mode Select 2** (1)
This signal on this pin determines which control mode is selected to control the device:
<table>
<tr><th>MODE 2</th><th>Control Interface</th></tr>
<tr><td>Low</td><td>Control by Hardware mode</td></tr>
<tr><td>VDDIO/2</td><td>Control by Serial Host Interface</td></tr>
<tr><td>High</td><td>Control by Parallel Host Interface</td></tr>
</table>
Hardware control pins include MODE[2:0], TS[2:0], CLKE and OE. Serial host interface pins include CS, SCLK, SDI, SDO, and INT and Parallel host interface pins include CS, A[4:0], D[7:0], WR/DS, RD/RW, ALE/AS, INT and RDY/ACK. The device supports multiple parallel host interace as follows (refer to MODE1 and MODE0 pin description below for details):
<table>
<tr><th>MODE [2:0]</th><th>Host Interface</th></tr>
<tr><td>100</td><td>Non-multiplexed Motorola mode interface</td></tr>
<tr><td>101</td><td>Non-multiplexed Intel mode interface</td></tr>
<tr><td>110</td><td>Multiplexed Motorola mode interface</td></tr>
<tr><td>111</td><td>Multiplexed Intel mode interface</td></tr>
</table></td></tr>
<tr><td>MODE1</td><td>I</td><td>43</td><td>K2</td><td>**MODE1: Control Mode Select 1**(1)
In parallel host mode, the parallel interface operates with separate address bus and data bus when this pin is Low, and operates with multiplexed address and data bus when this pin is High. In serial host mode or hardware mode, this pin should be grounded.</td></tr>
<tr><td>MODE0</td><td>I</td><td>88</td><td>H12</td><td>**MODE0: Control Mode Select** (1)
In host mode, the parallel host interface is configured for Motorola compatible hosts when this pin is Low, or for Intel compatible hosts when this pin is High.
In serial host mode or hardware mode, this pin should be grounded.</td></tr>
<tr><td>$\overline{CS}$</td><td>I
(Pulled to VDDIO / 2)</td><td>87</td><td>J11</td><td>**$\overline{CS}$: Chip Select (Active Low)**
In host mode, this pin is asserted low by the host to enable host interface. A transition from High to Low must occur on this pin for each Read/Write operation and the level must not return to High until the operation is over.
In hardware control mode, this pin should be pulled to VDDIO/2.</td></tr>
</table>

NOTE:

1. In host mode operation, Extended register e-AFE has to be set to FF H for proper device operation. See Extended Register Description for details.

PIN DESCRIPTION (CONTINUED):

NAME	TYPE	PIN NO		DESCRIPTION
		QFP144	BGA160	
TS2/ SCLK/ ALE/$\overline{AS}$	I	86	J12	**TS2: Template Select 2** In hardware control mode, the signal on this pin is the most significant bit for the transmit template select. Refer to ***Transmit Template*** of the ***Functional Description*** for details. **SCLK: Shift Clock** In serial host mode, the signal on this pin is the shift clock for the serial interface. Data on pin SDO is clocked out on falling edges of SCLK if pin CLKE is Low, or on rising edge of SCLK if pin CLKE is High. Data on pin SDI is always sampled on rising edges of SCLK. **ALE: Address Latch Enable** In parallel Intel multiplexed host mode, the address on AD[4:0] is sampled into the device on falling edges of ALE (signals on AD[7:5] are ignored). in non-multiplexed host mode, ALE should be pulled High. **$\overline{AS}$: Address Strobe (Active Low)** In parallel Motorola multiplexed host mode, the address on AD[4:0] is latched into the device on fallind edges of $\overline{AS}$ (signals on AD[7:5] are ignored). In non-multiplexed host mode, $\overline{AS}$ should be pulled High.
TS1/$\overline{RD}$/ R/$\overline{W}$	I	85	J13	**TS1: Template Select 1** In hardware control mode, the signal on this pin is the second most significant bit for the transmit template select. Refer to Transmit Template of Functional Description for details. **$\overline{RD}$: Read Strobe (Active Low)** In parallel Intel multiplexed or non-multiplexed host mode, this pin is active for read operation. **R/$\overline{W}$: Read/Write Select** In parallel Motorola multiplexed host mode, the pin is active low for write operation and high for read operation.
TS0/ SDI/$\overline{WR}$/ $\overline{DS}$	I	84	J14	**TS0: Template Select 0** In hardware control mode, the signal on this pin is the least significant bit for the transmit template select. Refer to ***Transmit Template*** of ***Functional Description*** for detail. **SDI: Serial Data Input** In serial host mode, this pin input the data to the serial interface. Data on this pin is sampled on rising edges of SCLK. **$\overline{WR}$: Write Strobe (Active Low)** In parallel Intel host mode, this pin is is active low during write operation. The data on D[7:0] (in non-multiplexed mode) or A[7:0] (in multiplexed mode) is sampled into the device on rising edges of $\overline{WR}$. **$\overline{DS}$: Data Strobe (Active Low)** In parallel Motorola host mode, this pin is active low. During a write operation (R/$\overline{W}$ = 0), the data on D[7:0] (in non-multiplexed mode) or AD[7:0] (in multiplexed mode) is sampled into the device on rising edges of $\overline{DS}$. During a read operatoin (R/$\overline{W}$ = 1), the data is driven to D[7:0] (in non-multipled mode) or AD[7:0} (in multiplexed mode) by the device on rising edges of $\overline{DS}$. In parallel Motorola non-multiplexed host mode, the address information on the 5 bits of address bus A[4:0] are latched into the device on the falling edge of $\overline{DS}$.

PIN DESCRIPTION (CONTINUED):

NAME	TYPE	PIN NO		DESCRIPTION
		QFP144	BGA160	
SDO/ RDY/ $\overline{\text{ACK}}$	O	83	K14	**SDO: Serial Data Output** In serial host mode, the data is output on this pin. In serial write operation , SDO is always in High impedance. In serial read operation, SDO is in High impedance only when SDI is in address/command byte. Data on pin SDO is clocked out of the device on falling edges of SCLK in pin CLKE is Low, or on rising edges of SCLK if pin CLKE is High. **RDY: Ready Output** In parallel Intel host mode, the high level of this pin reports to the host that bus cycle can be completed, while low reports the host must insert wait status. **$\overline{\text{ACK}}$: Acknowledge Output (Active Low)** In parallel Motorola host mode, the low level of this pin indicates that valid information on the data bus is ready for a read operation or acknowledges the acceptance of the written data during a write operation.
$\overline{\text{INT}}$	O Open Drain	82	K13	**$\overline{\text{INT}}$: Interrupt (Active Low)** This in the open drain, active low interrupt output. Four sources may cause the interrupt (refer to ***Interrupt Handling*** of ***Functional Description*** for details).
D7/AD7	I/O	28	K1	**Dn: Data Bus 7-0** In non-multiplexed host mode, these pins are the bi-directional data bus. **ADn: Address/Data Bus 7-0** In multiplexed host mode, these pins are in multiplexed bi-directional address/data bus. In hardware mode, these pins should be tied to VDDIO/2. In serial host mode, these pins should be grounded.
D6/AD6		27	J1	
D5/AD5		26	J2	
D4/AD4	High-Z	25	J3	
D3/AD3		24	J4	
D2/AD2		23	H2	
D1/AD1		22	H3	
D0/AD0		21	G2	

PIN DESCRIPTION (CONTINUED):

<table>
<tr><th rowspan="2">NAME</th><th rowspan="2">TYPE</th><th colspan="2">PIN NO</th><th rowspan="2">DESCRIPTION</th></tr>
<tr><th>QFP144</th><th>BGA160</th></tr>
<tr><td>A4
MC3/A3
MC2/A2
MC1/A1
MC0/A0</td><td>I</td><td>12
13
14
15
16</td><td>F4
F3
F2
F1
G3</td><td>MCn: Performance Monitor Configuration 4-0
In hardware control mode, A4 must be connected to GND, MC[3:0] are used to select one transmitter or receiver of the channel 1 to 7 for non-intrusive monitoring. Channel 0 is used as the monitoring channel. If a transmitter is monitored, signals on the corresponding pins TTIPn and TRINGn are internally transmitted to RTIPn and RRINGn are internally transmitted to RTIP0 and RRING0. The clock and data recovery circuit in receiver 0 can then output the monitored clock pin RC0 as well as the monitored data to RDP0 and RDN0 pins. The signals monitored by channel 0 can be routed to TTIP0/RING0 by activating the remote loopback in this channel. Performance Monitor Configuration determines by MC[3:] is shown below. Note that if MC[2:0] = 000, the device is in normal operation of all the channels.
<table>
<tr><th>MC[3:]</th><th>Monitoring Configuration</th></tr>
<tr><td>0000</td><td>Normal operation without monitoring</td></tr>
<tr><td>0001</td><td>Monitoring receiver 1</td></tr>
<tr><td>0010</td><td>Monitoring receiver 2</td></tr>
<tr><td>0011</td><td>Monitoring receiver 3</td></tr>
<tr><td>0100</td><td>Monitoring receiver 4</td></tr>
<tr><td>0101</td><td>Monitoring receiver 5</td></tr>
<tr><td>0110</td><td>Monitoring receiver 6</td></tr>
<tr><td>0111</td><td>Monitoring receiver 7</td></tr>
<tr><td>1000</td><td>Normal operation without monitoring</td></tr>
<tr><td>1001</td><td>Monitoring transmitter 1</td></tr>
<tr><td>1010</td><td>Monitoring transmitter 2</td></tr>
<tr><td>1011</td><td>Monitoring transmitter 3</td></tr>
<tr><td>1100</td><td>Monitoring transmitter 4</td></tr>
<tr><td>1101</td><td>Monitoring transmitter 5</td></tr>
<tr><td>1110</td><td>Monitoring transmitter 6</td></tr>
<tr><td>1111</td><td>Montioring transmitter 7</td></tr>
</table>
An: Address Bus 4-0
When pin MODE1 is low, the parallel host interface operates with separate address and data bus. In this mode, the signal on this pin is the address bus of the host interface.</td></tr>
<tr><td>OE</td><td>I</td><td>114</td><td>E14</td><td>OE: Output Driver Enable
Pulling this pin to low can make all driver output into high impedance state immediately for redundacy application without external mechanical relays. In this condition, all the other internal circuits remain active.</td></tr>
<tr><td>CLKE</td><td>I</td><td>115</td><td>E113</td><td>CLKE: Clock Edge Select
The signal on this pin determines the active edge of RCn, RDPn, RDNn and SCLK (refer to <i>Functional Description</i> and <i>Table 2</i>).</td></tr>
</table>

PIN DESCRIPTION (CONTINUED):

NAME	TYPE	PIN NO		DESCRIPTION
		QFP144	BGA160	
$\overline{\text{TRST}}$	I Pullup	95	G12	**$\overline{\text{TRST}}$: JTAG Test Port Reset (Active Low)** This is the active low asynchronous reset to the JTAG Test Port. This pin has an internal pullup resistor and it can be left disconnected.
TMS	I Pullup	96	F11	**TMS: JTAG Test Mode Select** This signal on this pin controls the JTAG test performance and is clocked into the device on rising edges of TCK. This pin has an internal pullup resister and it can be left disconnected.
TCK	I High-Z	97	F14	**TCK: JTAG Test Clock** This pin input the clock of the JTAG Test. The data on TDI and TMS are clocked into the device on rising edges of TCK. TDO is a High-Z output signal. It is active only when scanning of data is out.
TDI	I Pullup	99	F12	**TDI: JTAG Test Data Input** This pin input the serial data of the JTAG Test. The data on the TDI is clocked into the device on rising edges of TCK. This pin has an internal pullup and it can be left disconnected.
IC	-	93	G13	**IC: Internal Connected** (Leave it open for normal operation).
IC	-	94	H13	**IC: Internal Connected** (Leave it open for normal operation).
				Supplies and Grounds
VDDIO	-	17	G1 G14	**3.3V I/O Power Supply**
GNDIO	-	18 91	G4 G11	**I/O Ground**
VDDT0	-	44	N4,P4	**3.3V / 5V Power Supply for Transmitter Driver**
VDDT1		53	L4,M4	
VDDT2		56	L11,M11	
VDDT3		65	N11,P11	
VDDT4		116	A11,B11	
VDDT5		125	C11,D11	
VDDT6		128	C4,D4	
VDDT7		137	A4,B4	
GNDT0	-	47	N6,P6	**Analog GND for Transmitter Driver**
GNDT1		50	L6,M6	
GNDT2		59	L9,M9	
GNDT3		62	N9,P9	
GNDT4		119	A9,B9	
GNDT5		122	C9,D9	
GNDT6		131	C6,D6	
GNDT7		134	A6,B6	
VDD0	-	19	H1	**3.3V Digital / Analog Core Power Supply**
VDDA		90	H14	
GND0	-	20	H4	**Digital / Analog Core GND**
GNDA		89	H1	

FUNCTIONAL DESCRIPTION

OVERVIEW

The IDT82V2048L is a fully integrated octal short-haul analog front end (AFE), which contains eight transmit and receive channels for use in either E1 or T1 applications. The raw sliced data (no retiming) can be output to the system. Transmit equalization is implemented with low-impedance output drivers that provide shaped waveforms to the transformer, guaranteeing template conformance. Moreover, testing fuctions, such as JTAG boundary scan is provided. The device is optimized for flexible software control through a serial or parallel host mode interface. Hardware control is also available. Figure 1 shows One of the Eight Identical Channels operation.

T1/E1 MODE SELECTION

T1/E1 mode selection configures the device globally. In Hardware Mode, the template selection pins: TS2, TS1 and TS0 determine whether the operation mode is T1 or E1 (refer to Table 4). In software Mode, the Transmit Template Select Register (Primary Register: 11Hex) determines whether the operation mode is T1 or E1.

SYSTEM INTERFACE

The system interface of each channel operates in Dual Rail Mode with data recovery, that is with raw data slicing only and without clock recovery.

The Dual Rail interface consist of TDPn, TDNn, TCLKn, RDPn, RDNn and RCn. Data transmitted from TDPn and TDNn appears on TTIPn and TRINGn at the line interface. The interface of the AFE is shown in *Figure 3*. Pin RDPn and RDNn, in the condition, are raw RZ slice output and internaly connected to an XOR which is fed to the RCn output for external clock recovery applications.

System Interface Configuration

For normal transmit and receive operation, the device is configured as follows:

In host mode, MCLK can be either clocked or pulled high. If MCLK is pulled high, TCLK1 has to be provided for proper device operation. In addition, register bits e-AFE in the extended register have to be set to "1" to ensure proper device operation (see Extended Register Description for details).

In hardware mode, MCLK has to be pulled high and TCLK1 has to be provided for proper device operation.

Depending on the state of TCLK1 and TCLKn, the transmiter will Transmit All Ones (TAO), will go into power down, or will go into high impedance.

The status of TCLK1 and TCLKn has no effect on the receive paths. By setting MCLK low, all the receive paths are powered down.

Table 1 summarizes the different combinations between MCLK and TCLKn.

TABLE 1 — SYSTEM INTERFACE CONFIGURATION

Mode: Host or Hardware	MCLK	TCLK1	TCLKn	AFEn in e-AFE	Interface
Transmit and Receive Normal Operation					
Host (1) only	Clocked	Clocked	Clocked	1	Normal Operation
Host or Hardware (2)	High	Clocked	Clocked	DC(3)	Normal Operation
Transmit Interface Modes					
Host Only	Clocked	High (≥ 16 MCLK)		1	Transmit All One (TAO) signals to line side in corresponding transmit channel
Host Only	Clocked	Low (≥ 64 MCLK)		1	Corresponding transmit channel is set to power down mode
Host or Hardware	High/Low	TCLK1 is Clocked	TCLKn High (≥ 16 TCLK1)	DC	Transmit All One (TAO) signals to line side in corresponding transmit channel
Host or Hardware	High/Low		TCLKn Low (≥ 64 TCLK1)	DC	Corresponding transmit channel is set to power down mode
Host or Hardware	High/Low	TCLK1 not available (H/L)	DC	DC	All eight transmitter (TTIPn & (TRINGn) in high impedance state
Receive Interface Modes					
Host or Hardware	Low	The receive path is not affected by the status of TCLK1 or TCLKn		DC	All receive paths are powered down

NOTES:
1. In host mode bits AFEn in e-AFE must be set to 1 for proper operation (see Extended Register Description for detail).
2. In hardware mode MCLK must be pulled high and TCLK1 provided for proper operation.
3. DC = Don't Care

CLOCK EDGES

The active edge of RCn and SCLK (serial interface clock) are also selectable. If pin CLKE is Low, the active edge of RCn is the rising edge, as for SCLK, that is falling edge. On the contrary, if CLKE is High, the active edge of RCn is the falling edge and that of SCLK is rising edge. Pins RDPn, RDNn, and SDO are always active high, and those output signals are valid on the active edge of RCn and SCLK respectively. See Table 2 for details. Pin CLKE is used to set the active level for RDPn/RDNn raw slicing output: High for active high polarity and Low for active low. It should be noted that data on pin SDI are always active high and is sampled on the rising edge of SCLK. The data on pin TDP or TDN are also always active high but is sampled on the falling edge of TCLK, despite the level on CLKE.

RECEIVER

In receive path, the line signals couple into RRINGn and RTIPn via a transformer and are converted into RZ digital pulses by a data slicer. Adaptation for attenuation is achieved using an integral peak detector that sets the slicing levels. The recovered data clocked out of pin RDPn/RDNn in a undecoded dual rail RZ. Loss of signal is detected. This change in status may be enabled to generate an interrupt.

Peak Detector and Slicer

The slicer determines the presence and polarity of the received pulses. The raw positive slicer output appears on RDPn while the negative slicer output appears on RDNn. The slicer circuit has a built-in peak detector from which the slicing threshold is derived. The slicing threshold is default to 50% (typical) of the peak value.

Signals with an attenuation of up to 12dB (from 2.4V) can be recovered accurately by the receiver. To provide immunity from impulsive noise, the peak detectors are held above a minimum level of 0.150 V typically, despite the received signal level.

TABLE 2 — ACTIVE CLOCK EDGE AND ACTIVE LEVEL

Pin CLKE	RDP an RDN			SDO	
	RC Active Edge		Slicer Output		
Low	RC ↑	Active High	Active Low	SCLK ↓	Active High
High	RC ↓	Active High	Active High	SCLK ↑	Active High

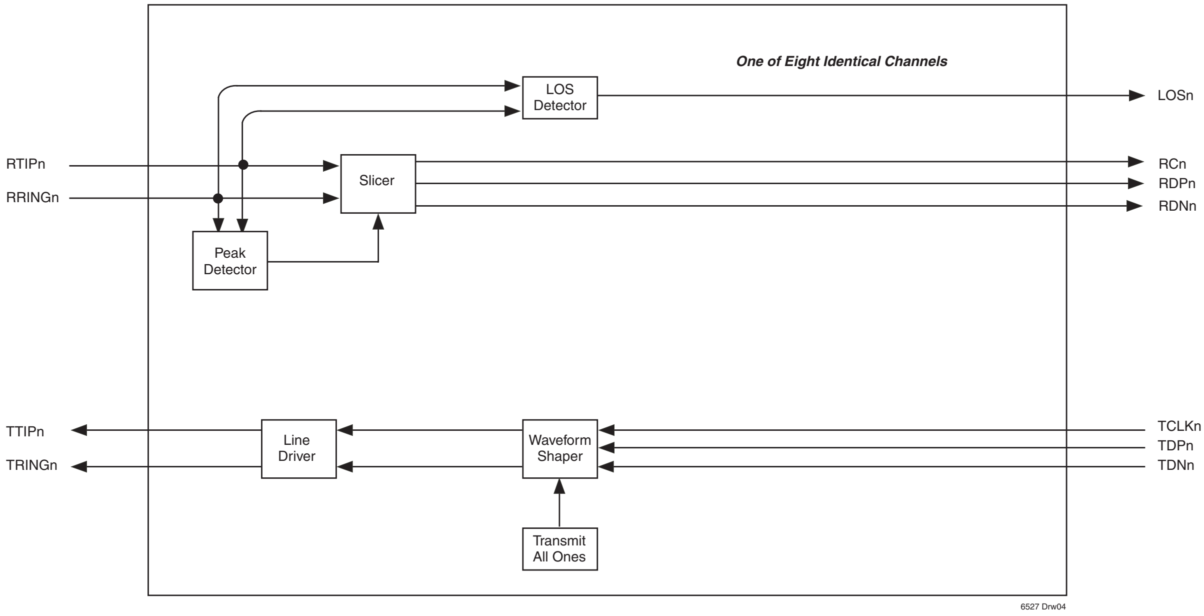


Figure 3. Analog Front End (AFE) Interface

Data Recovery

The analog line signals are converted to RZ digital bit streams on the RDPn/RDNn pins and internally connected to an XOR which is fed to the RCn output for external clock recovery applications.

Loss of Signal (LOS) Detection

The Loss of Signal Detector monitors the amplitude and density of the received signal on Receiver line before the transformer (measured on port A, B in Figure 6). The loss condition is reported by pulling pin LOS to high. In the same time, LOS alarm registers track LOS condition. When LOS is detected or cleared, and interrupt will be generated if not masked. In host mode, the detection supports the ANSI T1.231 mode and ITU-G.775 and ETSI 3600233 for E1 mode. In hardware mode, it only supports the ITU-G.775 and ANSI T1.231 specification.

Table 3 summarizes the conditions of LOS. The LOS condition is cleared upon detecting the signal level exceeds 540mV.

During LOS, the RDPn/RDNn output the sliced data when bit AISE in register GCF is 0 or output all ones as AIS (alarm indication signal) when bit AISE is set to 1; The RCn is replaced by MCLK only if the AISE is set.

TRANSMITTER

In transmit path, NRZ (non return to zero) data is clocked into the device on TDPn and TDNn. The data is sampled into the device on falling edges of TCLKn. The shape of the pulses are user programmable to ensure that the T1/E1 pulse template is met after the signal is passed through different cable lenghts or types.

TABLE 3 — LOS CONDITION

		STANDARD			Signal on Pin LOSn
		ANSI T1.231 for T1	G.775 for E1	ETSI 300233 for E1	
LOS Detected	Continuous Intervals	175	32	2048(1ms)	H
	Amplitude	below typ. 310mV (Vpp)	below typ. 310mV (Vpp)	below typ. 310mV (Vpp)	
LOS Cleared	Density	12.5% (16 marks in a sliding 128-bit period) with no more than 99 continuous zeros.	12.5% (4 marks in a sliding 32-bit period) with no more than 15 continuous zeros.	12.5% (4 marks in a sliding 32-bit period) with no more than 15 continous zeros	L
	Amplitude	exceed typ. 540mV (Vpp)	exceed typ. 540mV (Vpp)	exceed typ. 540mV (Vpp)	

Waveform Shaper

T1 pulse template, specified in the DSX-1 Cross-Connect by ANSI T1.102 is illustrated in Figure 4. The device has built-in transmit waveform templates, corresponding to 5 levels of pre-equalization for cable of a length from 0 to 655ft with each increment of 133ft.

E1 pulse template, specified in ITU-T G.703, is shown in Figure 5. The device has built-in transmit waveform templates for cable of 75Ω or 120Ω.

Any one of the six built-in waveform can be chosen in both hardware mode and host mode.

Setting the pins TS[2:0] as shown in Table 4 in hardware mode, is selecting the required waveform template for all the transmitters.

In host mode, the waveform template can be configured on per-channel basis. Bit TSIA[2:0] in register **TSIA** is used to select the channel and bit TS[2:0] in register **TS** is to select the required waveform template. Refer to ***Register Descritption*** for details. The built-in waveform shaper uses an internal high frequency clock which is 16XMCLK as clock reference. This function will be bypassed when MCLK is unavailable.

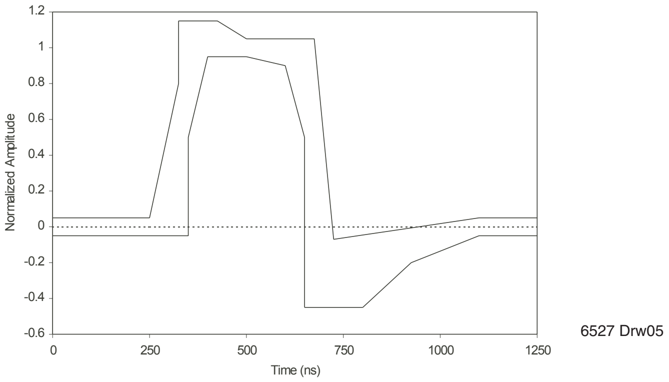


Figure 4. DSX-1 Waveform Template

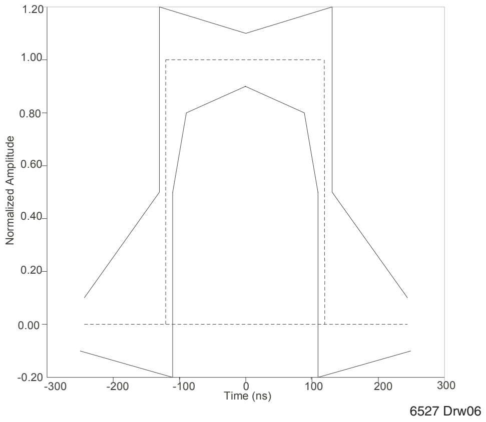


Figure 5. CEPT Waveform Template

TABLE 4 — BUILT-IN WAVEFORM TEMPLATE SELECTION

TS2	TS1	TS0	Service	Clock Rate	Cable Length	Maximum Cable Loss (dB)[1]
0	0	0	E1	2.048MHz	120 Ω / 75 Ω Cable	- -
0	0	1	Reserved			
0	1	0				
0	1	1	T1	1.544 MHz	0 - 133ft. ABAM	0.6
1	0	0			133 - 266ft. ABAM	1.2
1	0	1			266 - 399ft.ABAM	1.8
1	1	0			399 - 533ft. ABAM	2.4
1	1	1			533 - 655ft. ABAM	3.0

NOTE:

1. Maximum cable loss at 772 KHz

LINE INTERFACE CIRCUITRY

The transmit and receive interce RTIP/RRING connections provide a matched interface to the cable. Figure 6 shows the appropriate external components to connect with the cable for one transmit/receive channel. Table 6 summarizes the component values based on the specific application.

TRANSMIT DRIVER POWER SUPPLY

All transmit driver power supplies must be 5.0V or 3.3V.

In E1 mode, despite of the power supply voltage, the 75Ω/120Ω lines are driven through 9.5Ω series resistors and a 1:2 transformer.

In T1mode,when 5.0V is selected, 100Ω lines are driven through 9.1Ω series resistors and a 1:2 transformer. When 3.3V is selected, 100Ω lines are driven through a 1:2 transformer. To optimize the power consumption of the device, series resistors are removed in this case.

In harsh cable enviroments, series resistors are required to improve the transmit return loss performance and protect the device from surges coupling into the device.

TABLE 5 — TRANSFORMER SPECIFICATIONS

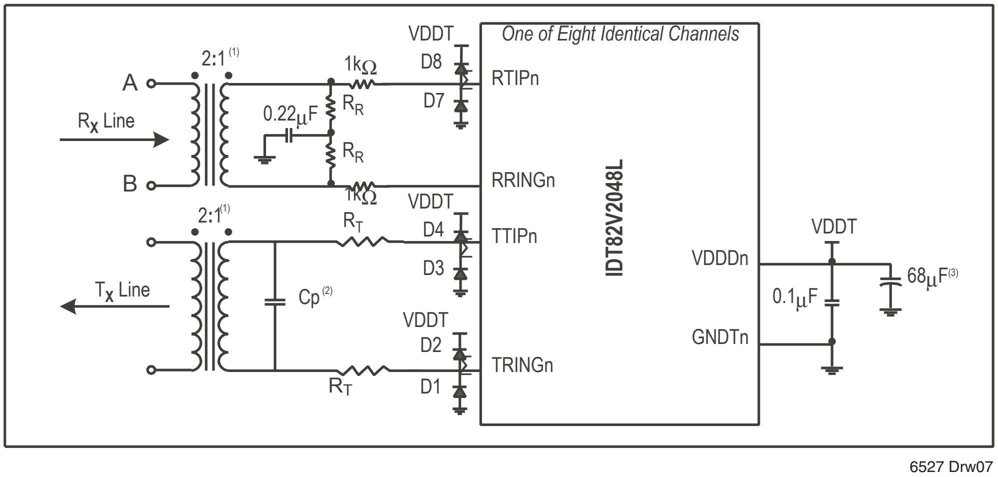
Electrical Specification @ 25°C										
Part No.		Turns Ratio (Pri: sec±2%)		OCI. @ 25°C (mH MIN)		L_I (mH MAX)		$C_{W/W}$ (pF MAX)		Package/ Schematic
STD Temp.	EXT Temp	Transmit	Receive	Transmit	Receive	Transmit	Receive	Transmit	Receive	
T1124	T1114	1:2CT	1CT:2	1.2	1.2	.6	.6	35	35	TOU/3

NOTES:

1. Pulse T1124 transformer is recommened to us in Standard (STD) operating temperature range (0° to 70°C), while Pulse T1114 is recommended to use in Extended (EXT) operating temperature range is -40° to +85°C.
2. Typical value. Adjust for actual board parasitics to obtain optium return loss.
3. Common decoupling capacitor for all VDDT and GNDT pins.

TABLE 6 — EXTERNAL COMPONENTS VALUES

	E1		T1	
Component	**75Ω Coax**	**120Ω Coax Twisted Pair**	**100Ω Twisted Pair VDDT = 5.0V**	**100Ω Twisted Pair VDDT = 3.3V**
R_T	9.5Ω ± 1%	9.5Ω ± 1%	9.1Ω ± 1%	0Ω
R_R	9.31Ω ± 1%	15Ω ± 1%	12.4Ω ± %	12.4Ω ± 1%
Cp	2200pf	1000pf		
D1 - D4	Nihon Inter Electronics - EP05Q03L, 11EQS03L, EC10QS04, EC10QS03L;			Motorola - MBR0540T1



NOTES:

1. Pulse T1124 transformer is recommened to use in Standard (STD) operating temperature range (0° to 70°C), while Pulse T1114 is recommended to use in Extended (EXT) operating temperature range is -40° to +85°C. See Transformer Specification Table for details.
2. Typical value. Adjust for actual board parasitics to obtain optium return loss.
3. Common decoupling capacitor for all VDDT and GNDT pins.

Figure 6. External Transmit/Receive Line Circuitry

POWER DRIVER FAILURE MONITOR

An internal power Driver Failure Monitor (DFM), parallelly connected with TTIPn and TRINGn, can detect short circuit failure in the secondary side of transformer. This feature is available only in host mode with no transmit series resistors, i.e. in T1mode with VDDT is 3.3V.

Bit SCPB in Register **GCF** decides whether the output driver short-circuit protection is enabled. (Refer to ***Programming information***). WHen it is enabled, the driver's output current is limited to 150mA (typical).

LINE PROTECTION

In transmit side, the Schottky diodes D1-D4 are required to protect the line driver and improve the design robustness. In receive side, the series resistors of 1kΩ are used to protect the receiver against current surges coupled in the device. It does not affect the receiver sensitivity, since the receiver impedance is as high as 120kΩ typically.

HITLESS PROTECTION SWITCHING (HPS)

The IDT82V2048L tranceiver include an output driver High-Z feature for T1/E1 redundancy applications. This feature greatly reduces the cost of implementing redundancy protection by eliminating external relays. Details of HPS is described in Application Note AN-357.

RESET

Writing register **RS** can cause software reset by initiating about 1ms reset cycle. The operation set all the registers to their default value.

POWER UP

During power up, an internal reset signal sets all the registers to default values. This procedure takes at least 2 machine cycles.

POWER DOWN

Each transmitter channel will be power down by pulling pin TCLKn to low for more than 64 MCLK cycles. (If MCLK is available) or about 30us (when MCLK is not available). In host mode, each transmitter channel will also be power down by setting bit TPDNn in **e-TPDNn** to 1.

All receivers will power down when MCLK is Low. In host mode, when MCLK is clocked or High, setting bit RPDNn in **e-RPDNn** to "1" will configure the corresponding receiver to power down.

INTERFACE WITH 5V LOGIC

The IDT82V2048L can interface directly with 5V family devices. The internal input pads are tolerant to 5V output from TTL and CMOS family devices.

TRANSMIT ALL ONES

In hardware mode, the TAOS mode is set by pulling TCLKn High for more that 16 MCLK cycles. In host mode, TAOS mode is set by programming register **TAO**. In addition, automatic TAO signals are inserted by setting register **ATAO** when Loss of Signal occurs. Note that the TAOS generator adopts MCLK as a timing reference. In order to assure that the output frequency is within specification limits, MCLK must have the applicable stability.

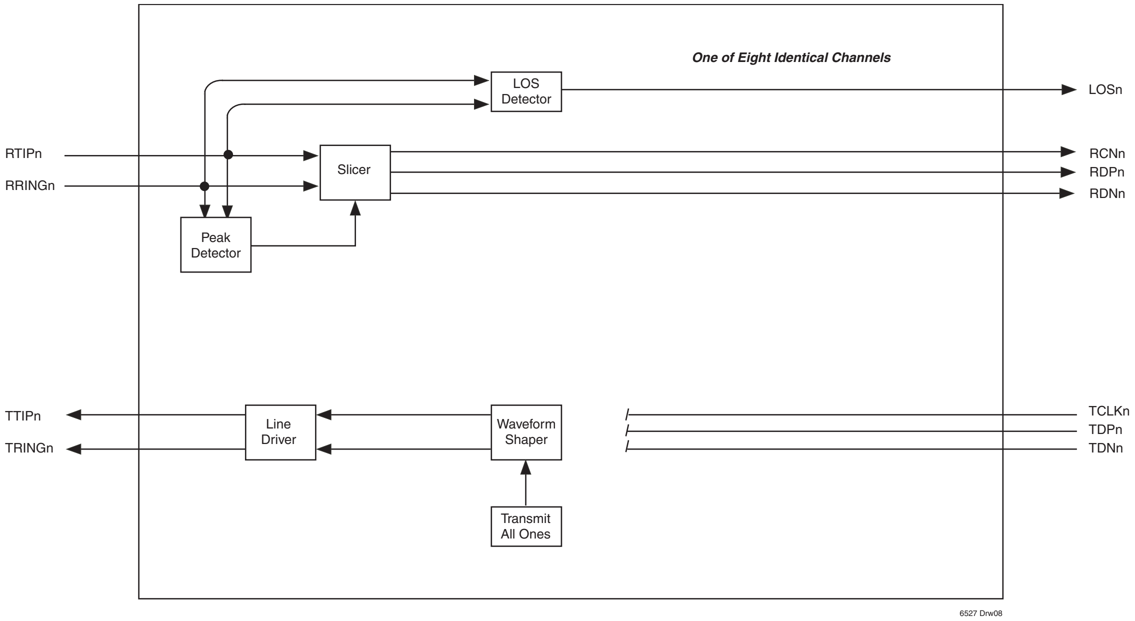


Figure 7. TAOS Data Path

HOST INTERFACES

The host interface provides access to read and write the registers in the device. The interface consists of serial host interface and parallel host interface. By pulling MODE2 to VDDIO/2 or to High, the device can be set to work in serial mode and in parallel mode respecively. In host mode operation, Extended register e-AFE has to be set to FF H for proper device operation. See Extended Register Description for details.

Parallel Host Interface

The interface is compatible with Motorola or Intel host. Pins MODE1 and MODE0 are used to select the operating mode of the parallel host interface. When pin MODE1 is pulled to Low, the host uses separate address bus and data bus. When High, multiplexed address/data bus is used. When pin MODE0 is pulled to Low, the parallel host interface is configured for Motorola compatible hosts. When High, for Intel compatible hosts. THis is well described in the ***Pin Description***. The host interface pins in each operation mode is tabulated in Table 6.

Serial Host Interface

By pulling pin MODE2 to VDDIOI/2, the device operates in the serial host Mode. In this mode, the registers are accessible through a 16-bit word which contains an 8-bit command/address byte (bit R/$\overline{W}$ and 5-address-bit A1-A5, A6 and A7 are ignored) and a subsequent 8-bit data byte (D0-D7). When bit R/$\overline{W}$ is 1, data is read out at pin SDO. When bit R/$\overline{W}$ is 0, data is written into pin SDI to the register which is indicated by address bits A5-A1.

TABLE 7 — PARALLEL HOST INTERFACE PINS

MODE[2:0]	Host Interface	Generic control, data and output pin name
100	Non-Multiplexed Motorola interface	$\overline{CS}$, $\overline{ACK}$, $\overline{DS}$, R/$\overline{W}$, $\overline{AS}$, A[4:0], D[7:0], $\overline{INT}$
101	Non-Multiplexed Intel interface	$\overline{CS}$, RDY, $\overline{WR}$, $\overline{RD}$, ALE, A[4:0], D[7:0], $\overline{INT}$
110	Multiplexed Motorola interface	$\overline{CS}$, $\overline{ACK}$, $\overline{DS}$, R/$\overline{W}$, $\overline{AS}$, AD[7:0], $\overline{INT}$
111	Multiplexed Intel interface	$\overline{CS}$, RDY, $\overline{WR}$, $\overline{RD}$, ALE, AD[7:0],$\overline{INT}$

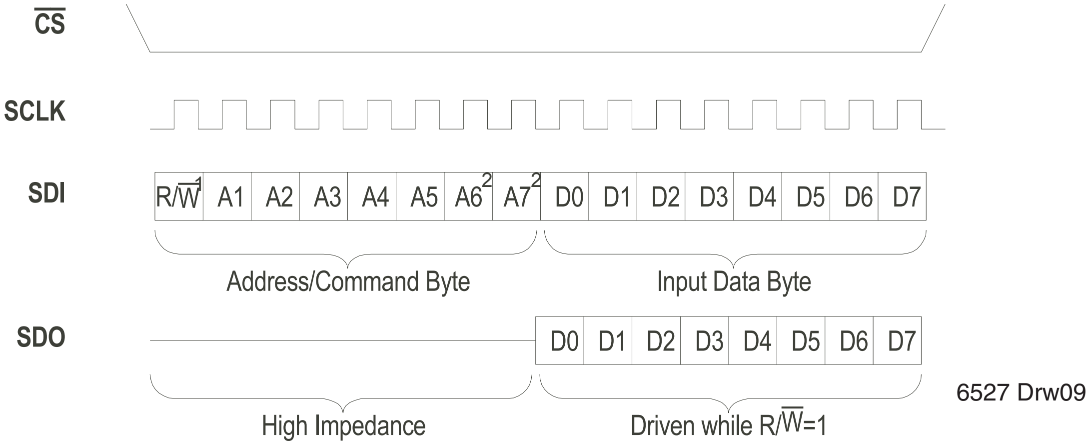


Figure 8. Serial Host Mode Timing

INTERRUPT HANDLING

Interrupt Sources

There are two kinds of interrupt sources:

1. Status change in the **LOS** (Loss of Signal) Status Register (04H). The analog/digital loss of signal detector continuously monitors the received signal to update the specific bit in **LOS** which indicates presence or absence of a LOS condition.

2. Status change in the **DF** (Driver Fault) Status Register (05H). The automatic power driver circuit continuously montiors the output drivers signal to update the specific bit in **DFM** which indicates presence or absence of a secondary driver short circuit condition.

Interrupt Enable

The IDT82V2048L provides a latched interrupt output ($\overline{\text{INT}}$) and the four kinds of interrupts are all reported by this pin. When the Interrupt Maske register (**LOSM, DFM**) is set to “1”, the Interrupt Status register (**LOSI, DFI**) is enabled repectively. Whenever there is a transition (“0” to “1” to “0”) in the corresponding Status register, the Interrupt Status register will change into “1”, which means an interrupt occurs, and there will be a transition from high to low on $\overline{\text{INT}}$. An external pull-up resistor of approximately 10kΩ is required to support the wire-OR operation of $\overline{\text{INT}}$. When any of the four Interrupt Mask registers is set to “0” (the power-on default value is “0”), the corresponding Interrupt Status register is disabled and the transition on status register is ignored.

Interrupt Clearing

When an interrupt occurs, the Interrupt Status registers (**LOSI,DFI**, are read to identify the interrupt source. And these registers will be cleared to “0” after the corresponding Status register (**LOS, DF**) being read. The Status registers will be cleared once the corresponding conditions are met.

Pin $\overline{\text{INT}}$ is pulled High when there are no pending interrupt left. The interrupt handling in the interrupt service routine is showed Figure 9.

G.772 MONITORING

The eight channels of IDT82V2048L can all be configured to work as regular transceivers. In applications using only seven channels (channels 1 to 7), channel 0 is configured to non-intrusively monitor any of the other channels’ inputs or outputs on the line side. The monitoring is non-intrusive per ITU-T G.772. Figure 10 shows the Monitoring Principle. The receiver or transmitter path to be monitored is configured by pin MC[0:3] in hardware mode or by **PMON** in host mode (refer to ***Programming Information*** for details).

The signal which is monitored goes through the clock and data recovery circuit of channel 0. The monitored clock can output on RCn0 which can be used as a timing interfaces derived from E1 signal. The monitored data can be observed digitally at the output pin RCn0, RD0/RDP0 and RDN0. LOS detector is still in use in channel 0 for the monitored signal.

In monitoring mode, channel 0 can be configured to the Remote Loopback. The signal which is being monitored will output on TTIP0 and TRING0. The output signal can then be connected to a standard test equipment with an E1 electrical interface for non-intrusive monitoring.

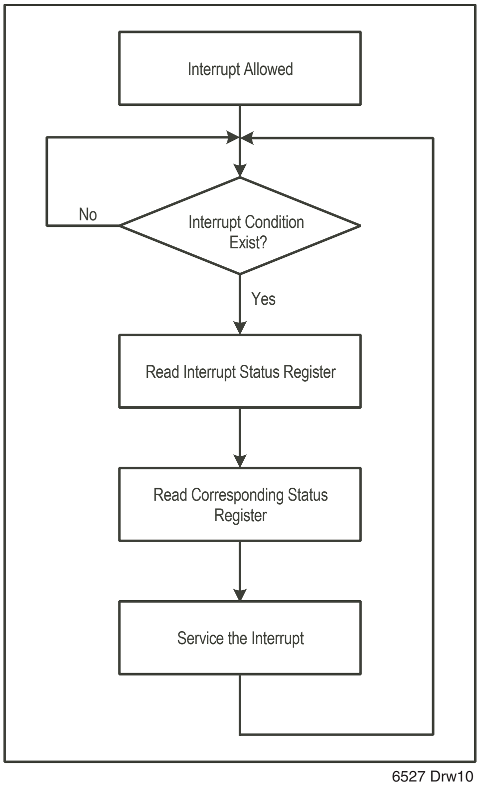


Figure 9. Interrupt Service Routine

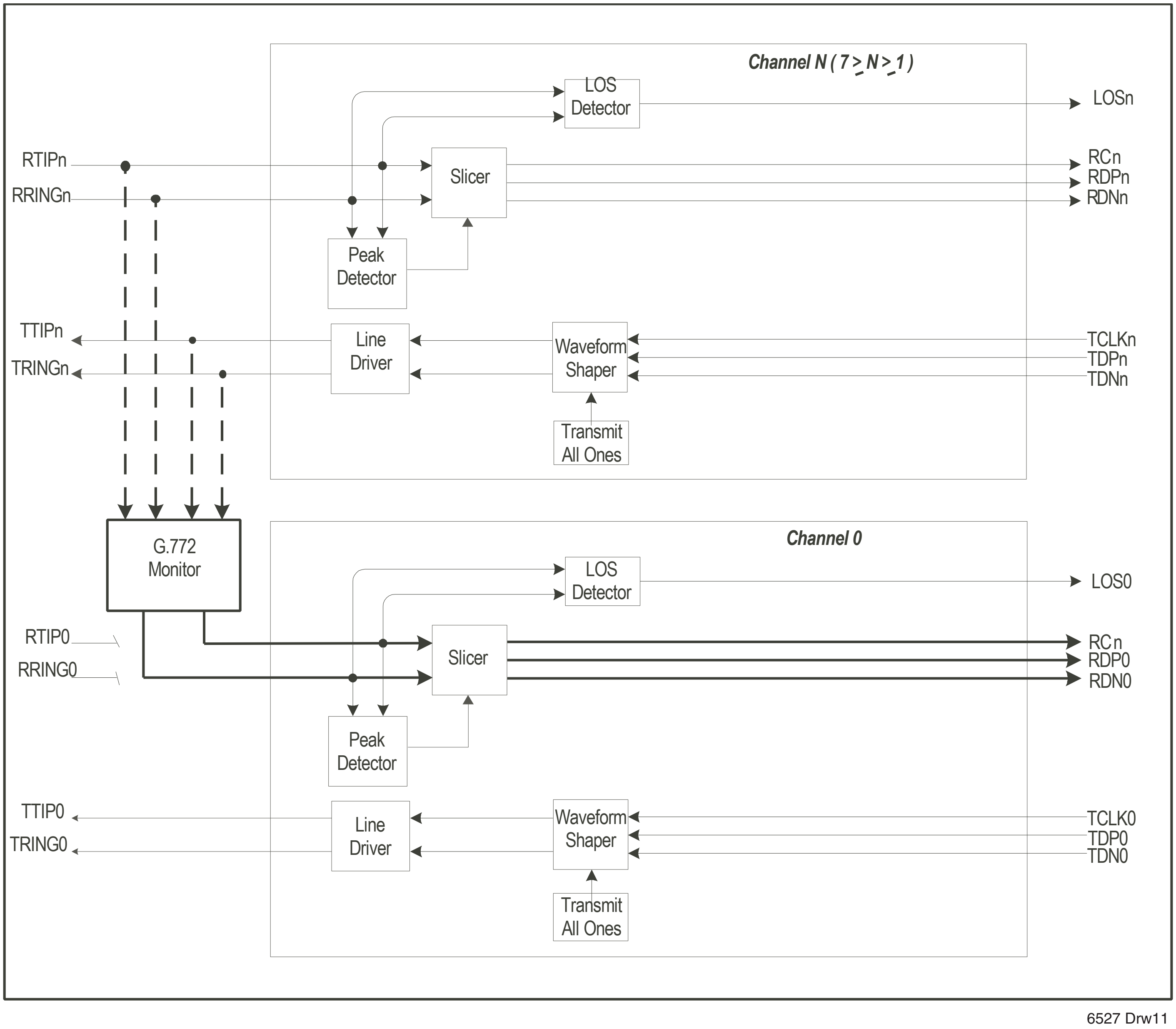


Figure 10. Monitoring Principle

PROGRAMMING INFORMATION

REGISTER LIST AND MAP

There are 17 primary registers (including an Address Pointer Control Register), including 4 Extended registers in the device[1].

Whatever the control interface is, 5 address bits are used to set the registers. In non-multiplexed parallel interface mode, the five dedicated address bits are A[4:0]. In multiplexed parallel interface mode, AD[4:0] carries the address information. In serial interface mode, A[5:1] are used to address the register. The Address Pointer Control Register (**ADDP**), addressed as 11111 of 1F Hex, switches between primary registers bank and Extended registers bank.

By setting the content of **ADDP** to AAH, the 5 address bits point to the Extended register bank, that is, 16 Extended registers are then available to access. By clearing ADDP, the primary registers are accessible again.

TABLE 8 — PRIMARY REGISTER LIST

Address			Register A7-A0	R/W	Explanation
Hex	Serial Interface A7-A1	Parallel Interface			
00	XX00000	XXX00000	ID	R	Device ID Register
01	XX00001	XXX00001			Reserved
02	XX00010	XXX00010			
03	XX00011	XXX00011	TAO	R/W	Transmit All One Code Configuration Register
04	XX00100	XXX00100	LOS	R	Loss of Signal Status Register
05	XX00101	XX00101	DF	R	Driver Fault Status Register
06	XX00110	XXX00110	LOSM	R/W	LOS Interrupt Mask Register
07	XX00111	XXX00111	DFM	R/W	Driver Fault Interrupt Mast Register
08	XX01000	XXX01000	LOSI	R	LOS Interrupt Status Register
09	XX01001	XXX01001	DFI	R	Driver Fault Interrupt Status Register
0A	XX01010	XXX01010	RS	W	Software Reset Register
0B	XX01011	XXX01011	PMON	R/W	Performance Monitor Configuration Register
0C	XX01100	XXX01100			Reserved
0D	XX01101	XXX01101	LAC	R/W	LOS Criteria Configuration Register
0E	XX01110	XXX01110	ATAO	R/W	AutomaticTAO Configuration Register
0F	XX01111	XXX01111	GCF	R/W	Global Configuration Register
10	XX10000	XX10000	TSIA	R/W	Indirect Address Register for Transmit Template Select
11	XX10001	XXX10001	TS	R/W	Transmit Template Select Register
12	XX10010	XXX10010	OE	R/W	Output Enable Configuration Register
13	XX10011	XXX10011			Reserved
14	XX10100	XXX10100			
15	XX10101	XXX10101			
16	XX10110	XXX10110			
17	XX10111	XXX10111			
18	XX11000	XXX11000			
19	XX11001	XX11001			
1A	XX11010	XXX11010			
1B	XX11011	XXX11011			
1C	XX11100	XXX11100			
1D	XXX11101	XXX11101			
1E	XX11110	XXX11110			
1F	XX11111	XXX11111	ADDP	R/W	Address pointer control Register for switching between primary register bank and Extended register bank

NOTE:

1. In host mode operation, Extended register e-AFE has to be set to FF H for proper device operation. See Extended Register Description for details.

TABLE 9 — EXTENDED (INDIRECT ADDRESS MODE) REGISTER LIST

Address			Register A7-A0	R/W	Explanation
Hex	Serial Interface A7-A1	Parallel Interface			
00	XX00000	XXX00000			Reserved
01	XX00001	XXX00001			Reserved
02	XX00010	XXX00010	e-AFE(1)	R/W	AFE Enable Register
03	XX00011	XXX00011	e-RDPN	R/W	Receiver n Powerdown Enable/Disable Register
04	XX00100	XXX00100	e-TPDN	R/W	Transmitter n Powerdown Enable/Disable Register
05	XX00101	XXX00101			Reserved
06	XX00110	XXX00110			
07	XX00111	XXX00111	e-EQUA	R/W	Enable Equalizer Enable/Disable Register
08	XX01000	XXX01000			Reserved
09	XX01001	XXX01001			
0A	XX01010	XXX01010			
0B	XX01011	XXX01011			
0C	XX01100	XXX01100			
0D	XX01101	XX011010			
0E	XX01110	XXX01110			
0F	XX01111	XXX01111			
10	XX1000	XXX10000			Test
11	XX10001	XXX10001			
12	XX10010	XXX10010			
13	XX10011	XXX10011			
14	XX10100	XXX10100			
15	XX10101	XXX10101			
16	XX10110	XXX10110			
17	XX10111	XX101111			
18	XX11000	XXX11000			
19	XX11001	XXX11001			
1A	XX11010	XXX11010			
1B	XX11011	XXX11011			
1C	XX11100	XXX11100			
1D	XX11101	XXX11101			
1E	XX11110	XXX11110			
1F	XX11110	XXX11110	ADDP	R/W	Address pointer control register for switching between primary register bank and Extended register bank.

NOTE:

1. In host mode operation, Extended register e-AFE has to be set to FF H for proper device operation. See Extended Register Description for details.

TABLE 10 — PRIMARY REGISTER MAP

Register	Address R/W Default	B7	B6	B5	B4	B3	B2	B1	B0
ID	00 Hex R/W Default	ID 7 R 0	ID 6 R 0	ID 5 R 0	ID 4 R 1	ID 3 R 0	ID 2 R 0	ID 1 R 0	ID 0 R 0
TAO	03 Hex R/W Default	TAO 7 R/W 0	TAO 6 R/W 0	TAO 5 R/W 0	TAO 4 R/W 0	TAO 3 R/W 0	TAO 2 R/W 0	TAO 1 R/W 0	TAO 0 R/W 0
LOS	04 Hex R/W Default	LOS 7 R 0	LOS 6 R 0	LOS 5 R 0	LOS 4 R 0	LOS 3 R 0	LOS 2 R 0	LOS 1 R 0	LOS 0 R 0
DF	05 Hex R/W Default	DF 7 R 0	DF 6 R 0	DF 5 R 0	DF 4 R 0	DF 3 R 0	DF 2 R 0	DF 1 R 0	DF 0 R 0
LOSM	06 Hex R/W Default	LOSM 7 R/W 0	LOSM 6 R/W 0	LOSM 5 R/W 0	LOSM 4 R/W 0	LOSM 3 R/W 0	LOSM 2 R/W 0	LOSM 1 R/W 0	LOSM 0 R/W 0
DFM	07 Hex R/W Default	DFM 7 R/W 0	DFM 6 R/W 0	DFM 5 R/W 0	DFM 4 R/W 0	DFM 3 R/W 0	DFM 2 R/W 0	DFM 1 R/W 0	DFM 0 R/W 0
LOSI	08 Hex R/W Default	LOSI 7 R 0	LOSI 6 R 0	LOSI 5 R 0	LOSI 4 R 0	LOSI 3 R 0	LOSI 2 R 0	LOSI 1 R 0	LOSI 0 R 0
DFI	09 Hex R/W Default	DFI 7 R 0	DFI 6 R 0	DFI 5 R 0	DFI 4 R 0	DFI 3 R 0	DFI 2 R 00	DFI 1 R 0	DFI 0 R 0
RS	0A Hex R/W Default	RS 7 W 1	RS 6 W 1	RS 5 W 1	RS 4 W 1	RS 3 W 1	RS 2 W 1	RS 1 W 1	RS 0 W 1
PMON	0B Hex R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	MC 3 R/W 0	MC 2 R/W 0	MC 1 R/W 0	MC 0 R/W 0
LAC	0D Hex R/W Default	LAC 7 R/W 0	LAC 6 R/W 0	LAC 5 R/W 0	LAC 4 R/W 0	LAC 3 R/W 0	LAC 2 R/W 0	LAC 1 R/W 0	LAC 0 R/W 0
ATAO	0E Hex R/W Default	ATA 7 RW 0	ATA 6 R/W 0	ATA 5 R/W 0	ATA 4 R/W 0	ATA 3 R/W 0	ATA 2 R/W 0	ATA 1 R/W 0	ATA 0 R/W 0
GCF	0F Hex R/W Default	- R/W 0	AISE R/W 0	SCPB R/W 0	CODE R/W 0	JADP R/W 0	JABW R/W 0	JACF 1 R/W 0	JACF 0 R/W 0
TSIA	10 Hex R/W Default	0 R/W 0	0 R/W 0	0 R/W 0	0 R/W 0	0 R/W 0	TSIA 2 R/W 0	TSIA 1 R/W 0	TSIA 0 R/W 0
TS	11 Hex R/W Default	- R/W 0	- R/W 0	- R/W 0	- R/W 0	- R/W 0	TS 2 R/W 0	TS 1 R/W 0	TS 0 R/W 0
OE	12 Hex R/W Default 0	OE 7 R/W 0	OE 7 R/W 0	OE 7 R/W 0	OE 7 R/W 0	OE 7 R/W 0	OE 7 R/W 0	OE 7 R/W 0	OE 7 R/W 0
ADDP	1F Hex R/W Default	ADDP 7 R/W 0	ADDP 6 R/W 0	ADDP 5 R/W 0	ADDP 4 R/W 0	ADDP 3 R/W 0	ADDP 2 R/W 0	ADDP 1 R/W 0	ADDP 0 R/W 0

TABLE 11 — EXTENDED (INDIRECT ADDRESS MODE) REGISTER MAP

Register	Address R/W Default	B7	B6	B5	B4	B3	B2	B1	B0
e-AFE[(1)]	02 Hex R/W Default	AFE 7 R/W 0	AFE 6 R/W 0	AFE 5 R/W 0	AFE 4 R/W 1	AFE 3 R/W 0	AFE 2 R/W 0	AFE 1 R/W 0	AFE 0 R/W 0
e-RDPN	03 Hex R/W Default	RPDN 7 R/W 0	RPDN 6 R/W 0	RPDN 5 R/W 0	RDPN 4 R/W 0	RDPN 3 R/W 0	RDPN 2 R/W 0	RDPN 1 R/W 0	RDPN 0 R/W 0
e-TPDN	04 Hex R/W Default	TPDN 7 R/W 0	TPDN 6 R/W 0	TPDN 5 R/W 0	TPDN 4 R/W 0	TPDN 3 R/W 0	TPDN 2 R/W 0	TPDN 1 R/W 0	TPDN 0 R/W 0
e-EQUA	07 Hex R/W Default	EQUA 7 R 0	EQUA 6 R 0	EQUA 5 R 0	EQUA 4 R 0	EQUA 3 R 0	EQUA 2 R 0	EQUA 1 R 0	EQUA 0 R 0
ADDP	1F Hex R/W Default	ADDP 7 R/W 0	ADDP 6 R/W 0	ADDP 5 R/W 0	ADDP 4 R/W 0	ADDP 3 R/W 0	ADDP 2 R/W 0	ADDP 1 R/W 0	ADDP 0 R/W 0

NOTE:

1. In host mode operation, Extended register e-AFE has to be set to FF H for proper device operation. See Extended Register Description for details.

REGISTER DESCRIPTION

PRIMARY REGISTER DESCRIPTION

ID: Device ID Register (R, Address = 00 Hex)

Symbol	Position	Default	Description
ID[7:0]	ID.7.0	10 H	An 8-bit word is pre-set into the device as the identification and revision number. This number is different with the functional changes and is mask programmed.

TAO: Transmit All One Code Configuration Register (R/W, Address = 03 Hex)

Symbol	Position	Default	Description
TAO[7:0]	TAO.7.0	00 H	0 = Normal operation (Default) 1 = Transmit all one code.

LOS: Loss of Signal Status Register (R, Address = 04 Hex)

Symbol	Position	Default	Description
LOS[7:0]	LOS.7.0	00 H	0 = Normal operation (Default) 1 = Loss of signal detected.

DF: Driver Fault Status Register (R, Address = 05 Hex)

Symbol	Position	Default	Description
DF[7:0]	DF.7.0	00 H	0 = Normal operation (Default) 1 = Driver fault detected. *Note that DF is available only in T1 mode with 3.3V (without transmit series resistors).*

LOSM: Loss of Signal Interrupt Mask Register (R/W, Address = 06 Hex)

Symbol	Position	Default	Description
LOSM[7:0]	LOSM.7.0	00 H	0 = LOS interrupt is not allowed. (Default) 1 = LOS interrupt is allowed.

DFM: Driver Fault Interrupt Mask Register (R/W, Address = 07 Hex)

Symbol	Position	Default	Description
DFM[7:0]	DFM.7.0	00 H	0 = Driver fault interrupt is not allowed. (Default) 1 = Driver fault interrupt is allowed.

LOSI: Loss of Signal Interrupt Status Register (R, Address = 08 Hex)

Symbol	Position	Default	Description
LOSI[7:0]	LOSI.7.0	00 H	0 = (Default). Or after **LOS** read operation. 1 = Any transition on **LOSn** (Corresponding **LOSMn** is set to 1).

DFI: Driver Fault Interrupt Status Register (R, Address = 09 Hex)

Symbol	Position	Default	Description
DFI[7:0]	DFI.7.0	00 H	0 = (Default). Or after **DF** read operation. 1 = Any transition on **DFn** (Corresponding **DFn** is set to 1).

RS: Software Reset Register (W, Address = 0A Hex)

Symbol	Position	Default	Description
RS[7:0]	RS.7.0	FF H	Writing to this register will not change the content in this register but initiate a 1µs reset cycle, which means all the registers in the device are set to their default values.

PMON: Performance Monitor Configuration Register (R/W, Address = 0B Hex)

<table>
<tr><th>Symbol</th><th>Position</th><th>Default</th><th colspan="2">Description</th></tr>
<tr><td>-</td><td>PMON.7-4
1 = Reserved.</td><td>0000</td><td colspan="2">0 = Normal operation (Default)</td></tr>
<tr><td rowspan="17">MC[3:0]</td><td rowspan="17">PMON.3-0</td><td rowspan="17">0000</td><td>MC[3:0]</td><td>Monitoring Configurations</td></tr>
<tr><td>0000</td><td>Normal operation without monitoring.</td></tr>
<tr><td>0001</td><td>Monitoring receiver 1.</td></tr>
<tr><td>0010</td><td>Monitoring receiver 2.</td></tr>
<tr><td>0011</td><td>Monitoring receiver 3.</td></tr>
<tr><td>0100</td><td>Monitoring receiver 4.</td></tr>
<tr><td>0101</td><td>Monitoring receiver 5.</td></tr>
<tr><td>0110</td><td>Monitoring receiver 6..</td></tr>
<tr><td>0111</td><td>Monitoring receiver 7.</td></tr>
<tr><td>1000</td><td>Normal operation without monitoring.</td></tr>
<tr><td>1001</td><td>Monitoring transmitter 1.</td></tr>
<tr><td>1010</td><td>Monitoring transmitter 2.</td></tr>
<tr><td>1011</td><td>Monitoring transmitter 3.</td></tr>
<tr><td>1100</td><td>Monitoring transmitter 4.</td></tr>
<tr><td>1101</td><td>Monitoring transmitter 5.</td></tr>
<tr><td>1110</td><td>Monitoring transmitter 6.</td></tr>
<tr><td>1111</td><td>Monitoring transmitter 7.</td></tr>
</table>

LAC: LOS Criteria Configuration Register (R/W, Address = 0D Hex)

Symbol	Position	Default	Description
LAC[7:0]	LAC.7.0	00 H	For E1 mode, the criteria is selected as below: 0 = G.775 mode. (Default) 1 = ETSI 300233 mode. for T1 mode, the LOS cirteria meets T1.231.

ATAO: Automatice TAO Configuration Register (R/W, Address = 0E Hex)

Symbol	Position	Default	Description
ATAO[7:0]	ATAO.7.0	00 H	0 = No automatic TAO (Default) 1 = Automatic transmit all ones to the line side on LOS.

GCF: Global Configuration Register (R/W, Address = 0F Hex)

Symbol	Position	Default	Description
-	GCF.7-6	0	0 = Normal Operation (Default) 1 = Reserved.
SCPB	GCF.5	0	**Short Circuit Protection Enable.** 0 = Short circuit protection is enabled. (Default) 1 = Short circuit protection is disabled.
-	GCF.4-0	0	0 = Normal Operation (Default) 1 = Reserved.

TSIA: Indirect Address Register for Transmit Template Select Registers (R/W, Address = 10 Hex)

Symbol	Position	Default	Description			
-	TSIA.7	00000	0 = Normal Operatin (Default) 1 = Reserved.			
TSIA[2:0]	TSIA.2-0	000	TSIA[2:0]	Channel	TSIA[2:0]	Channel
			000	0	100	4
			001	1	101	5
			010	2	110	6
			011	3	111	7

TS: Transmit Template Select Register (R/W, Address = 11 Hex)

<table>
<tr><th>Symbol</th><th>Position</th><th>Default</th><th colspan="3">Description</th></tr>
<tr><td>-</td><td>TS.7.3</td><td>00000</td><td colspan="3">0 = Normal Operatin (Default)
1 = Reserved.</td></tr>
<tr><td rowspan="9">TS[2:0]</td><td rowspan="9">TS.2-0</td><td rowspan="9">000</td><td colspan="3">TS[2:0] select one of eight built-in transmit template for different applications.</td></tr>
<tr><td>TS[2:0]</td><td>Mode</td><td>Cable Length</td></tr>
<tr><td>000</td><td>E1</td><td>75 Ω coaxial cable/120 Ω twisted pair cable.</td></tr>
<tr><td>001
010</td><td colspan="2">Reserved</td></tr>
<tr><td>011</td><td>T1</td><td>0 - 133 ft.</td></tr>
<tr><td>100</td><td>T1</td><td>133 - 266 ft.</td></tr>
<tr><td>101</td><td>T1</td><td>266 - 399 ft.</td></tr>
<tr><td>110</td><td>T1</td><td>399 - 533 ft.</td></tr>
<tr><td>111</td><td>T1</td><td>533 - 655 ft.</td></tr>
</table>

OE: Output Enable Configuration Register (R/W, Address = 12 Hex)

Symbol	Position	Default	Description
OE[7:0]	OE.7.0	00 H	0 = Transmit drivers enabled. (Default) 1 = Transmit drivers placed in high impedance state.

ADDP: Address Pointer Control Register (R/W, Address = 1F Hex)

Symbol	Position	Default	Description
ADDP[7:0]	ADDP.7-0	00 H	Two Kinds of configuration in this register can be set to switch between primary register bank and Extended register bank. When power up, the address pointer will point to the top address of primary register bank automatically. 00H = The address pointer points to the top address of primary register bank. (default). AAH = The address pointer points to the top address of Extended register bank.

EXTENDED REGISTER DESCRIPTION

e-AFE: AFE Enable Selection Register (R/W, Extended Address = 02 Hex)

Symbol	Position	Default	Description
AFE[7:0]	AFE.7-0	00 H[1]	0 = Reserved (Default) 1 = **AFE mode enabled**

Note:

1. In host mode AFE[7:0] must be set to FF H for proper device operation

e-RPDN: Receiver Powerdown Register (R/W, Extended Address = 03 Hex)

Symbol	Position	Default	Description
RPDN[7:0]	RPDN.7-0	00 H	0 = Normal Operation (Default) 1 = Power down in receiver n.

e-TPDN: Transmitter n Powerdown Register (R/W, Extended Address = 04 Hex)

Symbol	Position	Default	Description
TPDN[7:0]	TPDN.7-0	00 H	0 = Normal Operation (Default) 1 = Power down in Transmitter n (the corresponding transmit output driver enters a low power high impedance mode). *Note that transmitter n is power down when either pin TCLKn is pulled to low ot TPDNn is set to 1.*

e-EQUA: Receive Equalizer Enable/Disable Register (R/W, Extended Address = 07 Hex)

Symbol	Position	Default	Description
EQUA[7:0]	EQUA.7-0	00 H	0 = Normal Operation (Default) 1 = Equalizer in Receiver n enabled, which can improve the receive performance when transmission lenghts is more than 200 m.

IEEE STD 1149.1 JTAG TEST ACCESS PORT

The IDT82V2048L supports the digital Boundary Scan Specification as described in the IEEE 1149.1 standards.

The boundary scan architecture consists of data and instruction registers plus a Test Access Port (TAP) controller. Control of the TAP is acheived through signals applied to the Test Mode Select (TMS) and Test Clock (TCK) input pins. Data is shifted into the registers via the Test Data Input (TDI) pin, and shifted out of the registers via the Test Data Output (TDO) pin. Both TDI and TDO are clocked at a rate determined by TCK.

The JTAG boundary scan registers includes BSR (Boundary Scan Registers), IDR (Device Identification Register), BR (Bypass Register) and IR (Instruction Register). These will be described in the following pages. *Refer to Figure 11 for architecture.*

JTAG INSTRUCTIONS AND INSTRUCTION REGISTER (IR)

The **IR** (Instruction Register) with instruction decode block is used to select the test to be executed or the data register to be accessed or both.

The instructions are shifted in LSB first to this 3-bit register. *See Table 8 for details ofthe codes and the instructions related.*

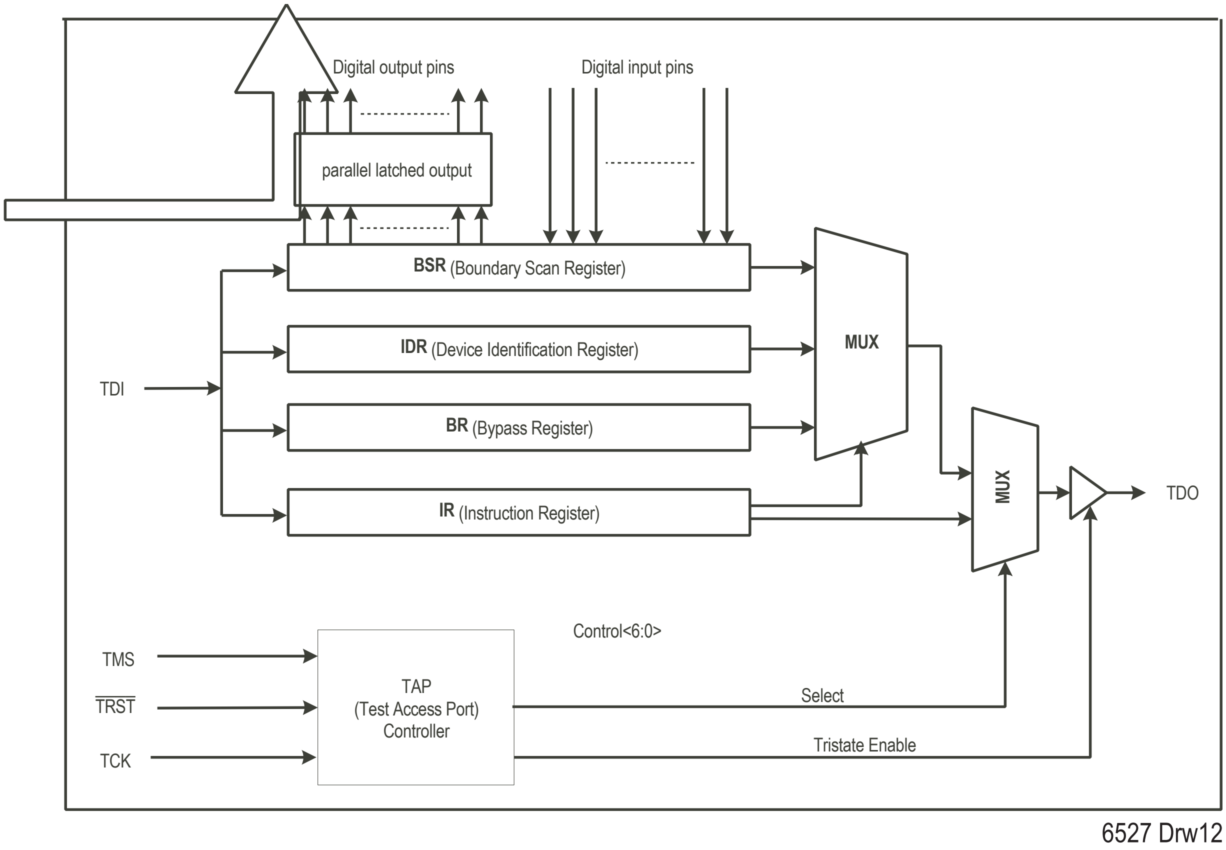


Figure 11. JTAG Architecture

TABLE 12 — INSTRUCTION REGISTER DESCRIPTION

IR CODE	INSTRUCTION	COMMENTS
000	Extest	The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. The signal on the output pins can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.
100	Sample / Preload	The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. The normal path between IDT82V2048L logic and the I/O pins is maintained. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DT state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.
110	Idcode	The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.
111	Bypass	The bypass instruction shifts data from input TDI and TDO with one TCK clock period delay. The instruction is used to bypass the device.

TABLE 13 — DEVICE IDENTIFICATION REGISTER DESCRIPTION

BIT No.	COMMENTS
0	Set to "1"
1-11	Producer Number
12-27	Part Number
28-31	Device Revision

JTAG DATA REGISTER

Device Identification Register (IDR)

The IDR can be set to define the producer number, part number and the device revision, which can be used to verify the proper version or revision number that has been used in the system under test. The IDR is 32 bits long and is partitioned as in *Table 14*. Data from the IDR is shifted out to TDO LSB first.

Bypass Register (BR)

The BR consists of a single bit, it can provide a serial path between the TDI input and TDO output, bypassing the BSR to reduce test access times.

Boudary Scan Register (BSR)

The BSR can apply and read test patterns in parallel to or from all the digital I/O pins. The BSR is a 98 bits long shift register and is initialized and read using the instruction EXTEST or SAMPLE/PRELOAD. Each pin is related to one or more bits in the BSR. *Please refer to Table 15 for details of BSR bits and their functions.*

TEST ACCESS PORT CONTROLLER

The TAP controller is a 16-state synchrnous state machine. Figure 6 shows its state diagram. A description of each state follows. Note that the figure contains two main branches to access either the data or instruction registers. The value shown next to each state transition in this figure states the value present at TMS at each rising edge of TCK. *Please refer to Table 14.*

TABLE 14 — BOUNDARY SCAN REGISTER DESCRIPTION

BIT No.	BIT SYMBOL	PIN SIGNAL	TYPE	COMMENTS
0	POUT0	D0	I/O	
1	PIN0	D0	I/O	
2	POUT1	D1	I/O	
3	PIN1	D1	I/O	
4	POUT2	D2	I/O	
5	PIN2	D2	I/O	
6	POUT3	D3	I/O	
7	PIN3	D3	I/O	
8	POUT4	D4	I/O	
9	PIN4	D4	I/O	
10	POUT5	D5	I/O	
11	PIN5	D5	I/O	
12	POUT6	D6	I/O	
13	PIN6	D6	I/O	
14	POUT7	D7	I/O	

TABLE 14 — BOUNDARY SCAN REGISTER DESCRIPTION (CONTINUED)

BIT No.	BIT SYMBOL	PIN SIGNAL	TYPE	COMMENTS
15	PIN7	D7	I/O	
16	PIOS	N/A	-	Controls pin D7-0 When “0” , the pins are configured as outputs. The output values to the pins are set in POUT7-0. When “1”, the pins are High-Z. The input value to the pins are read in PIN7-0
17	TCLK1	TCLK1	I	
18	TDP1	TDP1	I	
19	TDN1	TDN1	I	
20	RC1	RC1	O	
21	RDP1	RDP1	O	
22	RDN1	RDN1	O	
23	HZEN1	N/A	-	Controls pin RDP1, RDN1 and RC1 When “0”, the outputs are enabled on the pins When “1”, the pins are High-Z.
24	LOS1	LOS1	O	
25	TCLK0	TCLK0	I	
26	TDP0	TDP0	I	
27	TDN0	TDN0	I	
28	RC0	RC0	O	
29	RDP0	RDP0	O	
30	RDN0	RDN0	O	
31	HZEN0	N/A	-	Controls pin RDP0, RDN0 and RC0. When “0”, the outputs are enabled on the pins. When “1”, the pins are High-Z
32	LOS0	LOS0	O	
33	MODE1	MODE1	I	
34	LOS3	LOS3	O	
35	RDN3	RDN3	O	
36	RDP3	RDP3	O	
37	HZEN3	N/A	-	Controls pin RDP3, RDN3 and RC3. When “0”, the outputs are enabled on the pins. When “1”, the pins are High-Z
38	RC3	RC3	O	
39	TDN3	TDN3	I	
40	TDP3	TDP3	I	
41	TCLK3	TCLK3	I	
42	LOS2	LOS2	O	
43	RDN2	RDN2	O	
44	RDP2	RDP2	O	
45	HZEN2	N/A	-	Controls pin RDP2, RDN2 and RC2. When “0”, the outputs are enabled on the pins. When “1”, the pins are High-Z
46	RC2	RC2	O	
47	TDN2	TDN2	I	
48	TDP2	TDP2	I	
49	TCLK2	TCLK2	I	
50	INT	INT	O	
51	ACK	ACK	O	
52	SDORDYS	N/A	-	Control pin ACK. When “0”, the outputs is enabled on pin $\overline{\text{ACK}}$. When “1”, the pin is High-Z.
53	WRB	DS	I	
54	RDB	R/W	I	
55	ALE	ALE	I	

TABLE 14 — BOUNDARY SCAN REGISTER DESCRIPTION (CONTINUED)

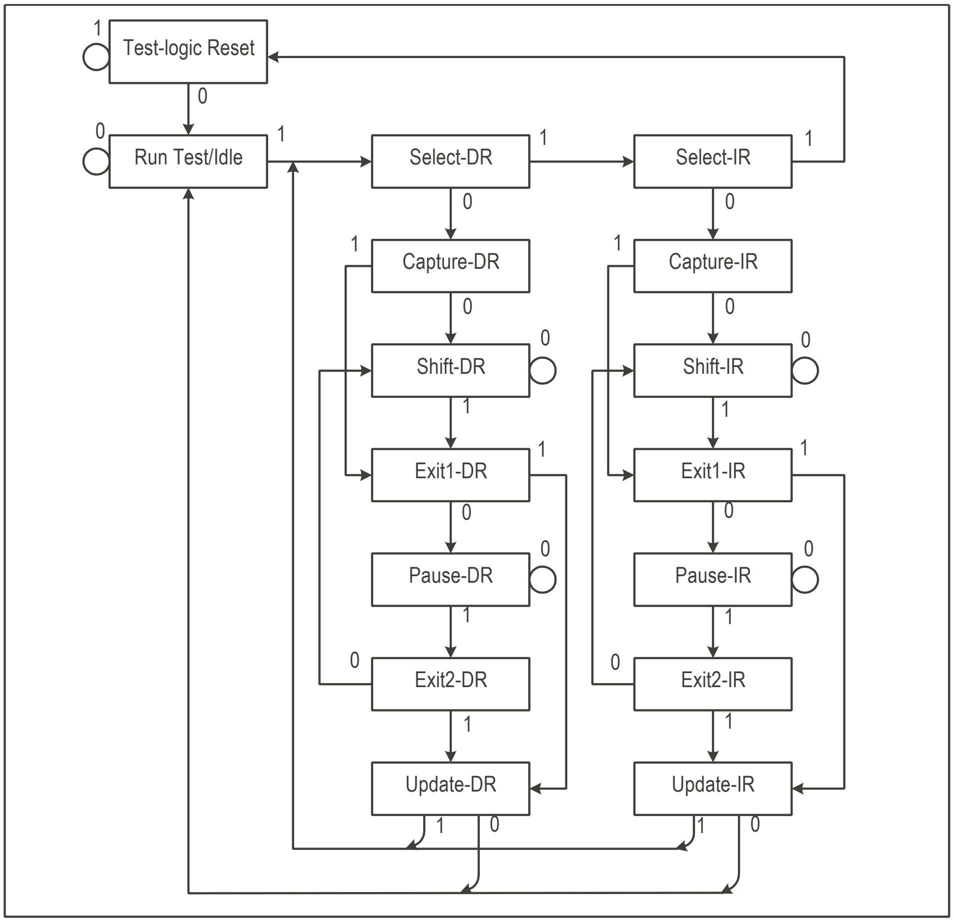
BIT No.	BIT SYMBOL	PIN SIGNAL	TYPE	COMMENTS
56	CSB	CS	I	
57	MODE0	MODE0	I	
58	TCLK5	TCLK5	I	
59	TDP5	TDP5	I	
60	TDN5	TDN5	I	
61	RC5	RC5	O	
62	RDP5	RDP5	O	
63	RDN5	RDN5	O	
64	HZEN5	N/A	-	Controls pin RDP5, RDN5 and RC5. When "0", the output are enabled on the pins. When "1", the pins are High-Z.
65	LOS5	LOS5	O	
66	TCLK4	TCLK4	I	
67	TDP4	TDP4	I	
68	TDN4	TDN4	I	
69	RC4	RC4	O	
70	RDP4	RDP4	O	
71	RDN4	RDN4	O	
72	HZEN4	N/A	-	Controls pin RDP4, RDN4 and RC4. When "0", the outputs are enabled on the pins. When "1", the pins are High-Z.
73	LOS4	LOS4	O	
74	OE	OE	I	
75	CLKE	CLKE	I	
76	LOS7	LOS7	O	
77	RDN7	RDN7	O	
78	RDP7	RDP7	O	
79	HZEN7	HZEN7	-	Controls pin RDP7, RDB7 and RC7. When "0", the outputs are enabled on the pins. When "1", the pins are High-Z.
80	RC7	RC7	0	
81	TDN7	TDN7	I	
82	TDP7	TDP7	I	
83	TCLK7	TCLK7	I	
84	LOS6	LOS6	O	
85	RDN5	RDN5	O	
86	RDP6	RDP6	O	
87	HZEN	N/A	-	Controls pin RDP6, RDN6 and RC6. When "0", the outputs are enabled on the pins. When "1", the pins are High-Z.
88	RC6	RC6	O	
89	TDN6	TDN6	I	
90	TDP6	TDP6	I	
91	TCLK6	TCLK6	I	
92	MCLK	MCLK	I	
93	MODE2	MODE2	I	
94	A4	A4	I	
95	A3	A3	I	
96	A2	A2	I	
97	A1	A1	I	
98	A0	A0	I	

TABLE 15 — TAP CONTROLLER STATE DESCRIPTION

STATE	DESCRIPTION
Test Logic Reset	In this state, the test logic is diabled. The device is set to normal operation. During initialization, the device initializes the instruction register with the IDCODE instruction. Regardless of the original state of the controller, the controller enters the Test-Logic-Reset state when the TMS input is held high for at least 5 rising edges of TCK. The controller remains in this state while TMS is high. The device processor automatically enters this state at power-up.
Run-Test/Idle	This is a controller state between scan operations. Once in this state, the controller remains in the state as long as TMS is held low. The instruction register and all registers retain their previous state. When TMS is high and a rising edge is applied to TCK, the controller moves to the Select-DR State.
Select-DR-Scan	This is a temporary controller state and the instruction does not change in this state. The test data register selected by the current instruction retains its previous state. If TMS is held low and a rising edge is applied to TCK when in this state, the controller moves into the Capture-DR state and a scan sequence test data register is initiated. If TMS is held high and a rising edge applied to TCK, the controller moves to the Select-IR-Scan State.
Capture-DR	In this state, the Boundary Scan Register captures input pin data if the current instruction is EXTEST or SAMPLE/PRELOAD. The instruction does not change in this state. The other data registers, which do not have parallel input, are not changed. When the TAP controller is in the state and a rising edge is applied to TCK, the controller enters the Exit1-DR state if TMS is high or the Shift-DR state if TMS is low.
Shift-DR	In this controller state, the test data register connected between TDI and TDO as a result of the current instruction shifts data on stage toward its serial output on each rising edge of TCK. The instruction does not change in this state. When the TAP controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-DR state if TMS is high or remains in the Shift-DR state if TMS is low.
Exit1-DR	This is a temporary state. When in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-DR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Pause-DR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Pause-DR	The pause state allows the test controller to temporarily halt the shifting of data through the test data register in the serial path between TDI and TDO. For example, this state could be used to allow the tester to reload its pin number memory from disk during application of a long test sequence. The test data register selected by the current instruction retains its previous value and the instructin does not change during this state. The controller remains in this state as long as TMS is low. When TMS goes high and a rising edge is applied to TCK, the controller moves to the Exit2-DR state.
Exit2-DR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-DR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Shift-DR state. The test dataregister selected by the current instruction retains its previous value and the instruction does not change during this state.
Update-DR	The Boundary Scan Register is provided with a latched parallel output to prevent changes while data is shifted in response to the EXTEST and SAMPLE/PRELOAD instructions. When the TAP controller is in this state and the Boundary Scan Register is selected, data is latched into the parallel output of this register from the shift path on the falling edge of TCK. The data held at the latched parallel output changes only in the state. All shift-register stages in the test data register selected by the current instruction retain thier previous value and the instruction does not change during this state.
Select-IR-Scan	This is temporary controller state. The test data register selected by the current instruction retains its previous state. If TMS is held low and a rising edge is applied to TCK when in this state, the controller moves into the Capture-IR state, and a scan sequence for the instruction register is initiated. If TMS is held high and a rising edge is applied to TCK, the controller moves to the Test-Logic-Reset state. The instruction does not change during this state.
Capture-IR	In this controller state, the shift register contained in the instruction register loads a fixed value of "100" on the rising edge of TCK. This supports fault-isolation of the board-level serial test data path. Data registers selected by the current instruction retain their value and the instruction does not changeduring this state. When the controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-IR state if TMS is held high, or the Shift-IR state if TMS is held low.
Shift-IR	In this state, the shift register contained in the instruction register is connected between TDI and TDO and shifts data one stage towards its serial output on each rising edge of TCK. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state and a rising edge is applied to TCK, the controller enters the Exit1-IR state if TMS is held high, or remains in the Shift-IR state if TMS is held low.

TABLE 15 — TAP CONTROLLER STATE DESCRIPTION (CONTINUED)

STATE	DESCRIPTION
Exit1-IR	This is temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-IR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Pause-IR state. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state.
Pause-IR	The pause state allows the test controller to temporarily halt the shifting of data through the instruction register. The test data register selected by the current instruction retains its previous value and the instruction does not change during this state. The controller remains in this state as long as TMS is low. When TMS goes high and a rising edge is applied to TCK, the controller moves to the Exit2-IR state.
Exit2-IR	This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-IR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Shift-IR state. The test data register selected by the current instruction retains its previous value and the instruction does not change this state.
Update-IR	The instruction shifted into the instruction register is latched into the parallel output from the shift-register path on the falling edge of TCK. When the new instruction has been latched, it becomes the current instruction. The test data registers selected by the current instruction retain their previous value.



6527 drw13

Figure 12. JTAG State Diagram

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Min.	Max.	Unit
VDDA, VDDD	Core Power Supply	-0.5	4.0	V
VDDIO0, VDDIO1	I/O Power Supply	-0.5	4.0	V
VDDT0-7	Transmit Power Supply	-0.5	7.0	V
Vin	Input Voltage, Any Digital Pin	GND -0.5	5.5	V
	Input Voltage, Any RTIP and RRING pin(1)	GND -0.5	VDDA+0.5 VDDA+0.5	V
	ESD Voltage, any pin(2)	2000		V
Iin	Transient latch-up current, any pin	100	mA	
	Input current, any digital pin(3)	-10	10	mA
	DC Input current, any analog pin(3)	±100	mA	
Pd	Maximum power dissipation in package		1.6	W
Ts	Storage Temperature	-65	+150	°C

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Exposure to absolute maximuim rating conditions for extended periods may affect device reliability.

Notes:

1. Referenced to ground
2. Human body model
3. Constant input current

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDDA, VDDD	Core Power Supply	3.13	3.3	3.47	V
VDDIO	I/O Power Supply	3.13	3.3	3.47	V
VDDT	Transmit Power Supply				
	3.3V	3.13	3.3	3.47	V
	5V	4.75	5.0	5.25	V
TA	Ambient Operating Temperature	-40	25	85	°C
R_L	Output Load at TTIP and TRING	25			Ω
I_{VDD}	Average Core Power Supply Current(1)		55	65	mA
I_{VDDIO}	I/O Power Supply Current (4)		15	25	mA
I_{VDDT}	Average Transmitter Power Supply Current, T1 mode(1,2,3)				
	50% ones density data:			230	mA
	100% ones density data:			440	

Note:

1. Maximum power and current consumption over the full operating temperature and power supply voltage range. Includes all channels.
2. Power consumption includes power absorbed by line load and external transmitter components.
3. T1 maximum values measured with maximum cable length (LEN = 111). Typical values measured with typical cable lengths (LEN = 101).
4. Digital output is driving 50pF load, digital input is within 10% of the supply rails.

POWER CONSUMPTION

Symbol	Parameter	LEN	Min.	Typ.	Max.[1,2]	Unit
	E1, 3.3V, 75Ω Load					
	50% ones density data:	000	-	662	-	mW
	100% ones density data:	000	-	1100	1177	
	E1, 3.3V, 120Ω Load					
	50% ones density data:	000	-	576	-	mW
	100% ones density data:	000	-	930	992	
	E1, 5.0V, 75Ω Load					
	50% ones density data:	000	-	910	-	mW
	100% ones density data:	000	-	1585	1690	
	E1, 5.0V, 120Ω Load					
	50% ones density data:	000	-	785	-	mW
	100% ones density data:	000	-	1315	1410	
	T1, 3.3V, 100Ω Load(3)					
	50% ones density data:	101	-	820	-	mW
	100% ones density data:	111	-	1670	1792	
	T1, 5.0V, 100Ω Load(3)					
	50% ones density data:	101	-	1185	-	mW
	100% ones density data:	111	-	2395	2670	

Notes:

1. Maximum power and current consumption over the full operating temperature and power supply voltage range. Includes all channels.
2. Power consumption includes power absorbed by line load and external transmitter components.
3. T1 maximum values measured with maximum cable lengths (LEN = 111). Typical values measured with typical cable lengths (LEN = 101).

DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level Voltage MODE2, Dn pins All other digital inputs pins			1/3 VDDIO-0.2 0.8	V
V_{IM}	Input Mid Level Voltage MODE2, Dn pins	1/3 VDDIO+0.2	1/2 VDDIO	2/3 VDDIO-0.2	V
V_{IH}	Input High Voltage MODE2, Dn pins All other digital inputs pins	2/3 VDDIO+0.2 2.0			V
V_{OL}	Output Low Level Voltage(1) (Iout=1.6mA)			0.4	V
V_{OH}	Output High Level Voltage(1) (Iout=400mA)	2.4		VDDIO	V
V_{MA}	Analog Input Quiescent Voltage (RTIP, RRING pin while floating)	1.33	1.4	1.47	V
I_H	Input High Level Current (MODE2, Dn pin)			50	µA
I_L	Input Low Level Current (MODE2, Dn pin)			50	µA
I_I	Input Leakage Current TMS, TDI, $\overline{\text{TRST}}$ All other digital input pins	-10		50 10	µA µA
I_{ZL}	High-Z Leakage Current	-10		10	µA
Z_{OH}	Output High Impedance on (TTIP, TRING pins)	150			KΩ

Note:

1. Output drivers will output CMOS logic levels into CMOS loads.

TRANSMITTER CHARACTERISTICS

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{O-P}	Output pulse amplitudes[1]					
	E1, 75Ω load		2.14	2.37	2.6	V
	E1, 120Ω load		2.7	3.0	3.3	V
	T1, 100Ω load		2.4	3.0	3.6	V
V_{O-S}	Zero (space) level					
	E1, 75Ω load		-0.237		0.237	V
	E1, 120Ω load		-0.3		0.3	V
	T1, 100Ω load		-0.15		0.15	C
	Transmit amplitude variation with supply		-1		+1	%
	Difference between pulse sequences for 17 consecutive pulses				200	mV
T_{PW}	Output Pulse Width at 50% of nominal amplitude					
	E1:		232	244	256	ns
	T1:		338	350	362	ns
	Ratio of the amplitude of Positive and Negative Pulses at the center of the pulse interval		0.95		1.05	
RTX	Transmit Return Loss[2]					
	E1, 75Ω	51 KHz - 102 KHz	15			dB
		102 KHz - 2.048 MHz	15			dB
		2.048 MHz - 3.072 MHz	15			dB
	E1, 120Ω	51 KHz - 102 KHz	15			dB
		102 KHZ - 2.048 MHz	15			dB
		2.048 MHz - 3.072 MHz	15			dB
	T1	51 KHz - 102 KHz	15			dB
	(VDDT=5V)	102 KHz - 2.048 MHz	15			dB
		2.048 MHz - 3.072 MHz	15			dB
Td	Transmit path delay					
	Dual Rail		3			U.I.
I_{SC}	Line Short Circuit Current [3]			150		mA

Notes:

1. E1: measured at the line output ports; T1: measured at the DSX.
2. Test at IDT82V2048L evaluation board.
3. Measured at 2x9 5Ω series resistors and 1:2 transformer.

DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
ATT	Permissible Cable Attenuation (E1:@1024KHz, T1:@772KHz)			15	dB
IA	Input Amplitude	0.1		0.8	Vp
SIR	Signal to Intereference Ratio Margin (1)	-14			dB
SRE	Data decision threshold (reference to peak input voltage)		50		dB
	Data slicer threshold		150		mV
	Analog loss of signal (2)				
	Threshold:		310		mV
	Hysteresis:		230		mV
	Allowable consecutive zeros before LOS				
	E1, G.775:		32		
	E1, ETSI200233:		2048		
	T1, T1.231-1993		175		
	LOS reset				
	Clock recovery mode	12.5			% ones
JRX P-P	Peak to Peak Intrinsic Receive Jitter (JA disabled)				
	E1 (wide band):			0.0625	U.I.
	T1 (wide band):			0.0625	U.I
ZDM	Receiver Differential Input Impedance		120		KΩ
ZCM	Receiver Common Mode Input Impedance to GND	10			KΩ
RRX	Receive Return Loss				
	51 KHz - 102 KHz	20			dB
	102 KHz - 2.048 MHz	20			dB
	2.018 MHz - 3.072 MHz	20			dB
	Receive path delay				
	Dual rail		3		U.I.

Notes:

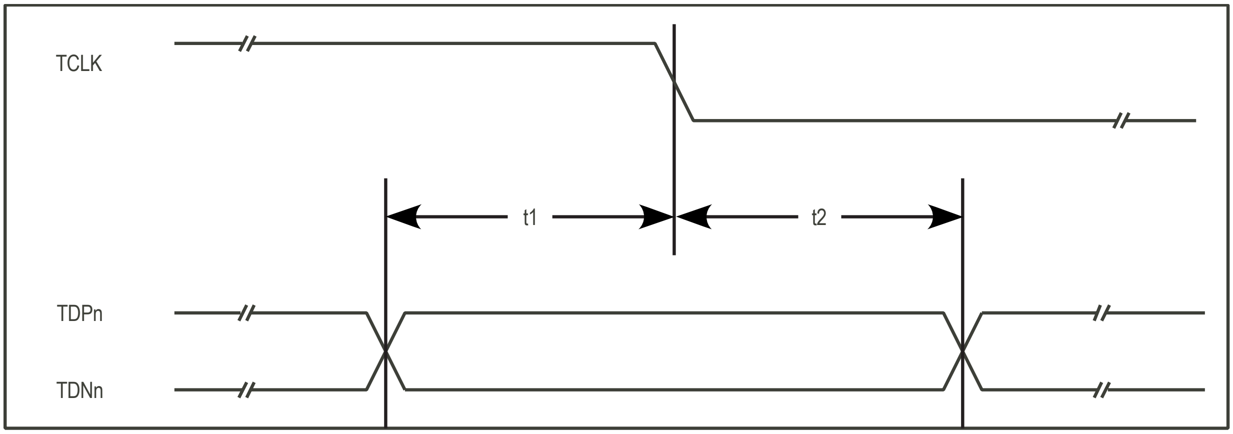
1. E1: per G.703, O.151 @6dB cable attenuation. T1: @655ft. of 22ABAM cable.
2. The test circuit for this parameter is shown in Figure 6. The analog signal is measured on the Receiver line before the transformer (port A and port B in Figure 6). And the receive line is a T1/E1 cable simulator.

TRANSCEIVER TIMING CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
	MCLK frequency				
	E1:	2.048		MHz	
	T1:	1.544			
	MCLK tolerance	-100		100	ppm
	MCLK Duty Cycle	40		60	%
Transmit path					
	TCLK frequency				
	E1:		2.048		MHz
	T1:		1.544		
	TCLK tolerance	-50		+50	ppm
	TCLK Duty Cycle	10		90	%
t1	Transmit Data Setup Time	40			ns
t2	Transmit Data Hold Time	40			ns
	Delay time of OE low to driver High-Z		1	ms	
	Delay time of TCLK low to driver High-Z	40	44	48	µs
Receive path					
	Clock Recovery capture range (1) E1		+/-80		ppm
	T1		+/-180		
	RCn Duty Cycle(2)	40	50	60	%
t4	RCn pulse width (2)				
	E1:	457	488	519	ns
	T1:	607	648	689	
t5	RCn pulse width low time				
	E1:	203	244	285	ns
	T1:	259	324	389	
t6	RCn pulse width high time				
	E1:	203	244	285	ns
	T1:	259	324	389	
	Rise/Fall Time (3)				
t7	Receive Data Setup Time				
	E1:	200	244		ns
	T1:	200	324		
t8	Receive Data Hold Time				
	E1:	200	244		ns
	T1:	200	324		
t9	RDN/RDP pulse width (MCLK = H) (4)				
	E1:	200	244		ns
	T1:	300	324		

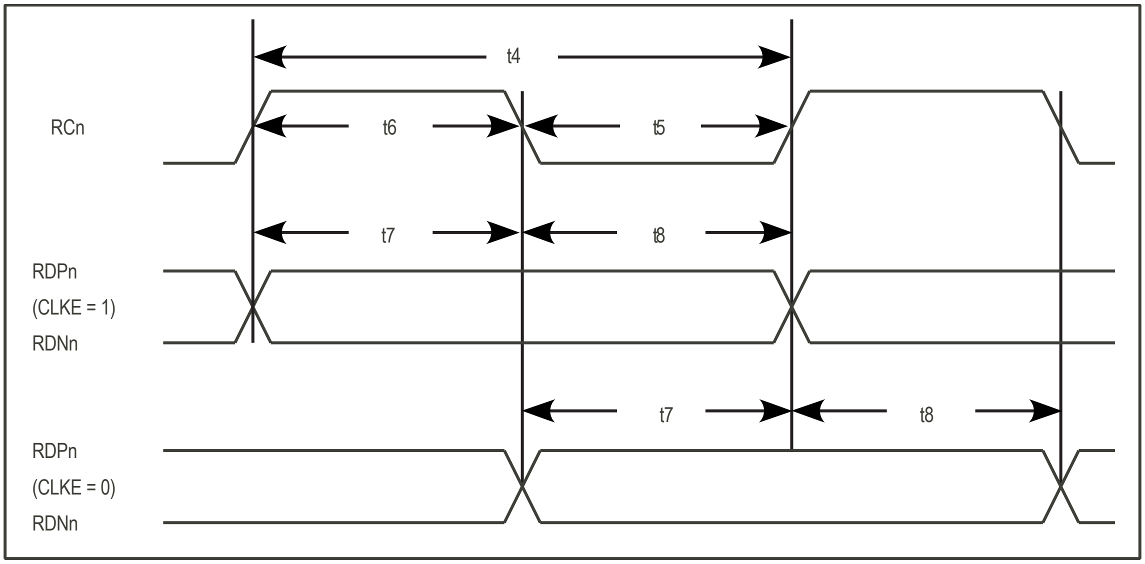
Notes:

1. Relative to nominal frequency, MCLK =+/- 100ppm.
2. RCn duty cycle widths will vary depending on extent of received pulse jitter displacement. Maximum and minimum RCn duty cycles are for worst case jitter conditions (0.2UI displacement for E1 per ITU G.823)
3. For all digital outputs. C load = 15 pF.
4. Clock recovery is disabled in this mode.



6527 drw14

Figure 13. Transmit System Interface Timing

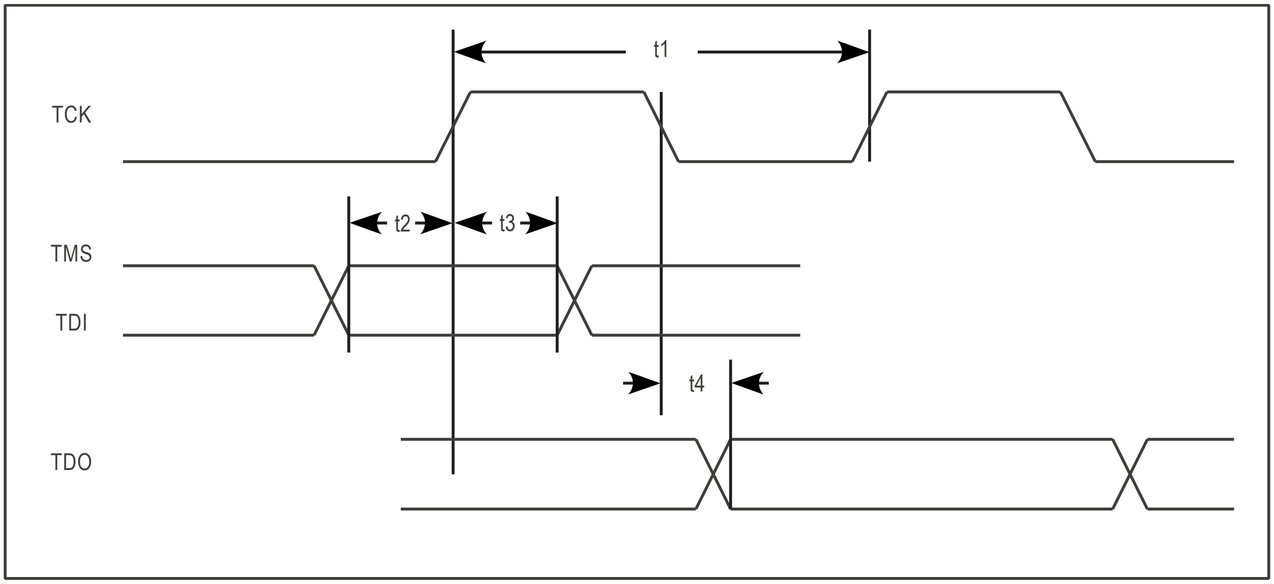


6527 drw15

Figure 14. Receive System Interface Timing

JTAG TIMING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t1	TCK Period	200			ns	
t2	TMS to TCK Setup Time TDI to TCK Setup Time	50			ns	
t3	TCK to TMS Hold Time TCK to TDI Hold Time	50			ns	
t4	TCK to TDO Delay Time			100	ns	



6527 drw16

Figure 15. JTAG Interface Timing

PARALLEL HOST INTERFACE TIMING CHARACTERISTICS

INTEL MODE READ TIMING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t1	Active $\overline{\text{RD}}$ Pulse Width	90			ns	Note 1
t2	Active $\overline{\text{CS}}$ to Active $\overline{\text{RD}}$ Setup Time	0			ns	
t3	Inactive $\overline{\text{RD}}$ to Inactive $\overline{\text{CS}}$ Hold Time	0			ns	
t4	Valid Address to Inactive ALE Setup Time (in Multiplexed Mode)	5			ns	
t5	Invalid $\overline{\text{RD}}$ to Address Hold Time (in Non-Multiplexed Mode)	0			ns	
t6	Active $\overline{\text{RD}}$ to Data Output Enable Time	7.5		15	ns	
t7	Inactive $\overline{\text{RD}}$ to Data High-Z Delay Time	7.5		15	ns	
t8	Active $\overline{\text{CS}}$ to RDY delay time	6		12	ns	
t9	Inactive $\overline{\text{CS}}$ to RDY High-Z Delay Time	6		12	ns	
t10	Inactive $\overline{\text{RD}}$ to Inactive $\overline{\text{INT}}$ Delay Time			20	ns	
t11	Address Latch Enable Pulse Width (in Multiplexed Mode)	10			ns	
t12	Address Latch Enable to $\overline{\text{RD}}$ Setup Time (in Multiplexed Mode)	0			ns	
t13	Address Setup Time to Valid Data Time (in Non-Multiplexed Mode) Inactive ALE to Valid Data Time (in Multiplexed Mode)	18		32	ns	
t14	Inactive $\overline{\text{RD}}$ to Active RDY Delay Time	10		15	ns	
t15	Active $\overline{\text{RD}}$ to Active RDY Delay Time	30		85	ns	
t16	Inactive ALE to Address Hold Time (in Multiplexed Mode)	5			ns	

NOTE:

1. The t1 is determined by the start time of the valid data when the RDY signal is not used.

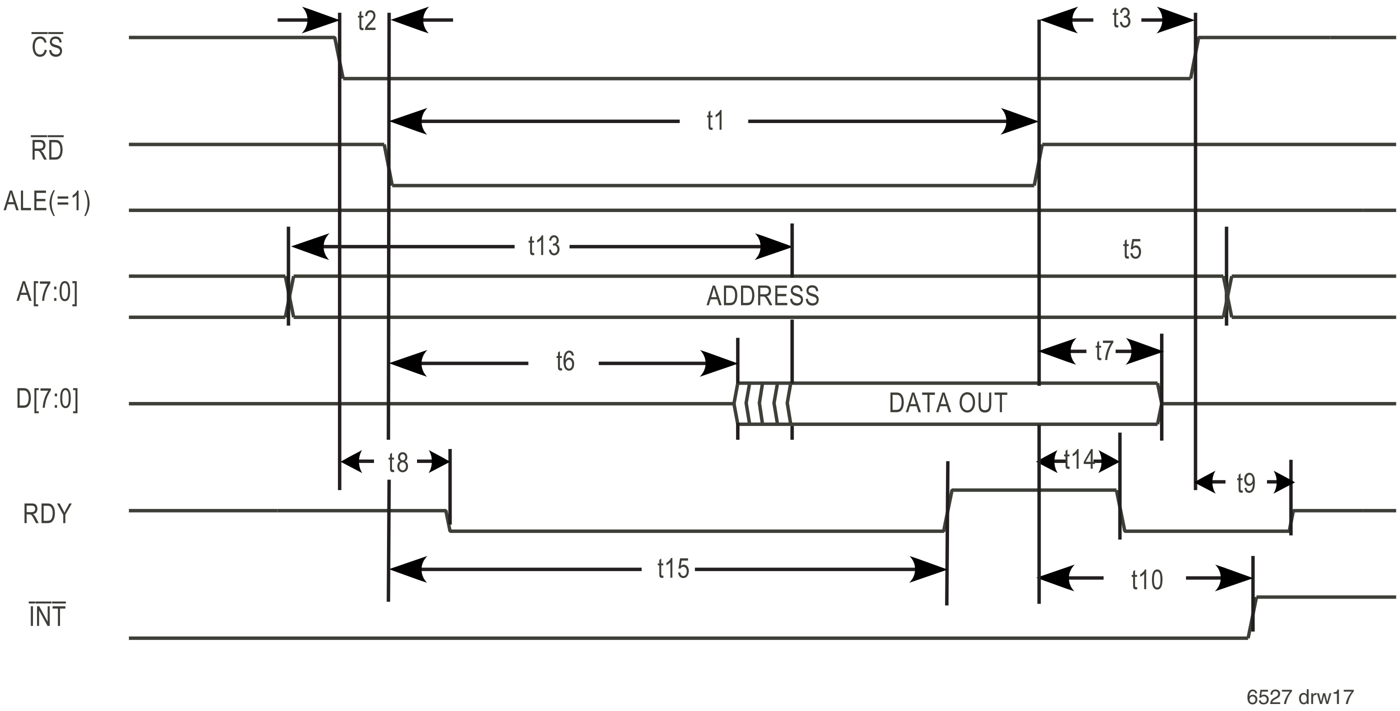


Figure 16. Non-Multiplexed Intel Mode Read Timing

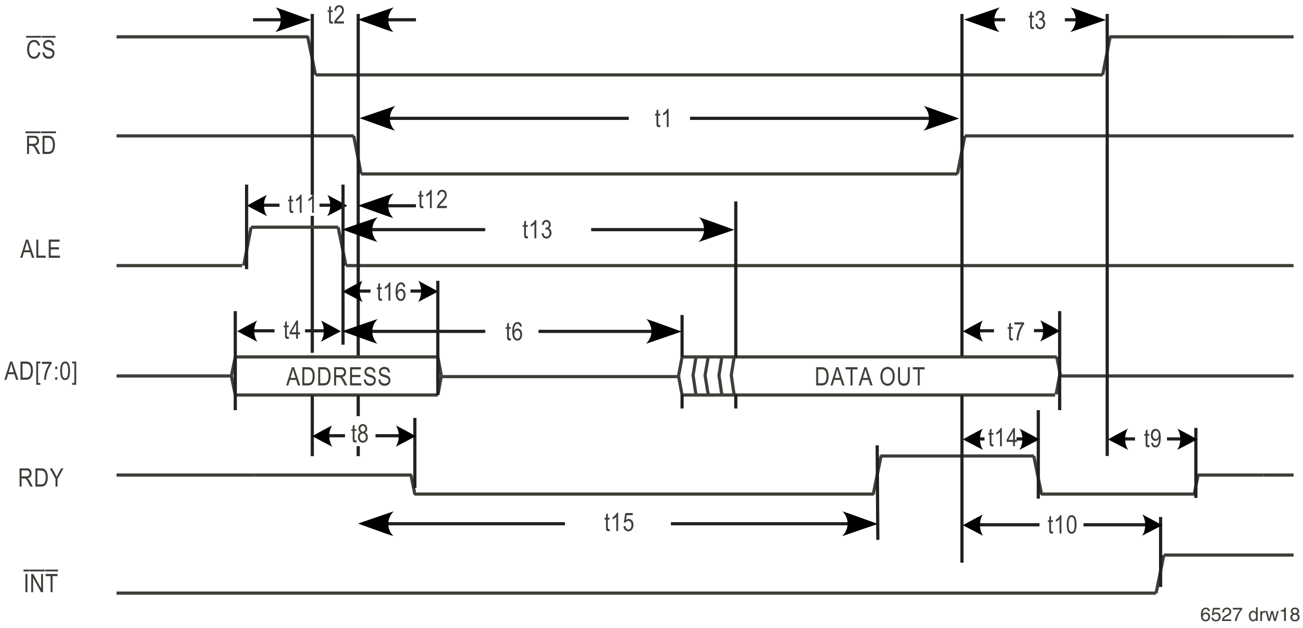


Figure 17. Multiplexed Intel Mode Read Timing

INTEL MODE WRITE TIMING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t1	Active $\overline{WR}$ Pulse Width	90			ns	Note 1
t2	Active $\overline{CS}$ to Active $\overline{WR}$ Setup Time	0			ns	
t3	Inactive $\overline{WR}$ to Inactive $\overline{CS}$ Hold Time	0			ns	
t4	Valid Address to Latch Enable Setup Time (in Multiplexed Mode)	5			ns	
t5	Invalid $\overline{WR}$ to Address Hold Time (in Non-Multiplexed Mode)	2			ns	
t6	Valid Data to Inactive $\overline{WR}$ Setup Time	5			ns	
t7	Inactive $\overline{WR}$ to Data Hold Time	10			ns	
t8	Active $\overline{CS}$ to inactive RDY Delay Time	6		12	ns	
t9	Active $\overline{WR}$ to Active RDY Delay Time	30		85	ns	
t10	Inactive $\overline{WR}$ to Inactive RDY Delay Time	10		15	ns	
t11	Invalid $\overline{CS}$ to RDY High-Z Delay Time	6		12	ns	
t12	Address Latch Enable Pulse Width (in Multiplexed Mode)	10			ns	
t13	Inactive ALE to $\overline{WR}$ Setup Time (in Multiplexed Mode)	0			ns	
t14	Inactive ALE to Address Hold Time (in Multiplexed Mode)	5			ns	
t15	Address Setup Time to Inactive $\overline{WR}$ time (In Non-Multiplexed Mode)	5			ns	

NOTE:

1. The t1 can be 15ns when RDY signal is not used.

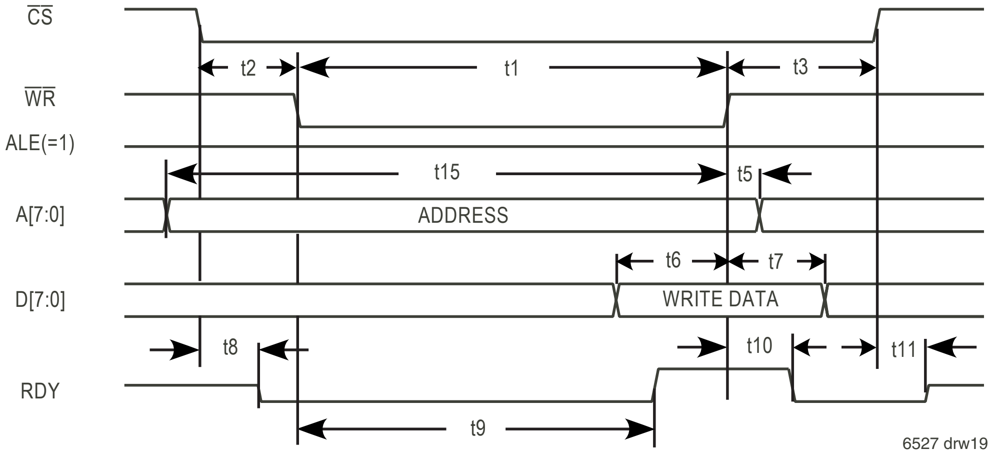


Figure 18. Non-Multiplexed Intel Mode Write Timing

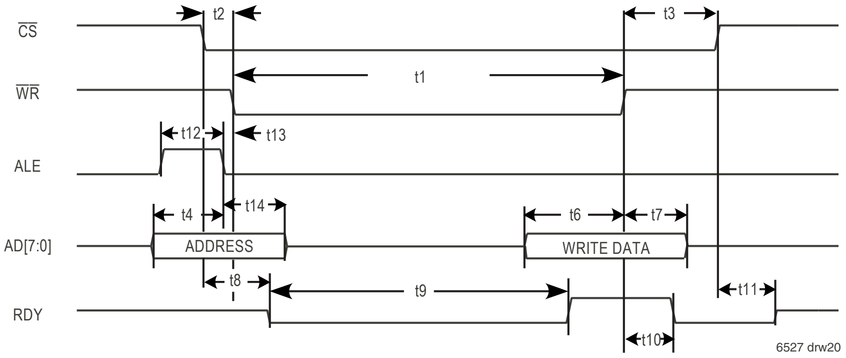


Figure 19. Multiplexed Intel Mode Write Timing

MOTOROLA MODE READ TIMING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t1	Active $\overline{DS}$ Pulse Width	90			ns	Note 1
t2	Active $\overline{CS}$ to Active $\overline{DS}$ Setup Time	0			ns	
t3	Inactive $\overline{DS}$ to Inactive $\overline{CS}$ Hold Time	0			ns	
t4	Valid R/$\overline{W}$ to Active $\overline{DS}$ Setup Time	0			ns	
t5	Inactive $\overline{DS}$ to R/$\overline{W}$ Hold Time	0.5			ns	
t6	Valid Address to Active $\overline{DS}$ Setup Time (in Non-Multiplexed Mode) Valid Address to $\overline{AS}$ Setup Time (in Multiplexed Mode)	5			ns	
t7	Active $\overline{DS}$ to Address Hold Time (in Non-Multiplexed Mode) Active $\overline{AS}$ to Address Hold Time (in Multiplexed Mode)	10			ns	
t8	Active $\overline{DS}$ to Data Valid Delay Time (in Non-Multiplexed Mode) Active $\overline{AS}$ to Data Valid Delay Time (in Multiplexed Mode)	20		35	ns	
t9	Active $\overline{DS}$ to Data Output Enable Time	7.5		15	ns	
t10	Inactive $\overline{DS}$ to Data High-Z Delay Time	7.5		15	ns	
t11	Active $\overline{DS}$ to Active $\overline{ACK}$ Delay Time	30		85	ns	
t12	Inactive $\overline{DS}$ to Inactive $\overline{ACK}$ Delay Time	10		15	ns	
t13	Inactive $\overline{DS}$ to Invalid $\overline{INT}$ Delay Time			20	ns	
t14	Active $\overline{AS}$ to Active $\overline{DS}$ Setup Time (in Multiplexed Mode)	5			ns	

NOTE:

1. The t1 is determined by the start time of the valid data when the $\overline{ACK}$ signal is not used.

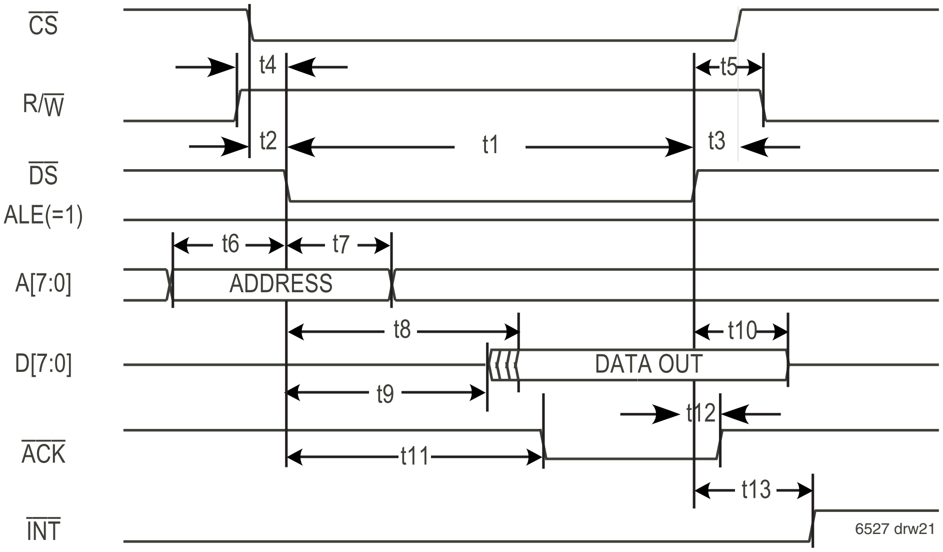


Figure 20. Non-Multiplexed Motorola Mode Read Timing

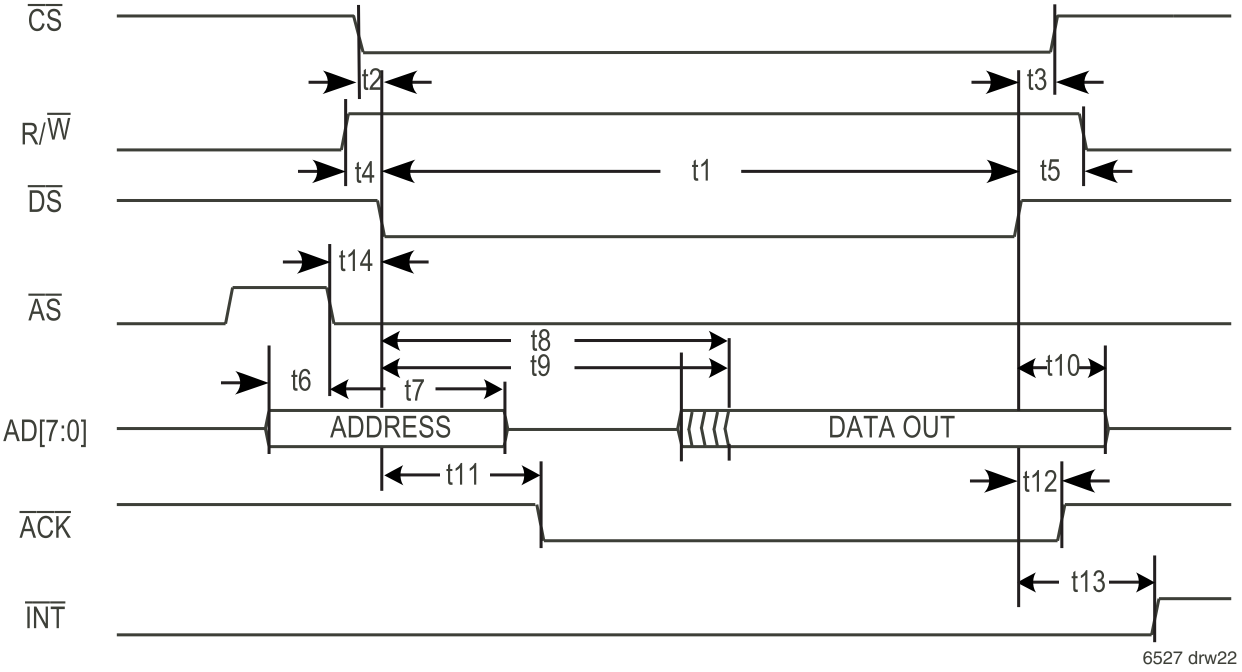


Figure 21. Multiplexed Motorola Mode Read Timing

MOTOROLA MODE WRITE TIMING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t1	Active $\overline{DS}$ Pulse Width	90			ns	Note 1
t2	Active $\overline{CS}$ to Active $\overline{DS}$ Setup Time	0			ns	
t3	Inactive $\overline{DS}$ to Inactive $\overline{CS}$ Hold Time	0			ns	
t4	Valid R/$\overline{W}$ to Active $\overline{DS}$ Setup Time	10			ns	
t5	Inactive $\overline{DS}$ to R/$\overline{W}$ Hold Time	0			ns	
t6	Valid Address to Active $\overline{DS}$ Setup Time (in Non-Multiplexed Mode) Valid Address to $\overline{AS}$ Setup Time (in Multiplexed Mode)	10			ns	
t7	Valid $\overline{DS}$ to Address Hold Time (in Non-Multiplexed Mode) Valid $\overline{AS}$ to Address Hold Time (in Multiplexed Mode)	10			ns	
t8	Valid $\overline{DS}$ to Inactive $\overline{DS}$ Setup Time	5			ns	
t9	Inactive $\overline{DS}$ to Data Hold Time	10			ns	
t10	Active $\overline{DS}$ to Active $\overline{ACK}$ Delay Time	30		85	ns	
t11	Inactive $\overline{DS}$ to Inactive $\overline{ACK}$ Delay Time	10		15	ns	
t12	Active $\overline{AS}$ to Active $\overline{DS}$ (in Multiplexed Mode)	0			ns	
t13	Inactive $\overline{DS}$ to Inactive $\overline{AS}$ Hold Time (in Multiplexed Mode)	15			ns	

NOTE:

1. The t1 can be 15ns when the $\overline{ACK}$ signal is not used.

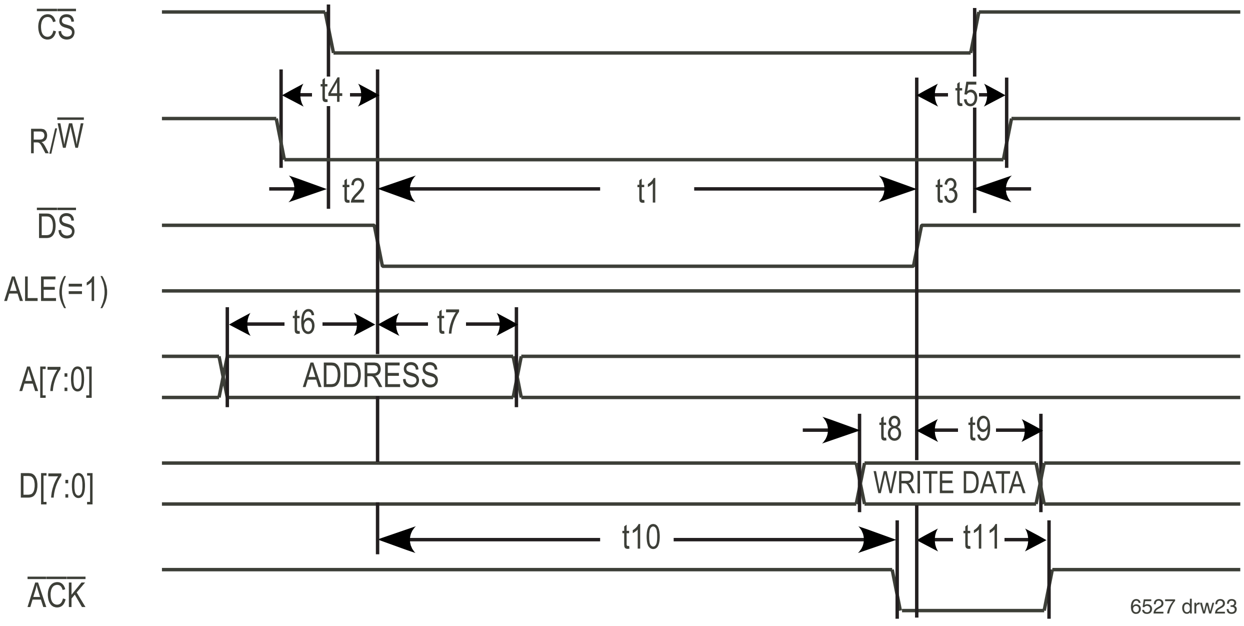


Figure 21. Non-Multiplexed Motorola Mode Write Timing

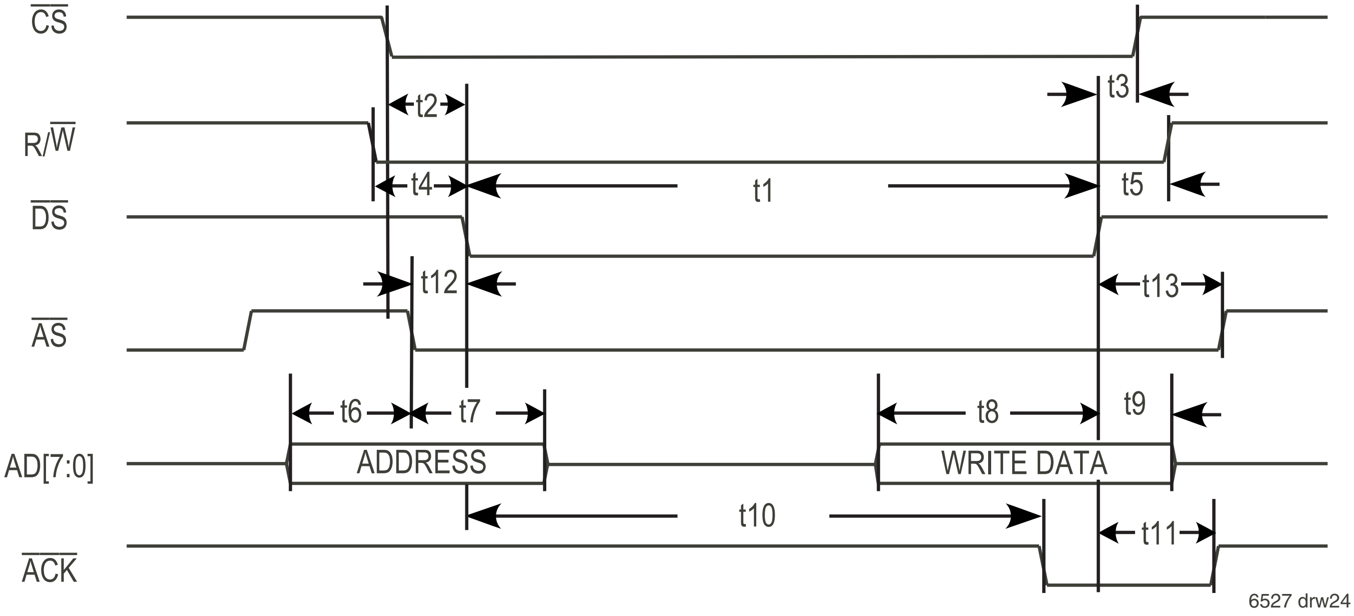


Figure 23. Multiplexed Motorola Mode Write Timing

SERIAL HOST INTERFACE TIMING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Comments
t1	SCLK High Time	25			ns	
t2	SCLK Low Time	25			ns	
t3	Active $\overline{CS}$ to SCLK Setup Time	10			ns	
t4	Last SCLK Hold Time to Inactive $\overline{CS}$ Time	50			ns	
t5	$\overline{CS}$ Idle Time	50			ns	
t6	SDI to SCLK Setup Time	5			ns	
t7	SCLK to SDI Hold Time	5			ns	
t8	Rise/Fall Time (any pin)			100	ns	
t9	SCLK Rise and Fall Time			50	ns	
t10	SCLK to SDO Valid Delay Time		100		ns	
t11	SCLK Falling Edges to SDO High-Z Hold Time (CLKE = 0) $\overline{CS}$ Rising Edges to SDO High-Z Hold Time (CLKD = 1)		100		ns	

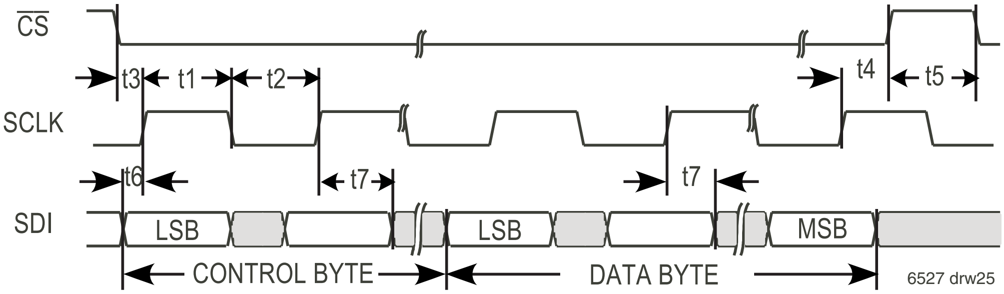


Figure 24. Serial Interface Writing Timing

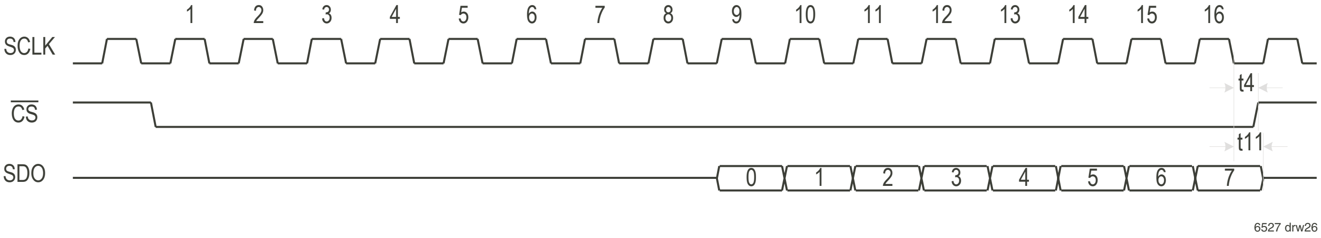


Figure 25. Serial Interface Read Timing with CLKE = 0

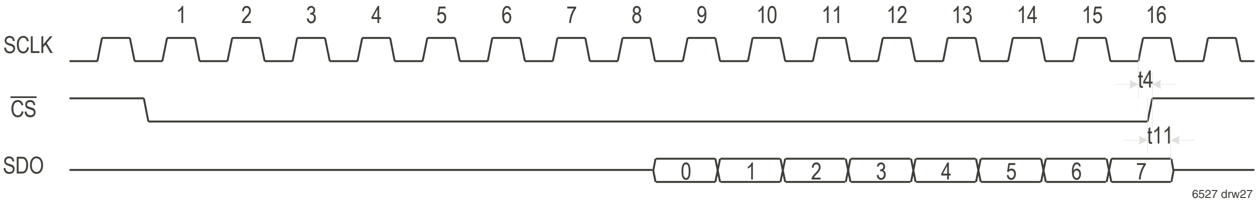
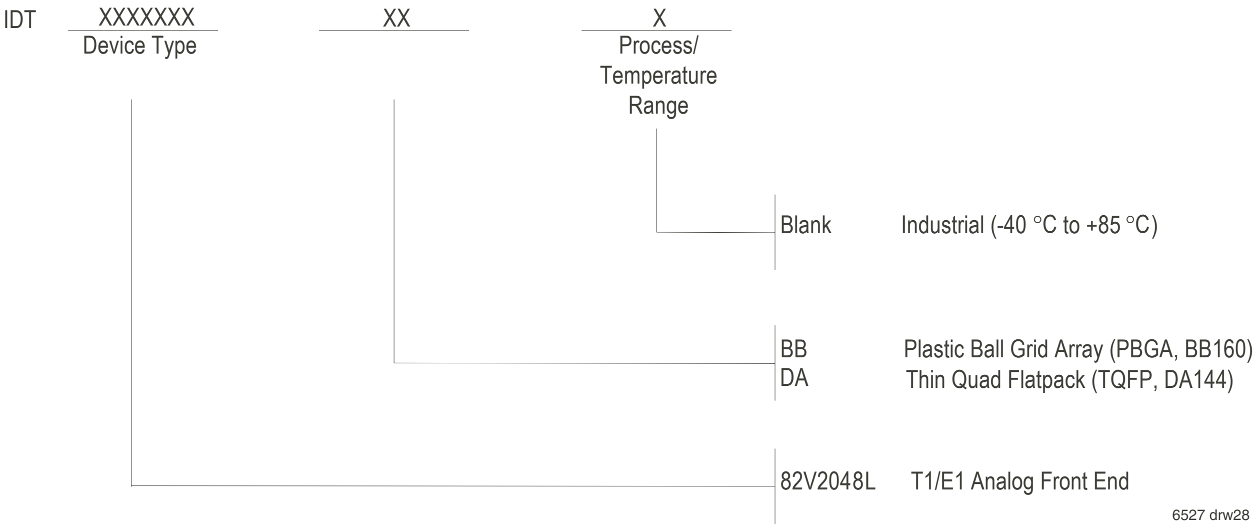


Figure 26. Serial Interface Read Timing with CLKE = 1

ORDERING INFORMATION



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