AS5163

12-Bit Automotive Angle Position Sensor

1 General Description

The AS5163 is a contactless magnetic angle position sensor for accurate angular measurement over a full turn of 360°. A sub range can be programmed to achieve the best resolution for the application. It is a system-on-chip, combining integrated Hall elements, analog front-end, digital signal processing and best in class automotive protection features in a single device.

To measure the angle, only a simple two-pole magnet, rotating over the center of the chip, is required. The magnet may be placed above or below the IC.

The absolute angle measurement provides instant indication of the magnet's angular position with a resolution of 0.022° = 16384 positions per revolution. According to this resolution the adjustment of the application specific mechanical positions are possible. The angular output data is available over a 12-bit PWM signal or 12-bit ratiometric analog output.

The AS5163 operates at a supply voltage of 5V and the supply and output pins are protected against overvoltage up to +27V. In addition, the supply pins are protected against reverse polarity up to -18V.

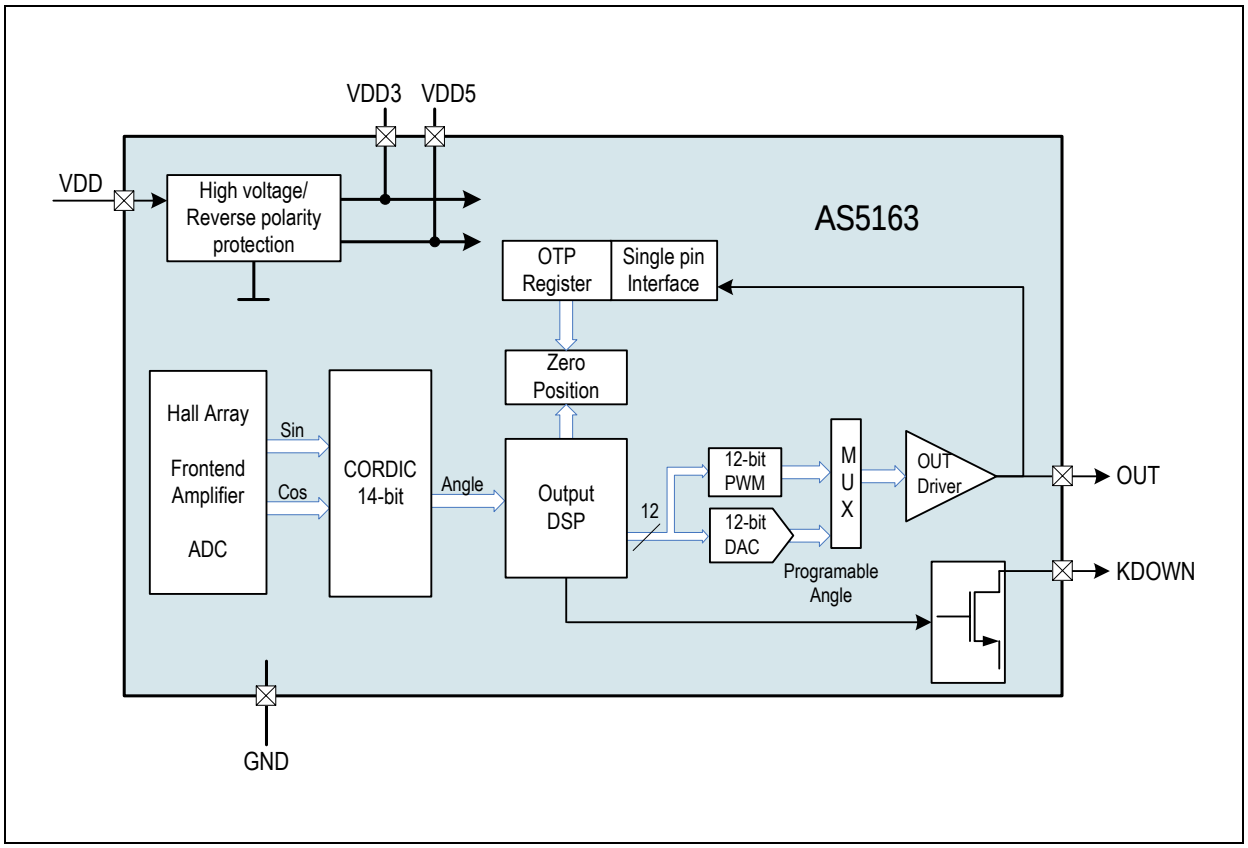
2 Key Features

- 360° contactless high resolution angular position encoding
- User programmable start and end point of the application region
- User programmable clamping levels and programming of the transition point
- Powerful analog output
  - Short circuit monitor
  - High driving capability for resistive and capacitive loads
- Wide temperature range: -40°C to +150°C
- Small Pb-free package: 14-pin TSSOP
- Broken GND and VDD detection over a wide range of different load conditions

3 Applications

The AS5163 is ideal for automotive applications like Throttle and valve position sensing, Gearbox position sensor, Headlight position control, Torque sensing, Pedal position sensing and non contact Potentiometers.

Figure 1. AS5163 Block Diagram



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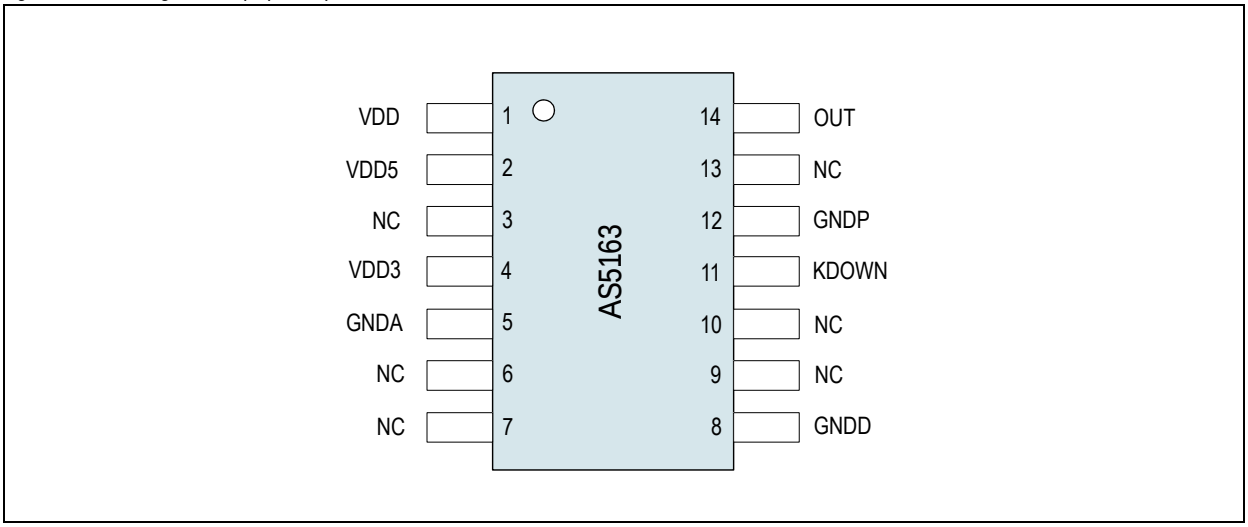
4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1 provides the description of each pin of the standard TSSOP14 package (14-Lead Thin Shrink Small Outline Package) (see Figure 2).

Table 1. Pin Descriptions

Pin Number	Pin Name	Pin Type	Description
1	VDD	Supply pin	**Positive supply pin.** This pin is high voltage protected.
2	VDD5	Supply pin	**4.5V- Regulator output, internally regulated from VDD.** This pin needs an external ceramic capacitor of minimum 2.2µF.
3	NC	DIO/AIO multi purpose pin	**Test pin for fabrication.** Connected to ground in the application board.
4	VDD3	Supply pin	**3.45V- Regulator output, internally regulated from VDD5.** This pin needs an external ceramic capacitor of minimum 2.2µF.
5	GNDA	Supply pin	**Analog ground pin.** Connected to ground in the application board.
6	NC	DIO/AIO multi purpose pin	**Test pin for fabrication.** Connected to ground in the application board.
7	NC	DIO/AIO multi purpose pin	**Test pin for fabrication.** Open in the application.
8	GNDD	Supply pin	**Digital ground pin.** Connected to ground in the application board.
9	NC	DIO/AIO multi purpose pin	**Test pins for fabrication.** Connected to ground in the application board.
10	NC	DIO/AIO multi purpose pin	
11	KDOWN	Digital output open drain	**Additional output pin with Kick down functionality.** This pin can be used for a compare function including a hysteresis. An open drain configuration is used. If the internal angle is above a programmable threshold, then the output is switched to low. Below the threshold the output is high using a pull-up resistor.
12	GNDP	Supply pin	**Analog ground pin.** Connected to ground in the application board.
13	NC	DIO/AIO multi purpose pin	**Test pin for fabrication.** Connected to ground in the application board.
14	OUT	DIO/AIO multi purpose pin	**Output pin.** This pin is used for the analog output or digital PWM signal. In addition, this pin is used for programming of the device.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 5 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
V_{DD}	DC supply voltage at pin VDD Overvoltage	-18	27	V	No operation
V_{OUT}	Output voltage OUT	-0.3	27	V	permanent
V_{KDOWN}	Output voltage KDOWN	-0.3	27	V	
VDD3	DC supply voltage at pin VDD3	-0.3	5	V	
VDD5	DC supply voltage at pin VDD5	-0.3	7	V	
I_{scr}	Input current (latchup immunity)	-100	100	mA	Norm: JEDEC 78
Electrostatic Discharge					
ESD	Electrostatic discharge		±4	kV	Norm: MIL 883 E method 3015 This value is applicable to pins VDD, GND, OUT, and KDOWN. All other pins ±2 kV.
Temperature Ranges and Storage Conditions					
T_{strg}	Storage temperature	-55	+150	ºC	Min -67ºF; Max +257ºF
T_{Body}	Body temperature (Lead-free package)		260	ºC	t=20 to 40s, The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"*. The lead finish for Pb-free leaded packages is matte tin (100% Sn).
H	Humidity non-condensing	5	85	%	
	Moisture Sensitive Level	3			Represents a maximum floor life time of 168h

6 Electrical Characteristics

6.1 Operating Conditions

In this specification, all the defined tolerances for external components need to be assured over the whole operation conditions range and also over lifetime.

T_{AMB} = -40 to +150ºC, VDD = +4.5V to +5.5V, CLREG5 = 2.2µF, CLREG3 = 2.2µF, R_{PU} = 1KΩ, R_{PD} = 1KΩ to 5.6KΩ (Analog only), C_{LOAD} = 0 to 42nF, R_{PUKDWN} = 1KΩ to 5.6KΩ, C_{LOAD_KDWN} = 0 to 42nF, unless otherwise specified. A positive current is intended to flow into the pin.

Table 3. Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{AMB}	Ambient temperature	-40ºF…+302ºF	-40		+150	ºC
I_{supp}	Supply current	Lowest magnetic input field			20	mA

6.2 Magnetic Input Specification

T_{AMB} = -40 to +150ºC, VDD = 4.5 to 5.5V (5V operation), unless otherwise noted.

Two-pole cylindrical diametrically magnetized source:

Table 4. Magnetic Input Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Units
B_{pk}	Magnetic input field amplitude	Required vertical component of the magnetic field strength on the die's surface, measured along a concentric circle with a radius of 1.1mm	30		70	mT
B_{off}	Magnetic offset	Constant magnetic stray field			±10	mT
	Field non-linearity	Including offset gradient			5	%

6.3 Electrical System Specifications

TAMB = -40 to +150ºC, VDD = 4.5 - 5.5V (5V operation), Magnetic Input Specification, unless otherwise noted.

Table 5. Electrical System Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RES	Resolution Analog and PWM Output	Angular operating range ≥ 90ºC			12	bit
INL_{opt}	Integral non-linearity (optimum) 360 degree full turn	Maximum error with respect to the best line fit. Centered magnet without calibration, TAMB=25ºC			±0.5	deg
INL_{temp}	Integral non-linearity (optimum) 360 degree full turn	Maximum error with respect to the best line fit. Centered magnet without calibration, TAMB = -40 to +150ºC			±0.9	deg
INL	Integral non-linearity 360 degree full turn	Best line fit = (Err_{max} – Err_{min}) / 2 Over displacement tolerance with 6mm diameter magnet, without calibration, TAMB = -40 to +150ºC. **Note:** This parameter is a system parameter and is dependant on the selected magnet.		±1.4		deg
TN	Transition noise	1 sigma; **Note:** The noise performance is dependent on the programming of the output characteristic.		0.06		Deg RMS
$VDD5_{LowTH}$	Undervoltage lower threshold	VDD5 = 5V	3.1	3.4	3.7	V
$VDD5_{HighTH}$	Undervoltage higher threshold		3.6	3.9	4.2	
t_{PwrUp}	Power-up time	Fast mode, times 2 in slow mode			10	ms
t_{delay}	System propagation delay absolute output: delay of ADC, DSP and absolute interface	Fast mode, times 2 in slow mode			100	µs

Note: The INL performance is specified over the full turn of 360 degrees. An operation in an angle segment increases the accuracy. A two point linearization is recommended to achieve the best INL performance for the chosen angle segment.

6.4 Timing Characteristics

Table 6. Timing Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
FRCOT	Internal Master Clock		4.05	4.5	4.95	MHz
TCLK	Interface Clock Time	TCLK = 1/ FRCOT	202	222.2	247	ns
TDETWD	WatchDog error detection time				12	ms

7 Detailed Description

The AS5163 is manufactured in a CMOS process and uses a spinning current Hall technology for sensing the magnetic field distribution across the surface of the chip.

The integrated Hall elements are placed around the center of the device and deliver a voltage representation of the magnetic field at the surface of the IC.

Through Sigma-Delta Analog / Digital Conversion and Digital Signal-Processing (DSP) algorithms, the AS5163 provides accurate high-resolution absolute angular position information. For this purpose, a Coordinate Rotation Digital Computer (CORDIC) calculates the angle and the magnitude of the Hall array signals.

The DSP is also used to provide digital information at the outputs that indicate movements of the used magnet towards or away from the device's surface.

A small low cost diametrically magnetized (two-pole) standard magnet provides the angular position information.

The AS5163 senses the orientation of the magnetic field and calculates a 14-bit binary code. This code is mapped to a programmable output characteristic. The type of output is programmable and can be selected as PWM or analog output. This signal is available at the pin 14 (OUT).

The analog and PWM output can be configured in many ways. The application angular region can be programmed in a user friendly way. The start angle position T1 and the end point T2 can be set and programmed according to the mechanical range of the application with a resolution of 14 bits. In addition, the T1Y and T2Y parameter can be set and programmed according to the application. The transition point 0 to 360 degree can be shifted using the break point parameter BP. This point is programmable with a high resolution of 14 bits of 360 degrees. The voltage for clamping level low CLL and clamping level high CLH can be programmed with a resolution of 7 bits. Both levels are individually adjustable.

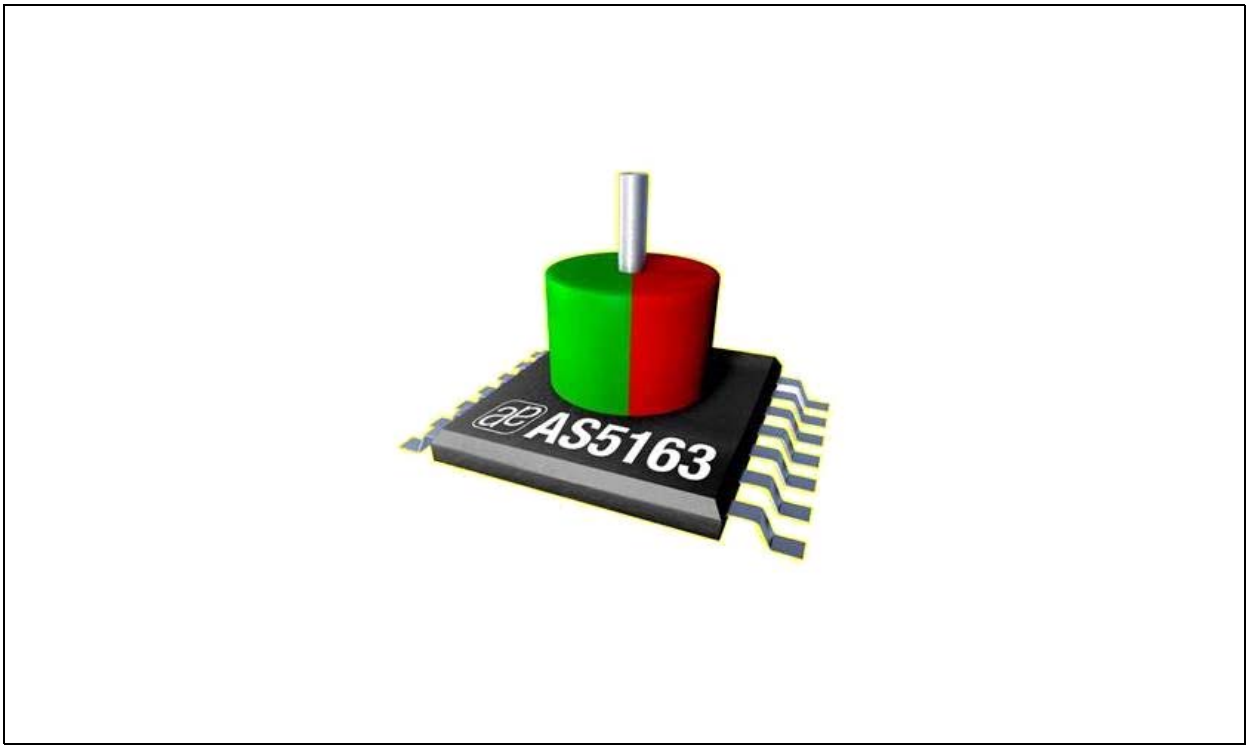
These parameters are also used to adjust the PWM duty cycle.

The AS5163 also provides a compare function. The internal angular code is compared to a programmable level using hysteresis. The function is available over the output pin 11 (KDOWN).

The output parameters can be programmed in an OTP register. No additional voltage is required to program the AS5163. The setting may be overwritten at any time and will be reset to default when power is cycled. To make the setting permanent, the OTP register must be programmed by using a lock bit. Else, the content could be frozen for ever.

The AS5163 is tolerant to magnet misalignment and unwanted external magnetic fields due to differential measurement technique and Hall sensor conditioning circuitry.

Figure 3. Typical Arrangement of AS5163 and Magnet

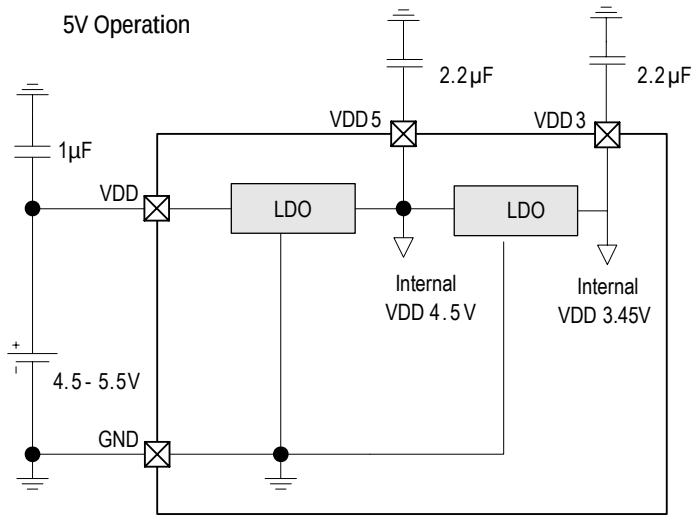


7.1 Operation

The AS5163 operates at 5V ±10%, using two internal Low-Dropout (LDO) voltage regulators. For operation, the 5V supply is connected to pin VDD. While VDD3 and VDD5 (LDO outputs) must be buffered by 2.2µF capacitors, the VDD requires a 1µF capacitor. All capacitors (low ESR ceramic) are supposed to be placed close to the supply pins (see Figure 4).

The VDD3 and VDD5 outputs are intended for internal use only. It must not be loaded with an external load.

Figure 4. Connections for 5V Supply Voltages



Notes:

1. The pins VDD3 and VDD5 must always be buffered by a capacitor. These pins must not be left floating, as this may cause unstable internal supply voltages, which may lead to larger output jitter of the measured angle.
2. Only VDD is overvoltage protected up to 27V. In addition, the VDD has a reverse polarity protection.

7.1.1 VDD Voltage Monitor

VDD Overvoltage Management. If the voltage applied to the VDD pin exceeds the overvoltage upper threshold for longer than the detection time, then the device enters a low power mode reducing the power consumption. When the overvoltage event has passed and the voltage applied to the VDD pin falls below the overvoltage lower threshold for longer than the recovery time, then the device enters the normal mode.

VDD5 Undervoltage Management. When the voltage applied to the VDD5 pin falls below the undervoltage lower threshold for longer than the VDD5_detection time, then the device stops the clock of the digital part and the output drivers are turned off to reduce the power consumption. When the voltage applied to the VDD5 pin exceeds the VDD5 undervoltage upper threshold for longer than the VDD5_recovery time, then the clock is restarted and the output drivers are turned on.

7.2 Analog Output

The reference voltage for the Digital-to-Analog converter (DAC) is taken internally from VDD. In this mode, the output voltage is ratiometric to the supply voltage.

7.2.1 Programming Parameters

The Analog output voltage modes are programmable by OTP. Depending on the application, the analog output can be adjusted. The user can program the following application specific parameters:

T1	Mechanical angle start point
T2	Mechanical angle end point
T1Y	Voltage level at the T1 position
T2Y	Voltage level at the T2 position
CLL	Clamping Level Low
CLH	Clamping Level High
BP	Break point (transition point 0 to 360 degree)

The above listed parameters are input parameters. Over the provided programming software and programmer, these parameters are converted and finally written into the AS5163 128-bit OTP memory.

7.2.2 Application Specific Angular Range Programming

The application range can be selected by programming T1 with a related T1Y and T2 with a related T2Y into the AS5163. The internal gain factor is calculated automatically. The clamping levels CLL and CLH can be programmed independent from the T1 and T2 position and both levels can be separately adjusted.

Figure 5. Programming of an Individual Application Range

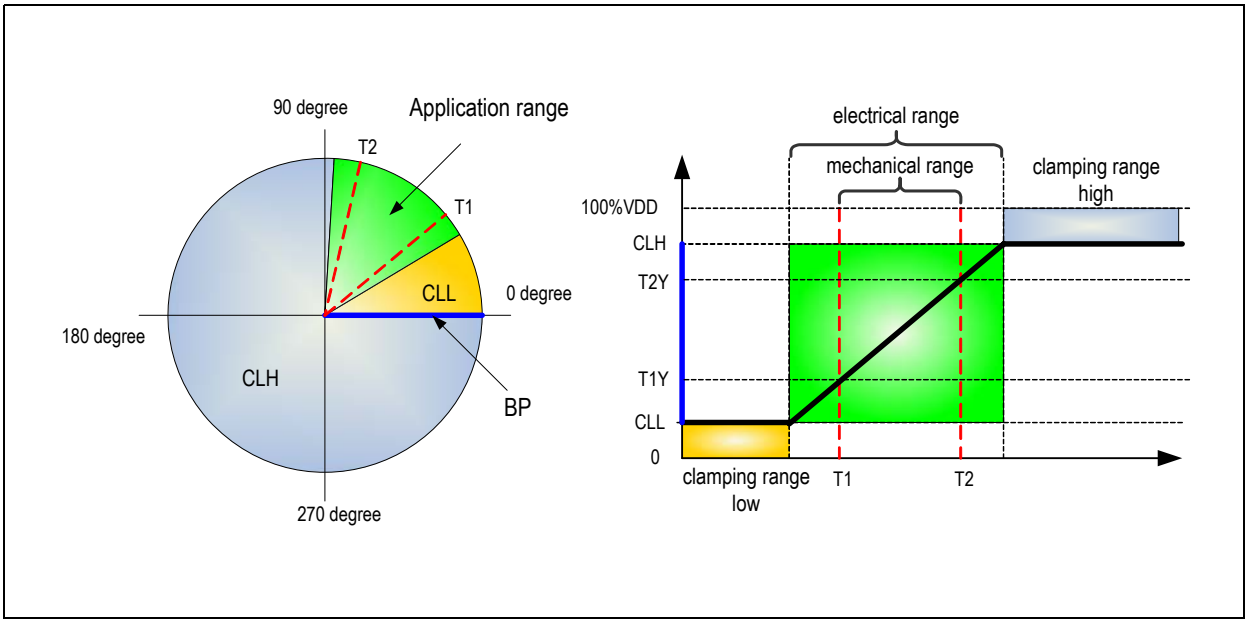
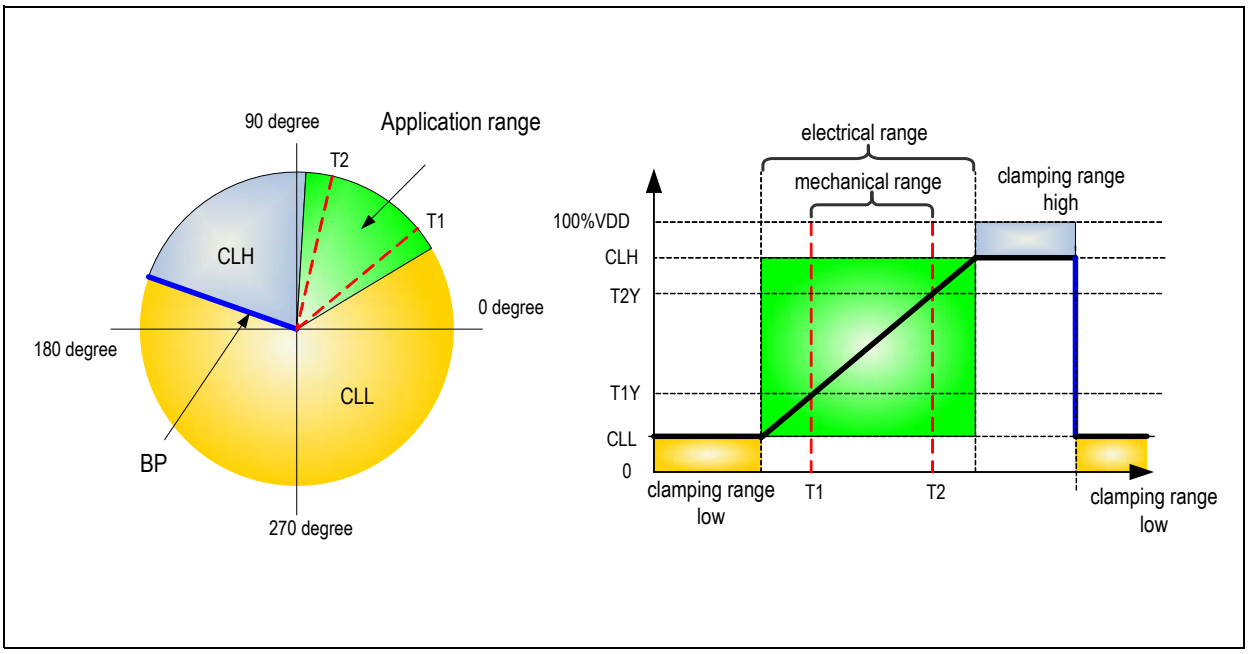


Figure 5 shows a simple example of the selection of the range. The mechanical starting point T1 and the mechanical end point T2 define the mechanical range. A sub range of the internal Cordic output range is used and mapped to the needed output characteristic. The analog output signal has 12 bit, hence the level T1Y and T2Y can be adjusted with this resolution. As a result of this level and the calculated slope the clamping region low is defined. The break point BP defines the transition between CLL and CLH. In this example, the BP is set to 0 degree. The BP is also the end point of the clamping level high CLH. This range is defined by the level CLH and the calculated slope. Both clamping levels can be set independently form each other. The minimum application range is 10 degrees.

7.2.3 Application Specific Programming of the Break Point

The break point BP can be programmed as well with a resolution of 14 bits. This is important when the default transition point is inside the application range. In such a case, the default transition point must be shifted out of the application range. The parameter BP defines the new position. The function can be used also for an on-off indication.

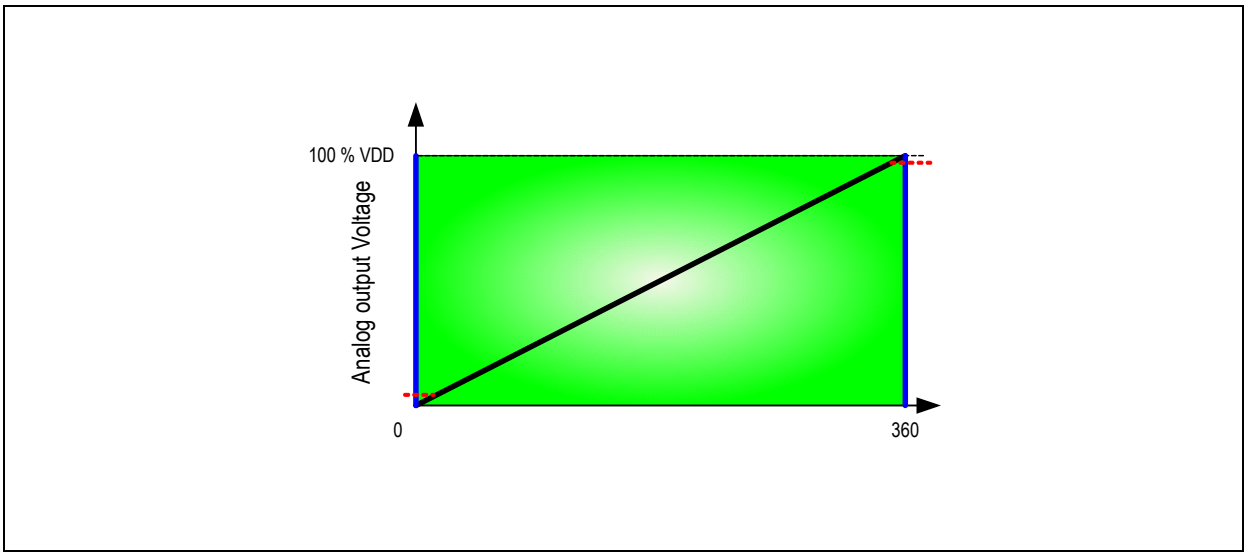
Figure 6. Individual Programming of the Break Point BP



7.2.4 Full Scale Mode

The AS5163 can be programmed as well in the full scale mode. The BP parameter defines the position of the transition.

Figure 7. Full Scale Mode



For simplification, Figure 7 describes a linear output voltage from rail to rail (0V to VDD) over the complete rotation range. In practice, this is not feasible due to saturation effects of the output stage transistors. The actual curve will be rounded towards the supply rails (as indicated Figure 7).

7.2.5 Resolution of the Parameters

The programming parameters have a wide resolution of up to 14 bits.

Table 7. Resolution of the Programming Parameters

Symbol	Parameter	Resolution	Note
T1	Mechanical angle start point	14 bits	
T2	Mechanical angle stop point	14 bits	
T1Y	Mechanical start voltage level	12 bits	
T2Y	Mechanical stop voltage level	12 bits	
CLL	Clamping level low	7 bits	4096 LSBs is the maximum level
CLH	Clamping level high	7 bits	31 LSBs is the minimum level
BP	Break point	14 bits	

Figure 8. Overview of the Angular Output Voltage

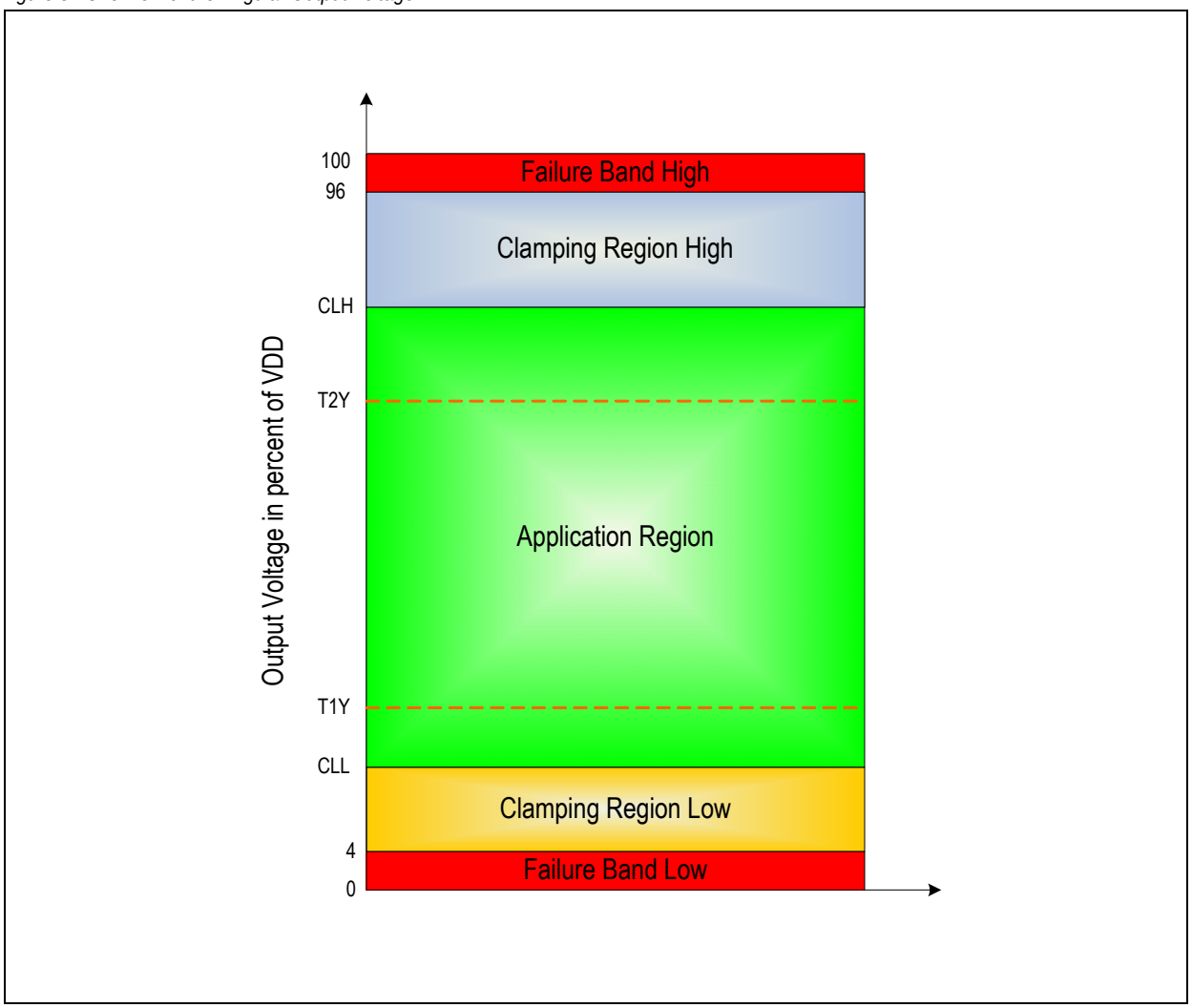


Figure 8 gives an overview of the different ranges. The failure bands are used to indicate a wrong operation of the AS5163. This can be caused due to a broken supply line. By using the specified load resistors, the output level will remain in these bands during a fail. It is recommended to set the clamping level CLL above the lower failure band and the clamping level CLH below the higher failure band.

7.2.6 Analog Output Diagnostic Mode

Due to the low pin count in the application, a wrong operation must be indicated by the output pin OUT. This could be realized using the failure bands. The failure band is defined with a fixed level. The failure band low is specified from 0% to 4% of the supply range. The failure band high is defined from 100% to 96%. Several failures can happen during operation. The output signal remains in these bands over the specified operating and load conditions. All the different failures can be grouped into the internal alarms (failures) and the application related failures.

$C_{LOAD} \leq 42$ nF, R_{PU}= 2k…5.6kΩ

R_{PD}= 2k…5.6kΩ load pull-up

Table 8. Different Failure Cases of AS5163

Type	Failure Mode	Symbol	Failure Band	Note
Internal alarms (failures)	Out of magnetic range (too less or too high magnetic input)	MAGRng	High/Low	Could be switched off by one OTP bit ALARM_DISABLE. Programmable by OTP bit DIAG_HIGH
	Cordic overflow	COF	High/Low	Programmable by OTP bit DIAG_HIGH
	Offset compensation finished	OCF	High/Low	Programmable by OTP bit DIAG_HIGH
	Watchdog fail	WDF	High/Low	Programmable by OTP bit DIAG_HIGH
	Oscillator fail	OF	High/Low	Programmable by OTP bit DIAG_HIGH
Application related failures	Overvoltage condition	OV	High/Low	Dependant on the load resistor Pull up → failure band high Pull down → failure band low
	Broken VDD	BVDD		
	Broken VSS	BVSS		
	Short circuit output	SCO	High/Low	Switch off → short circuit dependent

For efficient use of diagnostics, it is recommended to program to clamping levels CLL and CLH.

7.2.7 Analog Output Driver Parameters

The output stage is configured in a push-pull output. Therefore it is possible to sink and source currents.

$C_{LOAD} \leq 42$ nF, R_{PU}= 2k…5.6kΩ

R_{PD}= 2k…5.6kΩ load pull-up

Table 9. General Parameters for the Output Driver

Symbol	Parameter	Min	Typ	Max	Unit	Note
IOUTSCL	Short circuit output current (low side driver)	8		32	mA	V_{OUT}=27V
IOUTSCH	Short circuit output current (high side driver)	-8		-32	mA	V_{OUT}=0V
TSCDET	Short circuit detection time	20		600	µs	output stage turned off
TSCREC	Short circuit recovery time	2		20	ms	output stage turned on
ILEAKOUT	Output Leakage current	-20		20	µA	V_{OUT}=VDD=5V
BGNDPU	Output voltage broken GND with pull-up	96		100	%VDD	R_{PU} = 2k…5.6k
BGNDPD	Output voltage broken GND with pull-down	0		4	%VDD	R_{PD} = 2k…5.6k
BVDDPU	Output voltage broken VDD with pull-up	96		100	%VDD	R_{PU} = 2k…5.6k
BVDDPD	Output voltage broken VDD with pull-down	0		4	%VDD	R_{PD} = 2k…5.6k

Note: A Pull-Up/Down load is up to 1kΩ with increased diagnostic bands from 0%-6% and 94%-100%.

Table 10. Electrical Parameters for the Analog Output Stage

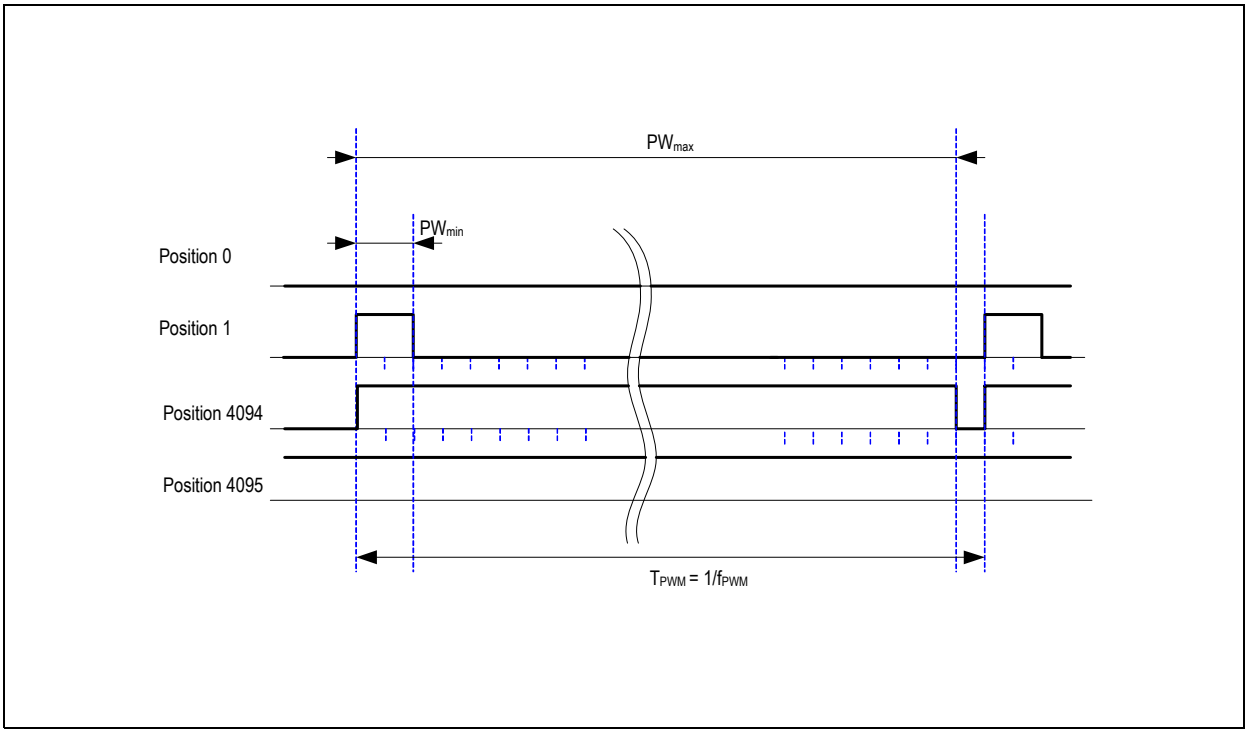
Symbol	Parameter	Min	Typ	Max	Unit	Note
VOUT	Output Voltage Range	4		96	% VDD	
		6		94		Valid when 1k ≤ RLOAD < 2k
VOUTINL	Output Integral nonlinearity			10	LSB	
VOUTDNL	Output Differential nonlinearity	-10		10	LSB	
VOUTOFF	Output Offset	-50		50	mV	At 2048 LSB level
VOUTUD	Update rate of the Output		100		µs	Info parameter
VOUTSTEP	Output Step Response			550	µs	Between 10% and 90%, R_{PU}/R_{PD} =1kΩ, CLOAD=1nF; VDD=5V
VOUTDRIFT	Output Voltage Temperature drift	2		2	%	Of value at mid code
VOUTRATE	Output ratiometricity error	-1.5		1.5	%VDD	0.04*VDD ≤ VOUT ≤ 0.96*VDD
VOUTNOISE	Noise[1]			10	mVpp	1Hz…30kHz; at 2048 LSB level

1. Not tested in production; characterization only.

7.3 Pulse Width Modulation (PWM) Output

The AS5163 provides a pulse width modulated output (PWM), whose duty cycle is proportional to the measured angle. This output format is selectable over the OTP memory OP_MODE(0) bit. If output pin OUT is configured as open drain configuration, then an external load resistor (pull up) is required. The PWM frequency is internally trimmed to an accuracy of ±10% over full temperature range. This tolerance can be cancelled by measuring the ratio between the on and off state. In addition, the programmed clamping levels CLL and CLH will also adjust the PWM signal characteristic.

Figure 9. PWM Output Signal



The PWM frequency can be programmed by the OTP bits PWM_frequency (1:0). Therefore, four different frequencies are possible.

Table 11. PWM Signal Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
f_{PWM1}	PWM frequency1	123.60	137.33	151.06	Hz	PWM_frequency (1:0) = “00”
f_{PWM2}	PWM frequency2	247.19	274.66	302.13	Hz	PWM_frequency (1:0) = “01”
f_{PWM3}	PWM frequency3	494.39	549.32	604.25	Hz	PWM_frequency (1:0) = “10”
f_{PWM4}	PWM frequency4	988.77	1098.63	1208.50	Hz	PWM_frequency (1:0) = “11”
PW_{MIN}	MIN pulse width		(1+1)*1/ f_{PWM}		µs	
PW_{MAX}	MAX pulse width		(1+4094)*1/ f_{PWM}		ms	

Taking into consideration the AC characteristic of the PWM output including load, it is recommended to use the clamping function. The recommended range is 0% to 4% and 96% to 100%.

Table 12. Electrical Parameters for the PWM Output Mode

Symbol	Parameter	Min	Typ	Max	Unit	Note
PWMVOL	Output voltage low	0		0.4	V	I_{OUT}=8mA
ILEAK	Output leakage	-20		20	µA	V_{OUT}=VDD=5V
PWMDC	PWM duty cycle range	4		96	%	
PWMSRF	PWM slew rate	1	2	4	V/µs	Between 75% and 25% R_{PU}/R_{PD} = 1kΩ, C_{LOAD} = 1nF, VDD = 5V

7.4 Kick Down Function

The AS5163 provides a special compare function. This function is implemented using a programmable angle value with a programmable hysteresis. It will be indicated over the open drain output pin KDOWN. If the actual angle is above the programmable value plus the hysteresis, the output is switched to low. The output will remain at low level until the value KD is reached in the reverse direction.

Figure 10. Kick Down Hysteresis Implementation

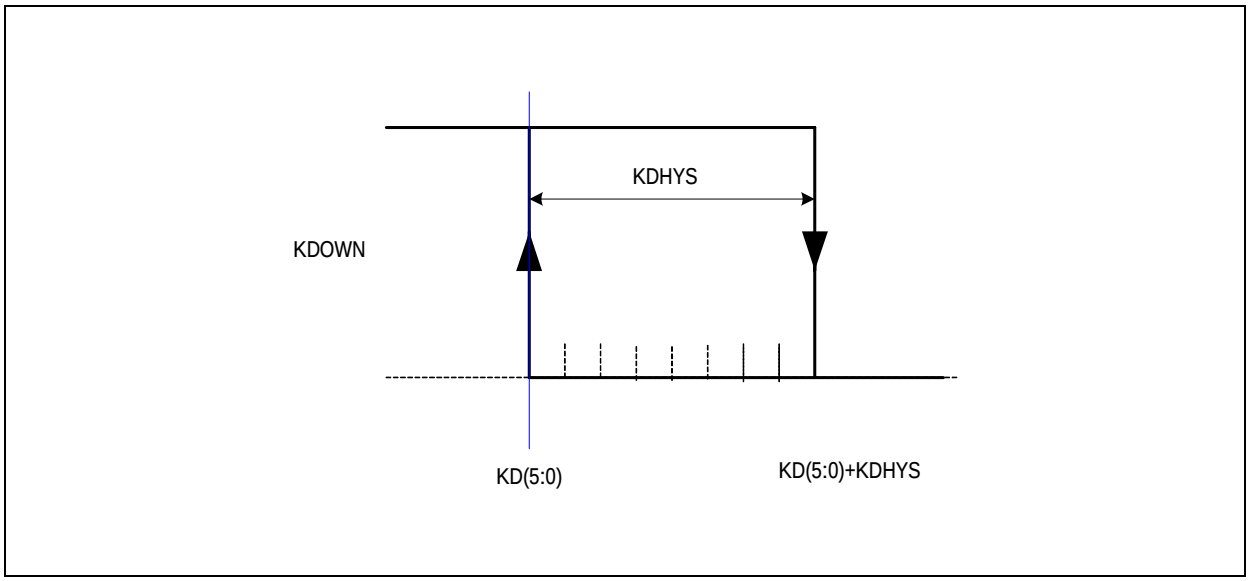


Table 13. Programming Parameters for the Kick Down Function

Symbol	Parameter	Resolution	Note
KD	Kick Down angle	6 bits	
KDHYS	Kick Down Hysteresis	2 bits	KDHYS (1:0) = “00” → 8 LSB hysteresis KDHYS (1:0) = “01” → 16 LSB hysteresis KDHYS (1:0) = “10” → 32 LSB hysteresis KDHYS (1:0) = “11” → 64 LSB hysteresis

Pull-up resistance 1k to 5.6K to VDD

CLOAD max 42nF

Table 14. Electrical Parameters of the KDOWN Output

Symbol	Parameter	Min	Typ	Max	Unit	Note
IKDSC	Short circuit output current (Low Side Driver)	6		24	mA	V_{KDOWN} = 27V
TSCDET	Short circuit detection time	20		600	µs	output stage turned off
TSCREC	Short circuit recovery time	2		20	ms	output stage turned on
KDVOL	Output voltage low	0		1.1	V	I_{KDOWN} = 6mA
KDILEAK	Output leakage	-20		20	µA	V_{KDOWN} = 5V
KDSRF	KDOWN slew rate (falling edge)	1	2	4	V/µs	Between 75% and 25%, R_{PUKDWN} = 1kΩ, C_{LOAD_KDWN} = 1nF, VDD = 5V

8 Application Information

The benefits of AS5163 are as follows:

- Unique fully differential patented solution
- Best protection for automotive applications
- Easy to program
- Flexible interface selection PWM, analog output
- Ideal for applications in harsh environments due to contactless position sensing
- Robust system, tolerant to magnet misalignment, airgap variations, temperature variations and external magnetic fields
- No calibration required because of inherent accuracy
- High driving capability of analog output (including diagnostics)

8.1 Programming the AS5163

The AS5163 programming is a one-time-programming (OTP) method, based on polysilicon fuses. The advantage of this method is that no additional programming voltage is needed. The internal LDO provides the current for programming.

The OTP consists of 128 bits, wherein several bits are available for user programming. In addition, factory settings are stored in the OTP memory. Both regions are independently lockable by built-in lock bits.

A single OTP cell can be programmed only once. By default, each cell is “0”; a programmed cell will contain a “1”. While it is not possible to reset a programmed bit from “1” to “0”, multiple OTP writes are possible, as long as only unprogrammed “0”-bits are programmed to “1”.

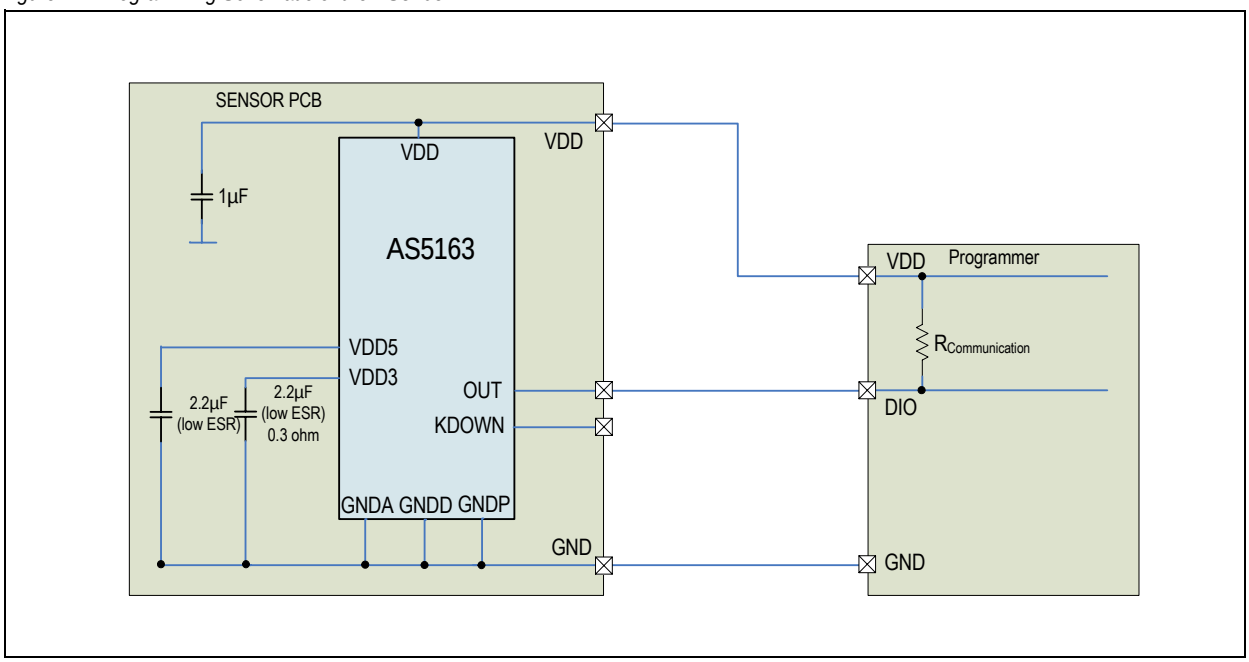
Independent of the OTP programming, it is possible to overwrite the OTP register temporarily with an OTP write command. This is possible only if the user lock bit is not programmed.

Due to the programming over the output pin, the device will initially start in the communication mode. In this mode, the digital angle value can be read with a specific protocol format. It is a bidirectional communication possible. Parameters can be written into the device. A programming of the device is triggered by a specific command. With another command (pass2funcion), the device can be switched into operation mode (analog or PWM output). In case of a programmed user lock bit, the AS5163 automatically starts up in the functional operation mode. No communication of the specific protocol is possible after this.

8.1.1 Hardware Setup

The pin OUT and the supply connection are required for OTP memory access. Without the programmed Mem_Lock_USER OTP bit, the device will start up in the communication mode and will remain into an IDLE operation mode. The pull up resistor $R_{Communication}$ is required during startup. Figure 1 shows the configuration of an AS5163.

Figure 11. Programming Schematic of the AS5163



8.1.2 Protocol Timing and Commands of Single Pin Interface

During the communication mode, the output level is defined by the external pull up resistor $R_{Communication}$. The output driver of the device is in tri-state. The bit coding (see Figure 18) has been chosen in order to allow the continuous synchronization during the communication, which can be required due to the tolerance of the internal clock frequency. Figure 18 shows how the different logic states '0' and '1' are defined. The period of the clock T_{CLK} is defined with 222.2 ns.

The voltage levels V_H and V_L are CMOS typical.

Each frame is composed by 20 bits. The 4 MSB (CMD) of the frame specifies the type of command that is passed to the AS5163. The 16 data bits contain the communication data. There will be no operation when the 'not specified' CMD is used. The sequence is oriented in such a way that the LSB of the data is followed by the command. The number of frames vary depending on the command. The single pin programming interface block of the AS5163 can operate in slave communication or master communication mode. In the slave communication mode, the AS5163 receives the data organized in frames. The programming tool is the driver of the single communication line and can pull down the level. In case of the master communication mode, the AS5163 transmits data in the frame format. The single communication line can be pulled down by the AS5163.

Figure 12. Bit Coding of the Single Pin Programming Interface

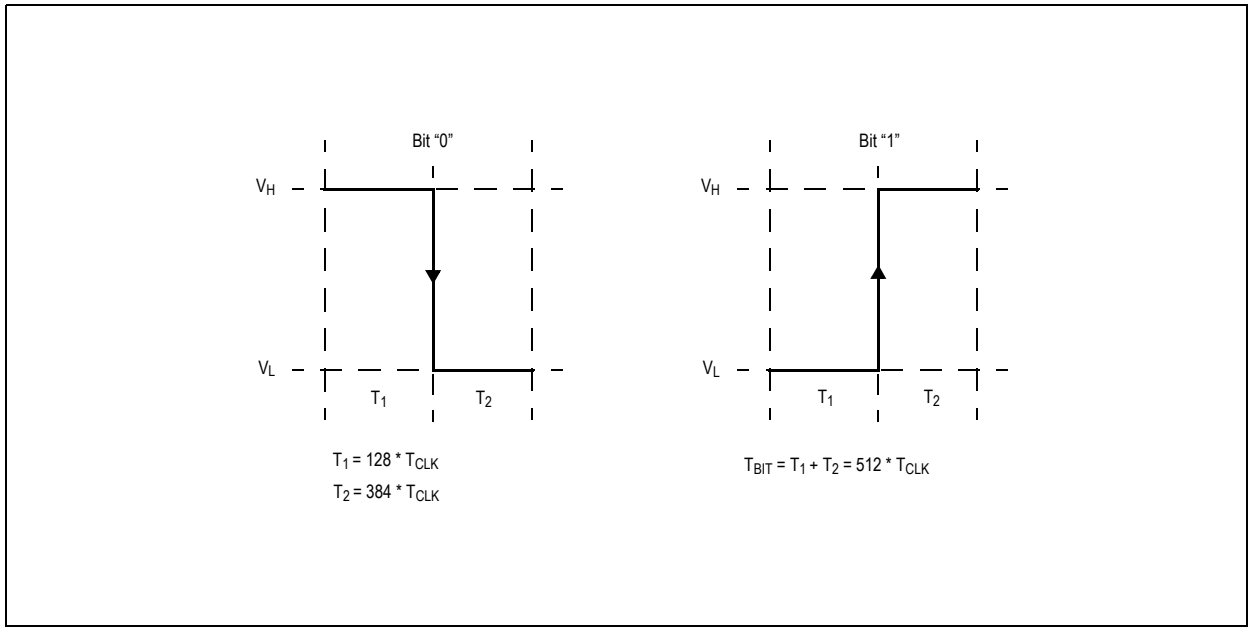


Figure 13. Protocol Definition

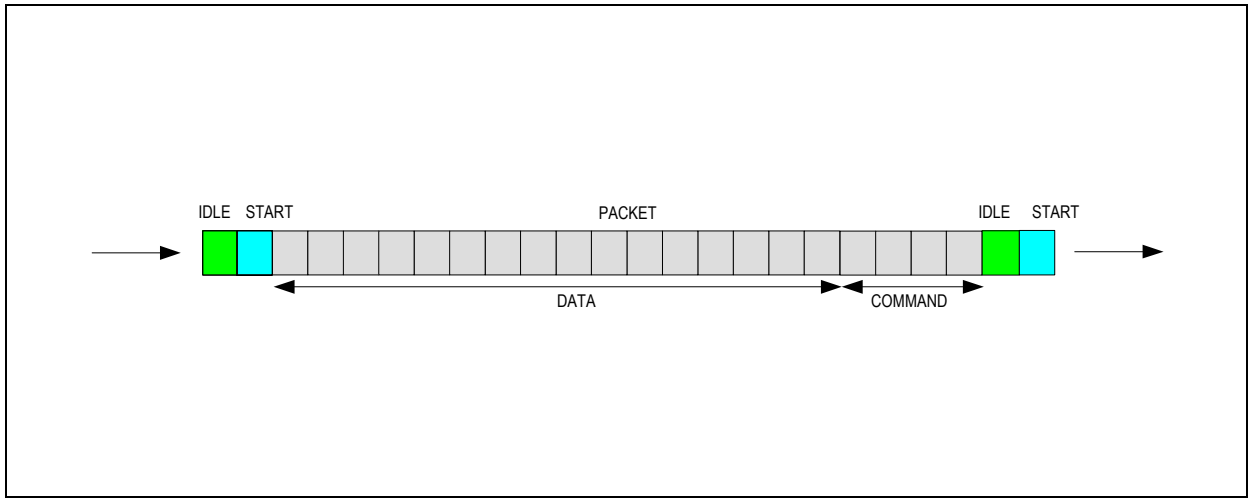


Table 15. OTP Commands and Communication Interface Modes

Possible Interface Commands	Description	AS5163 Communication Mode	Command CMD	Number of Frames
UNBLOCK	Resets the interface	SLAVE	0x0	1
WRITE128	Writes 128 bits (user + factory settings) into the device	SLAVE	0x9 (0x1)	8
READ128	Reads 128 bits (user + factory settings) from the device	SLAVE and MASTER	0xA	9
UPLOAD	Transfers the register content into the OTP memory	SLAVE	0x6	1
DOWNLOAD	Transfers the OTP content to the register content	SLAVE	0x5	1
FUSE	Command for permanent programming	SLAVE	0x4	1
PASS2FUNC	Change operation mode from communication to operation	SLAVE	0x7	1
READ	Read related to address the user data	SLAVE and MASTER	0xB	2
WRITE	Write related to address the user data	SLAVE	0xC	1

Note: Other commands are reserved and shall not be used.

When single pin programming interface bus is in high impedance state, the logical level of the bus is held by the pull up resistor $R_{Communication}$. Each communication begins by a condition of the bus level which is called START. This is done by forcing the bus in logical low level (done by the programmer or AS5163 depending on the communication mode). Afterwards the bit information of the command is transmitted as shown in Figure 14.

Figure 14. Bus Timing for the WRITE128 Command

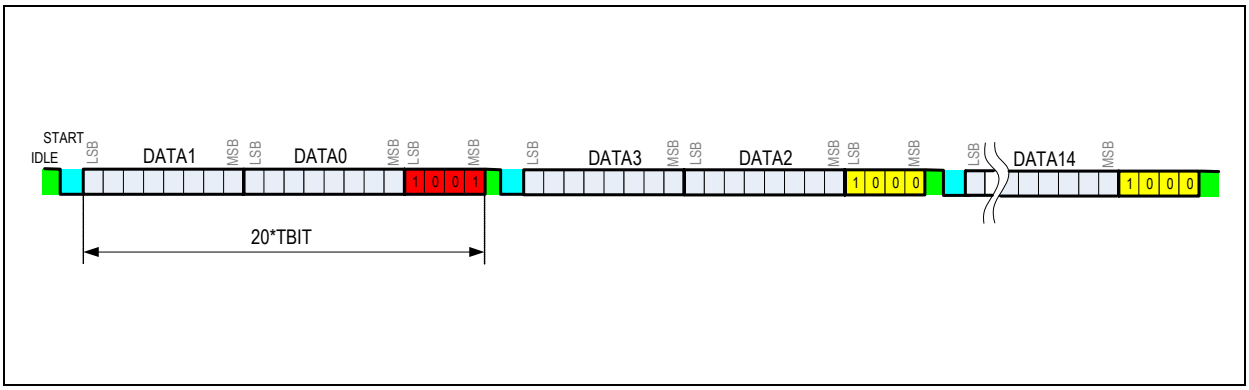
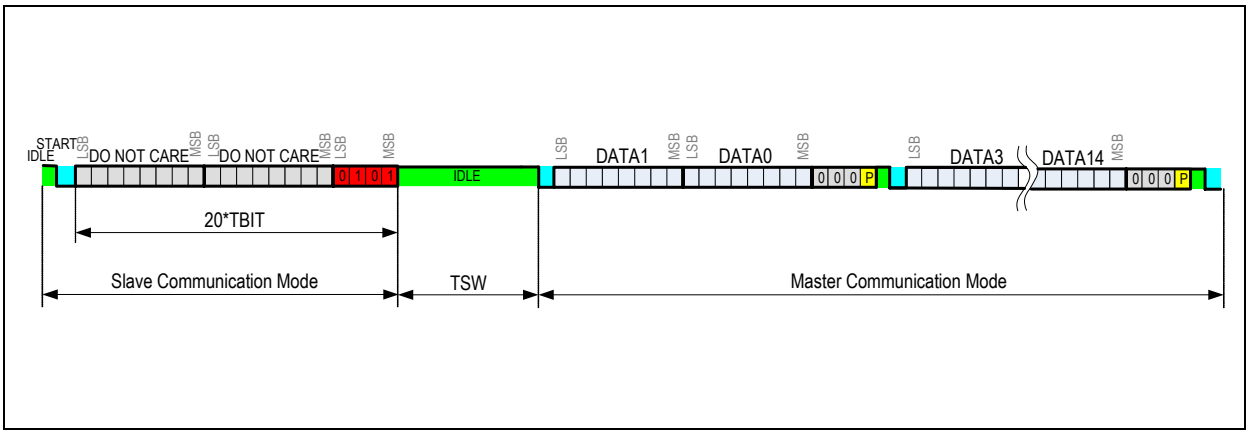
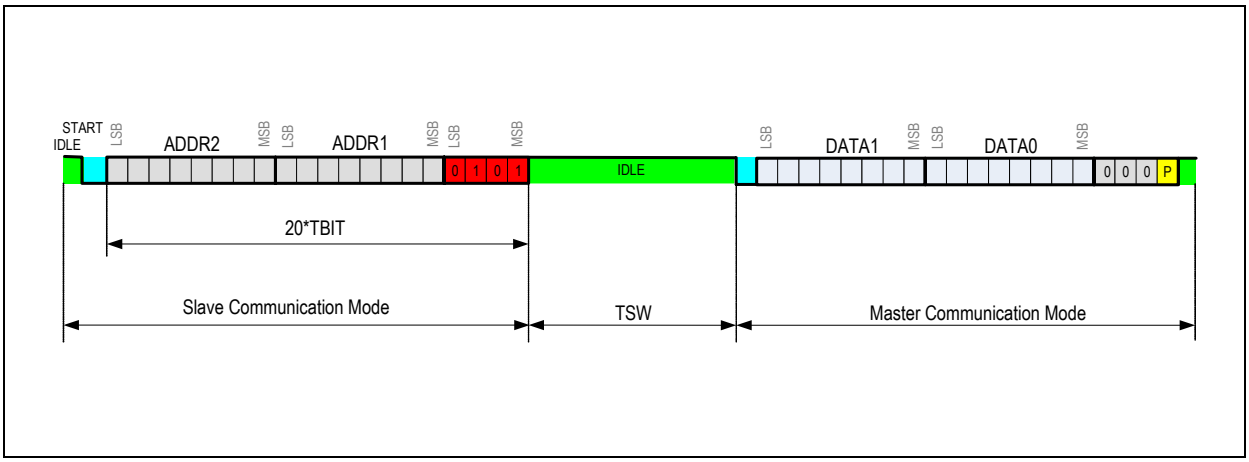


Figure 15. Bus Timing for the READ128 Command



In case of READ or READ128 command (see Figure 15) the idle phase between the command and the answer is 10 TBIT (TSW).

Figure 16. Bus Timing for the READ Commands



In case of a WRITE command, the device stays in slave communication mode and will not switch to master communication mode.

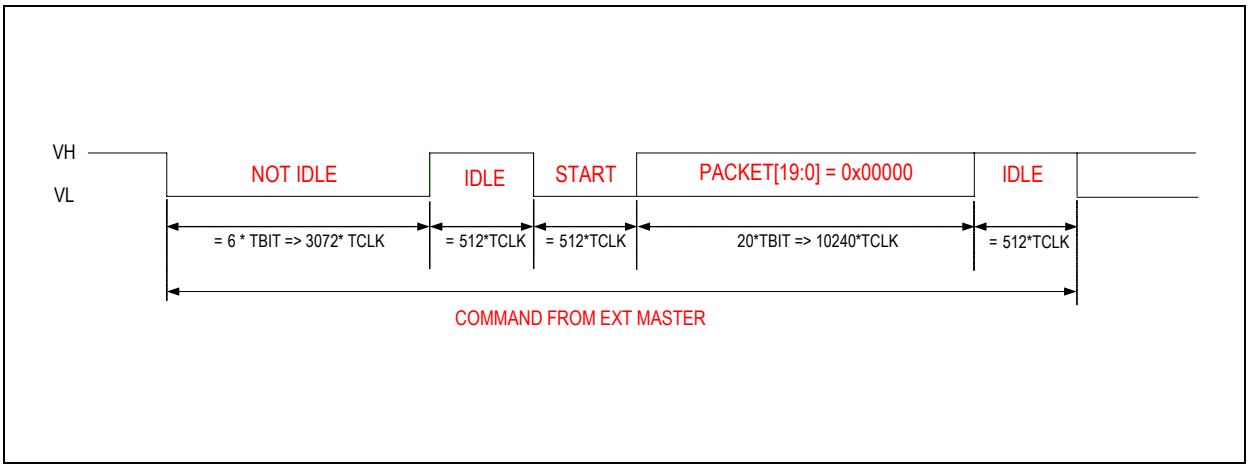
When using other commands like DOWNLOAD, UPLOAD, etc. instead of READ or WRITE, it does not matter what is written in the address fields (ADDR1, ADDR2).

8.1.3 UNBLOCK

The Unblock command can be used to reset only the one-wire interface of the AS5163 in order to recover the possibility to communicate again without the need of a POR after a stacking event due to noise on the bus line or misalignment with the AS5163 protocol.

The command is composed by a not idle phase of at least 6 TBIT followed by a packet with all 20 bits at zero (see Figure 17).

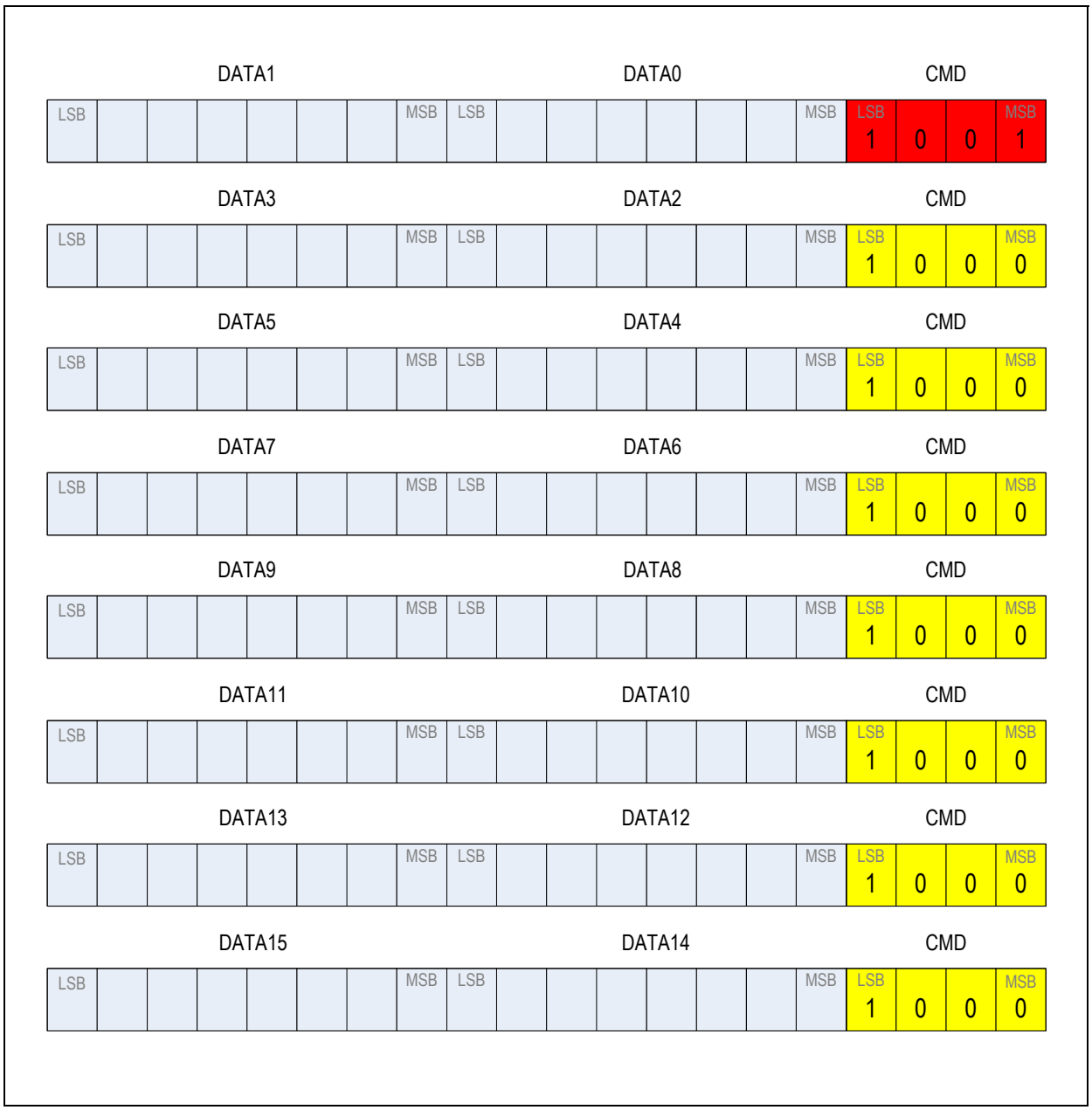
Figure 17. Unblock Sequence



8.1.4 WRITE128

Figure 18 illustrates the format of the frame and the command.

Figure 18. Frame Organization of the WRITE128 Command



The command contains 8 frames. With this command, the AS5163 receives only frames. This command will transfer the data in the special function registers (SFRs) of the device. The data is not permanent programmed using this command.

Table 16 describe the organization of the OTP data bits.

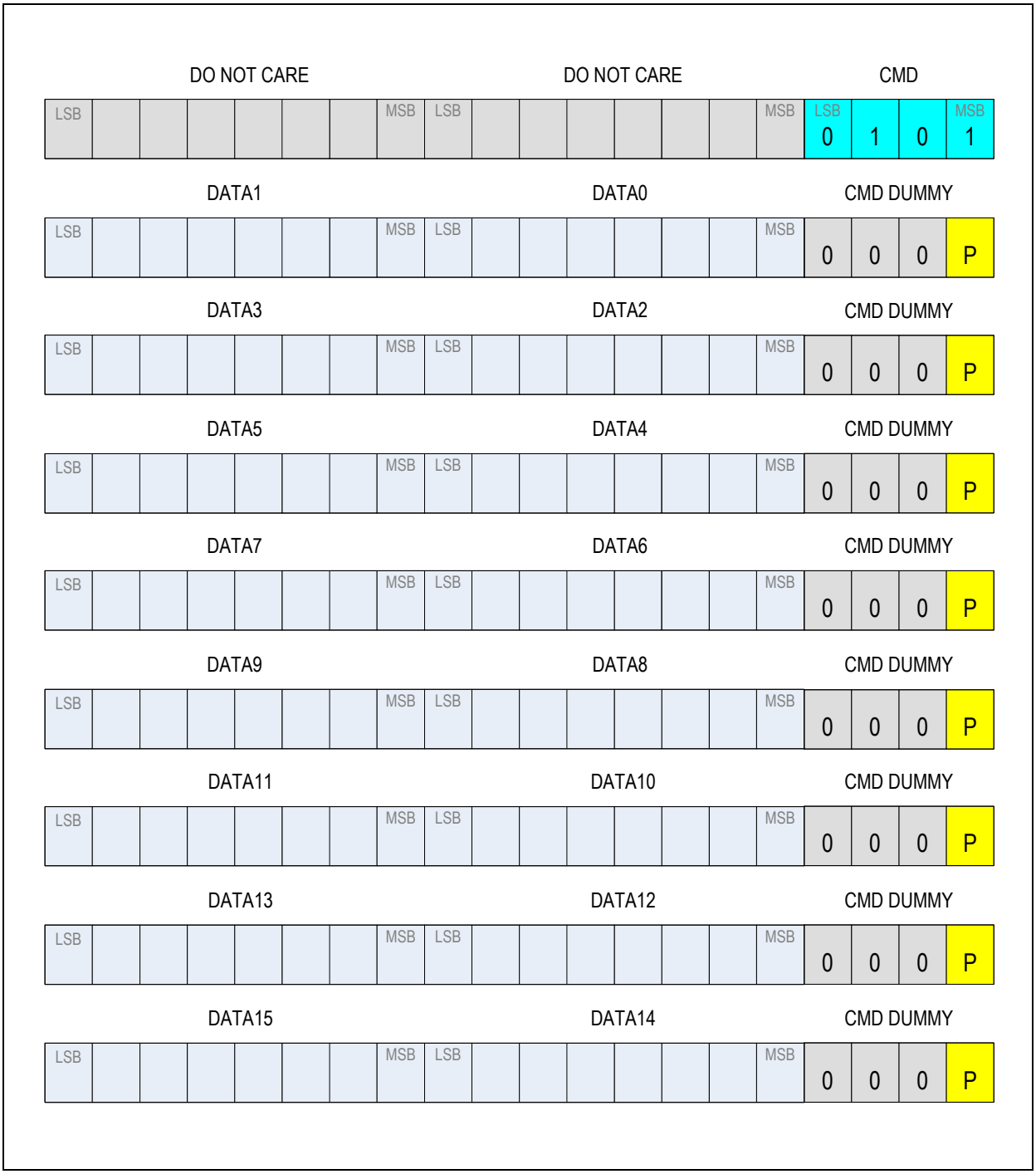
The access is performed with CMD field set to 0x9. The next 7 frames with CMD field set to 0x1. The 2 bytes of the first command will be written at address 0 and 1 of the SFRs; the 2 bytes of the second command will be written at address 2 and 3; and so on, in order to cover all the 16 bytes of the 128 SFRs.

Note: It is important to always complete the command. All 8 frames are needed. In case of a wrong command or a communication error, a power on reset must be performed. The device will be delivered with the programmed Mem_Lock_AMS OTP bit. This bit locks the content of the factory settings. It is impossible to overwrite this particular region. The written information will be ignored.

8.1.5 READ128

Figure 19 illustrates the format of the frame and the command.

Figure 19. Frame Organization of the READ128 Command



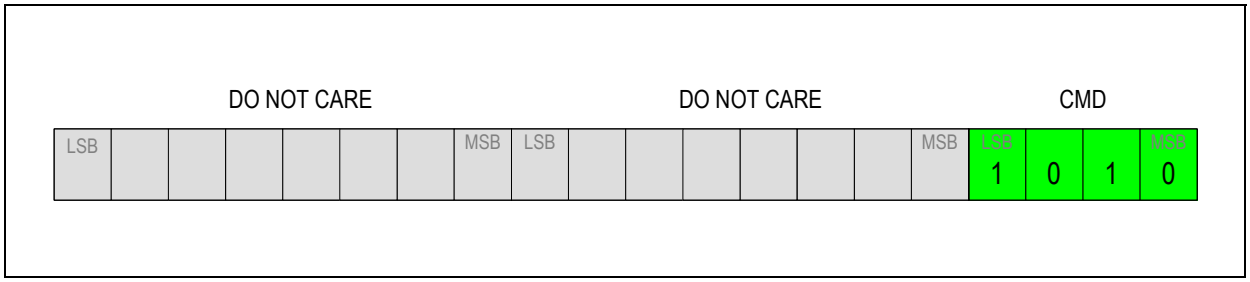
The command is composed by a first frame transmitted to the AS5163. The device is in slave communication mode. The device remains for the time T_{SWITCH} in IDLE mode before changing into the master communication mode. The AS5163 starts to send 8 frames. This command will read the SFRs. The numbering of the data bytes correlates with the address of the related SFR.

An even parity bit is used to guarantee a correct data transmission. Each parity (P) is related to the frame data content of the 16 bit word. The MSB of the CMD dummy (P) is reserved for the parity information.

8.1.6 DOWNLOAD

Figure 20 shows the format of the frame.

Figure 20. Frame Organization of the DOWNLOAD Command



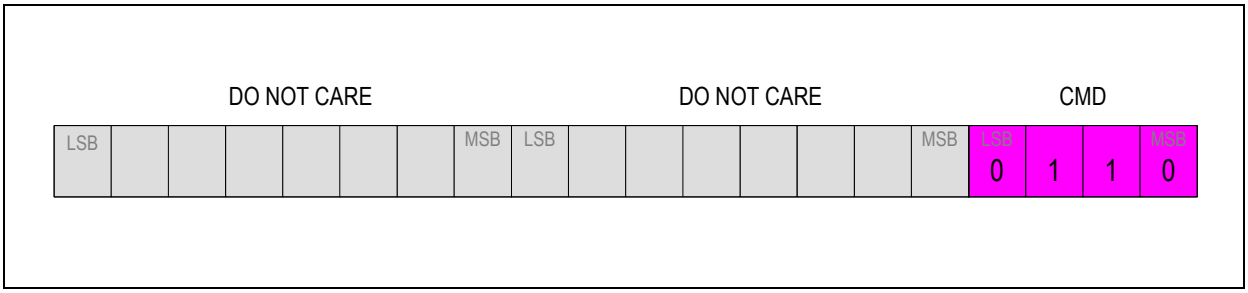
The command consists of one frame received by the AS5163 (slave communication mode). The OTP cell fuse content will be downloaded into the SFRs.

The access is performed with CMD field set to 0x5.

8.1.7 UPLOAD

Figure 21 shows the format of the frame.

Figure 21. Frame Organization of the UPLOAD Command



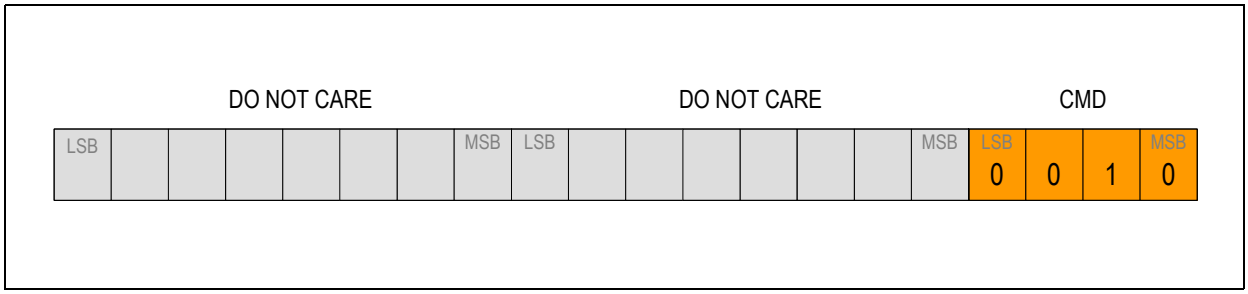
The command consists of one frame received by the AS5163 (slave communication mode) and transfers the data from the SFRs into the OTP fuse cells. The OTP fuses are not permanent programmed using this command.

The access is performed with CMD field set to 0x6.

8.1.8 FUSE

Figure 22 shows the format of the frame.

Figure 22. Frame Organization of the FUSE Command



The command consists of one frame received by the AS5163 (slave communication mode) and it is giving the trigger to permanent program the non volatile fuse elements.

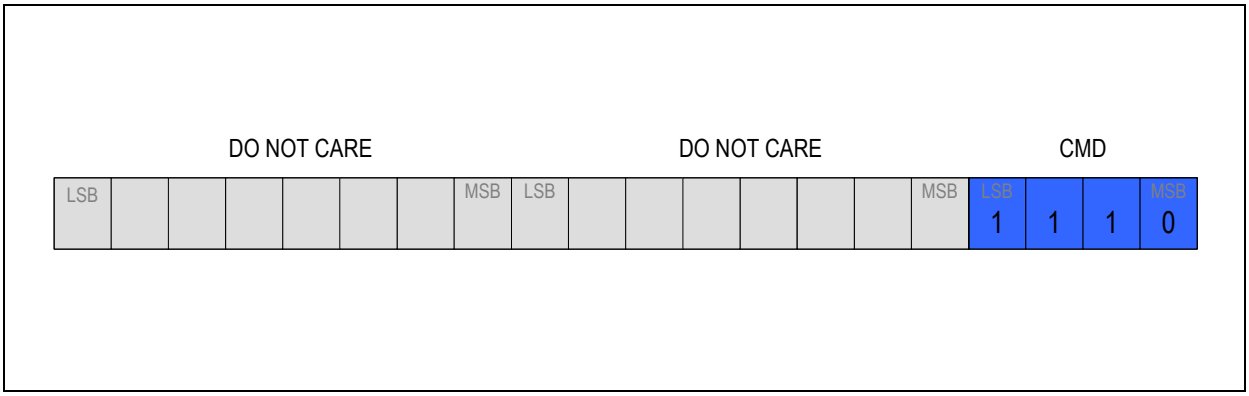
The access is performed with CMD field set to 0x4.

Note: After this command, the device automatically starts to program the built-in programming procedure. It is not allowed to send other commands during this programming time. This time is specified to 4ms after the last CMD bit.

8.1.9 PASS2FUNC

Figure 23 shows the format of the frame.

Figure 23. Frame Organization of the PASS2FUNCTION Command



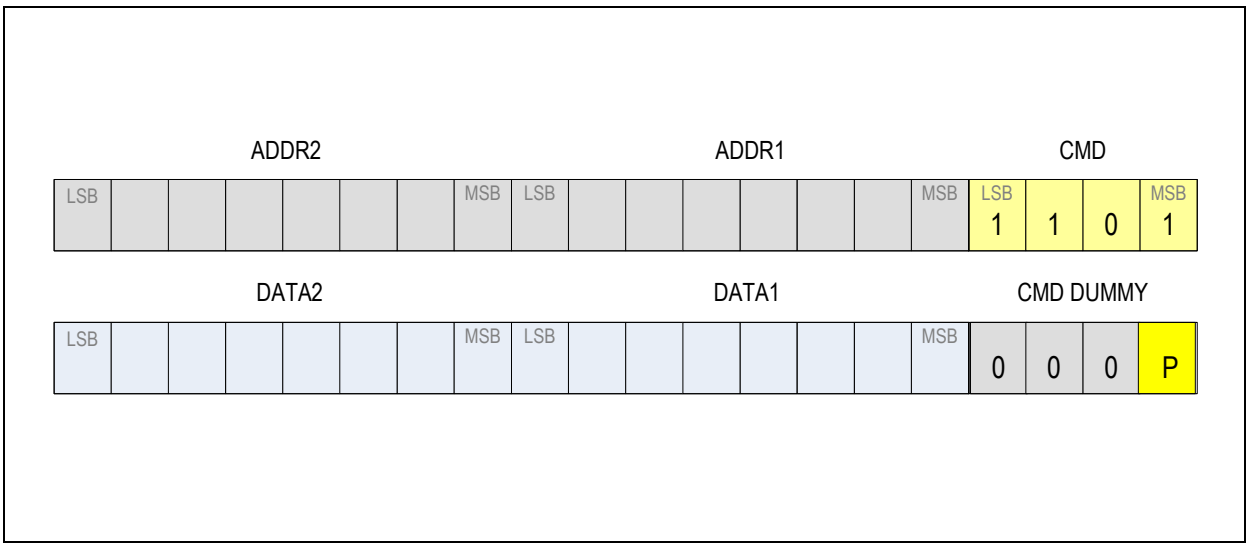
The command consists of one frame received by the AS5163 (slave communication mode). This command stops the communication receiving mode, releases the reset of the DSP of the AS5163 device and starts to work in functional mode with the values of the SFR currently written.

The access is performed with CMD field set to 0x7.

8.1.10 READ

Figure 24 shows the format of the frame.

Figure 24. Frame Organization of the READ Command



The command is composed by a first frame sent to the AS5163. The device is in slave communication mode. The device remains for the time T_{SWITCH} in IDLE mode before changing into the master communication mode. The AS5163 starts to send the second frame transmitted by the AS5163.

The access is performed with CMD field set to 0xB.

When the AS5163 receives the first frame, it sends a frame with data value of the address specified in the field of the first frame.

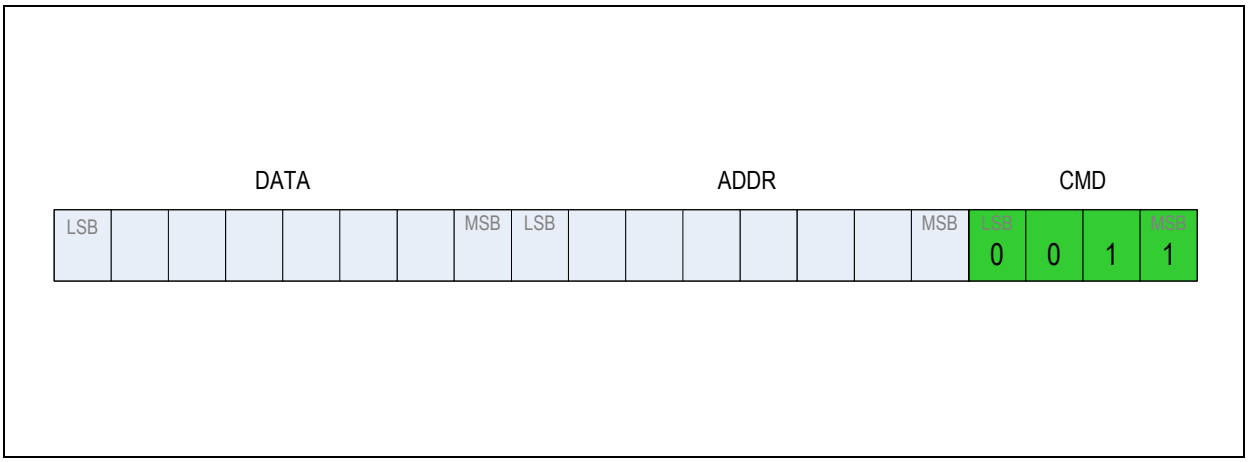
Table 17 shows the possible readable data information for the AS5163 device.

An even parity bit is used to guarantee a correct data transmission. The parity bit (P) is generated by the 16 data bits. The MSB of the CMD dummy (P) is reserved for the parity information.

8.1.11 WRITE

Figure 25 shows the format of the frame.

Figure 25. Frame Organization of the WRITE Command



The command consists of one frame received by the AS5163 (slave communication mode). The data byte will be written to the address. The access is performed with CMD field set to 0xC.

Table 17 shows the possible write data information for the AS5163 device.

Note: It is not recommended to access OTP memory addresses using this command.

8.2 OTP Programming Data

Table 16. OTP Data Organization

Data Byte	Bit Number	Symbol	Default	Description	
DATA15 (0x0F)	0	AMS_Test	FS	AMS Test Area	Factory Settings
	1	AMS_Test	FS		
	2	AMS_Test	FS		
	3	AMS_Test	FS		
	4	AMS_Test	FS		
	5	AMS_Test	FS		
	6	AMS_Test	FS		
	7	AMS_Test	FS		
DATA14 (0x0E)	0	AMS_Test	FS		
	1	AMS_Test	FS		
	2	AMS_Test	FS		
	3	AMS_Test	FS		
	4	ChipID<0>	FS	Chip ID	
	5	ChipID<1>	FS		
	6	ChipID<2>	FS		
	7	ChipID<3>	FS		
DATA13 (0x0D)	0	ChipID<4>	FS		
	1	ChipID<5>	FS		
	2	ChipID<6>	FS		
	3	ChipID<7>	FS		
	4	ChipID<8>	FS		
	5	ChipID<9>	FS		
	6	ChipID<10>	FS		
	7	ChipID<11>	FS		
DATA12 (0x0C)	0	ChipID<12>	FS		
	1	ChipID<13>	FS		
	2	ChipID<14>	FS		
	3	ChipID<15>	FS		
	4	ChipID<16>	FS		
	5	ChipID<17>	FS		
	6	ChipID<18>	FS		
	7	ChipID<19>	FS		

Table 16. OTP Data Organization

Data Byte	Bit Number	Symbol	Default	Description	
DATA11 (0x0B)	0	ChipID<20>	FS	Chip ID	
	1	MemLock_AMS	1	Lock of the Factory Setting Area	
	2	KD<0>	0	Kick Down Threshold	Customer Settings
	3	KD<1>	0		
	4	KD<2>	0		
	5	KD<3>	0		
	6	KD<4>	0		
	7	KD<5>	0		
DATA10 (0x0A)	0	ClampLow<0>	0	Clamping Level Low	
	1	ClampLow<1>	0		
	2	ClampLow<2>	0		
	3	ClampLow<3>	0		
	4	ClampLow<4>	0		
	5	ClampLow<5>	0		
	6	ClampLow<6>	0		
	7	DAC_MODE	0	DAC12/DAC10 Mode	
DATA9 (0x09)	0	ClampHi<0>	0	Clamping Level High	
	1	ClampHi<1>	0		
	2	ClampHi<2>	0		
	3	ClampHi<3>	0		
	4	ClampHi<4>	0		
	5	ClampHi<5>	0		
	6	ClampHi<6>	0		
	7	DIAG_HIGH	0	Diagnostic Mode, default=0 for Failure Band Low	
DATA8 (0x08)	0	OffsetIn<0>	0	Offset	
	1	OffsetIn<1>	0		
	2	OffsetIn<2>	0		
	3	OffsetIn<3>	0		
	4	OffsetIn<4>	0		
	5	OffsetIn<5>	0		
	6	OffsetIn<6>	0		
	7	OffsetIn<7>	0		

Table 16. OTP Data Organization

Data Byte	Bit Number	Symbol	Default	Description	
DATA7 (0x07)	0	OffsetIn<8>	0	Offset	Customer Settings
	1	OffsetIn<9>	0		
	2	OffsetIn<10>	0		
	3	OffsetIn<11>	0		
	4	OffsetIn<12>	0		
	5	OffsetIn<13>	0		
	6	OP_Mode<0>	0	Selection of Analog='00' or PWM Mode='01'	
	7	OP_Mode<1>	0		
DATA6 (0x06)	0	OffsetOut<0>	0	Output Offset	
	1	OffsetOut<1>	0		
	2	OffsetOut<2>	0		
	3	OffsetOut<3>	0		
	4	OffsetOut<4>	0		
	5	OffsetOut<5>	0		
	6	OffsetOut<6>	0		
	7	OffsetOut<7>	0		
DATA5 (0x05)	0	OffsetOut<8>	0		
	1	OffsetOut<9>	0		
	2	OffsetOut<10>	0		
	3	OffsetOut<11>	0		
	4	KDHYS<0>	0	Kick Down Hysteresis	
	5	KDHYS<1>	0		
	6	PWM Frequency<0>	0	Select the PWM frequency (4 frequencies)	
	7	PWM Frequency<1>	0		
DATA4 (0x04)	0	BP<0>	0	Break Point	
	1	BP<1>	0		
	2	BP<2>	0		
	3	BP<3>	0		
	4	BP<4>	0		
	5	BP<5>	0		
	6	BP<6>	0		
	7	BP<7>	0		

Table 16. OTP Data Organization

Data Byte	Bit Number	Symbol	Default	Description	
DATA3 (0x03)	0	BP<8>	0	Break Point	Customer Settings
	1	BP<9>	0		
	2	BP<10>	0		
	3	BP<11>	0		
	4	BP<12>	0		
	5	BP<13>	0		
	6	FAST_SLOW	0	Output Data Rate	
	7	EXT_RANGE	0	Enables a wider z-Range	
DATA2 (0x02)	0	Gain<0>	0	Gain	
	1	Gain<1>	0		
	2	Gain<2>	0		
	3	Gain<3>	0		
	4	Gain<4>	0		
	5	Gain<5>	0		
	6	Gain<6>	0		
	7	Gain<7>	0		
DATA1 (0x01)	0	Gain<8>	0	Gain	
	1	Gain<9>	0		
	2	Gain<10>	0		
	3	Gain<11>	0		
	4	Gain<12>	0		
	5	Gain<13>	0		
	6	Invert_Slope	0	Clockwise /Counterclockwise rotation	
	7	Lock_OTPCUST	0	Customer Memory Lock	
DATA0 (0x00)	0	redundancy<0>	0	Redundancy Bits	
	1	redundancy<1>	0		
	2	redundancy<2>	0		
	3	redundancy<3>	0		
	4	redundancy<4>	0		
	5	redundancy<5>	0		
	6	redundancy<6>	0		
	7	redundancy<7>	0		

Note: Factory settings (FS) are used for testing and programming at AMS. These settings are locked (only read access possible).

Data Content.

- Redundancy (7:0): For a better programming reliability, a redundancy is implemented. In case the programming of one bit fails, then this function can be used. With an address (7:0) one bit can be selected and programmed.

Redundancy Code	OTP Bit Selection
Redundancy <7:0> in decimal	
0	none
1	OP_Mode<1>
2	DIAG_HIGH
3	PWM Frequency<0>
4 - 10	ClampHi<6> - ClampHi<0>
11 - 17	ClampLow<6> - ClampLow<0>
18	OP_Mode<0>
19 - 32	OffsetIn<13> - OffsetIn<0>
33 - 46	Gain<13> - Gain<0>
47 - 60	BP<13> - BP<0>
61 - 72	OffsetOut<11> - OffsetOut<0>
73	Invert_Slope
74	FAST_SLOW
75	EXT_RANGE
76	DAC_MODE
77	Lock_OTPCUST
78 - 83	KD<5> - KD<0>
84 - 85	KDHYS<1> - KDHYS<0>
86	PWM Frequency<1>

- Lock_OTPCUST = 1, locks the customer area in the OTP and the device is starting up from now on in operating mode.
- Invert_Slope = 1, inverts the output characteristic in analog output mode.
- Gain (7:0): With this value one can adjust the steepness of the output slope.
- EXT_RANGE = 1, provides a wider z-Range of the magnet by turning off the alarm function.
- FAST_SLOW = 1, improves the noise performance due to internal filtering.
- BP (13:0): The breakpoint can be set with resolution of 14 bit.
- PWM Frequency (1:0): Four different frequency settings are possible. Please refer to Table 11.
- KDHYS (1:0): Avoids flickering at the KDOWN output (pin 11). For settings, refer to Table 13.
- OffsetOut (11:0): Output characteristic parameter
- ANALOG_PWM = 1, selects the PWM output mode.
- OffsetIn (13:0): Output characteristic parameter
- DIAG_HIGH = 1: In case of an error, the signal goes into high failure-band.
- ClampHI (6:0): Sets the clamping level high with respect to VDD.
- DAC_MODE disables filter at DAC
- ClampLow (6:0): Sets the clamping level low with respect to VDD.
- KD (5:0): Sets the kick-down level with respect to VDD.

8.2.1 Read / Write User Data

Table 17. Read / Write Data

Area Region	Address	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
R/W User Data	0x10	16	CORDIC_OUT[7:0]							
	0x11	17	0	0	CORDIC_OUT[13:8]					
	0x12	18	OCF	COF	0	0	0	0	DSP_RES	R1K_10K
	0x17	23	AGC_VALUE[7:0]							

Read only
Read and Write

Data Content:

Data only for read:

- CORDIC_OUT(13:0): 14-bit absolute angular position data.
- OCF (Offset Compensation Finished): logic high indicates the finished Offset Compensation Algorithm. As soon as this bit is set, the AS5163 has completed the startup and the data is valid.
- COF (Cordic Overflow): Logic high indicates an out of range error in the CORDIC part. When this bit is set, the CORDIC_OUT(13:0) data is invalid. The absolute output maintains the last valid angular value. This alarm may be resolved by bringing the magnet within the X-Y-Z tolerance limits.
- AGC_VALUE (7:0): magnetic field indication.

Data for write and read:

- DSP_RES resets the DSP part of the AS5163 the default value is 0. This is active low. The interface is not affected by this reset.
- R1K_10K defines the threshold level for the OTP fuses. This bit can be changed for verification purpose. A verification of the programming of the fuses is possible. The verification is mandatory after programming.

8.2.2 Programming Procedure

Note: After programming the OTP fuses, a verification is mandatory. The procedure described below must be strictly followed to ensure properly programmed OTP fuses.

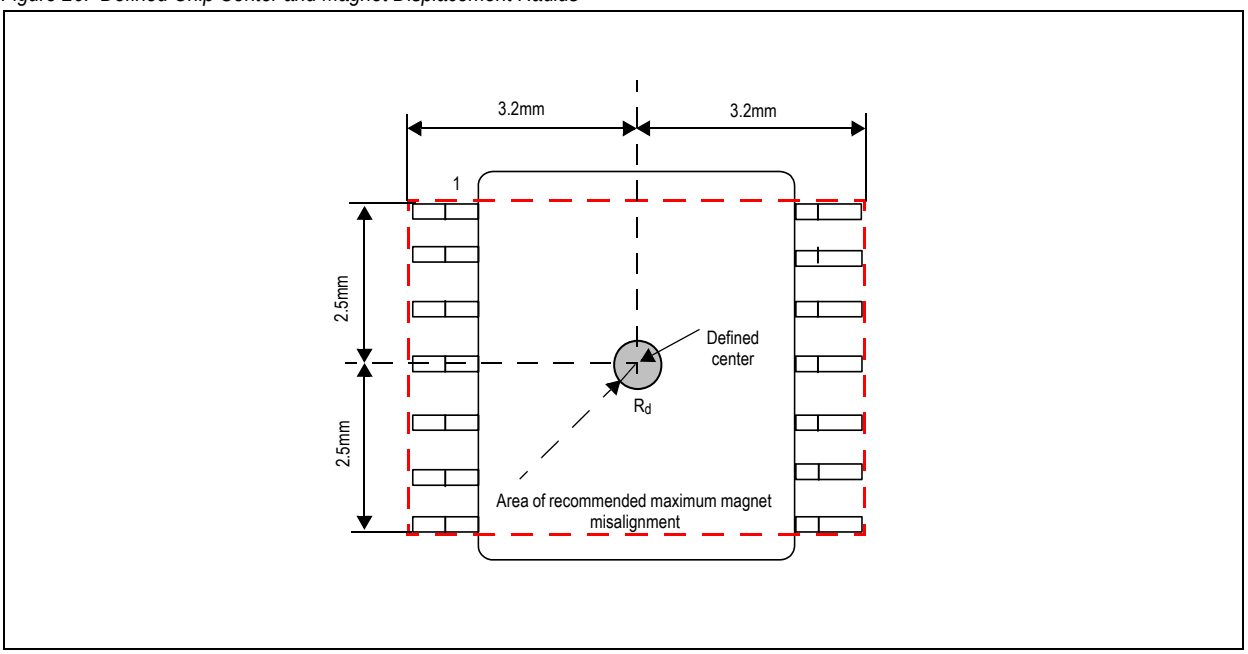
- Pull-up / Pull-down on OUT pin
- VDD=5V
- Wait startup time, device enters communication mode
- Write128 command: The trimming bits are written in the SFR memory.
- Read128 command: The trimming bits are read back.
- Upload command: The SFR memory is transferred into the OTP RAM.
- Fuse command: The OTP RAM is written in the Poly Fuse cells.
- Wait fuse time (6 ms)
- Write command (R1K_10K=1): Poly Fuse cells are transferred into the RAM cells compared with 10KΩ resistor.
- Download command: The OTP RAM is transferred into the SFR memory.
- Read128 command: The fused bits are read back.
- Write command (R1K_10K=0): Poly Fuse cells are transferred into the RAM cells compared with 1KΩ resistor.
- Download command: The OTP RAM is transferred into the SFR memory.
- Read128 command: The fused bits are read back.
- Pass2Func command or POR: Go to Functional mode.

For further information, please refer to Application Note AN5163-10 available at www.austriamicrosystems.com

8.2.3 Physical Placement of the Magnet

The best linearity can be achieved by placing the center of the magnet exactly over the defined center of the chip as shown in Figure 26.

Figure 26. Defined Chip Center and Magnet Displacement Radius



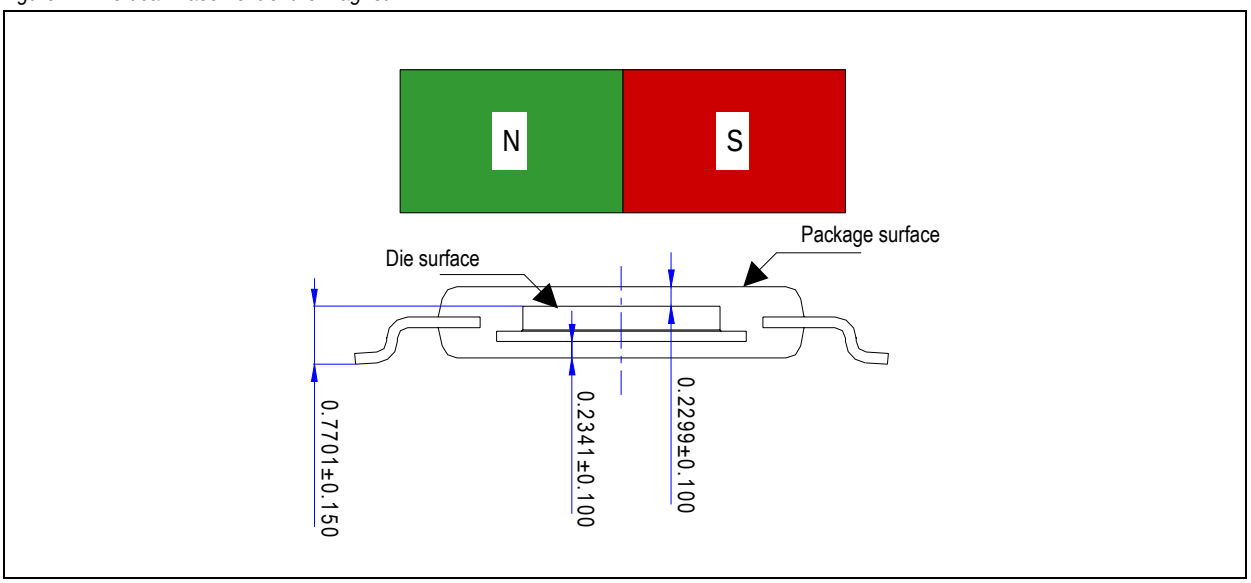
8.2.4 Magnet Placement

The magnet's center axis should be aligned within a displacement radius R_d of 0.25mm (larger magnets allow more displacement) from the defined center of the IC.

The magnet may be placed below or above the device. The distance should be chosen such that the magnetic field on the die surface is within the specified limits (see Figure 26). The typical distance "z" between the magnet and the package surface is 0.5mm to 1.5mm, provided the recommended magnet material and dimensions (6mm x 3mm) are used. Larger distances are possible, as long as, the required magnetic field strength stays within the defined limits.

However, a magnetic field outside the specified range may still produce usable results, but the out-of-range condition will be indicated by an alarm forcing the output into the failure band.

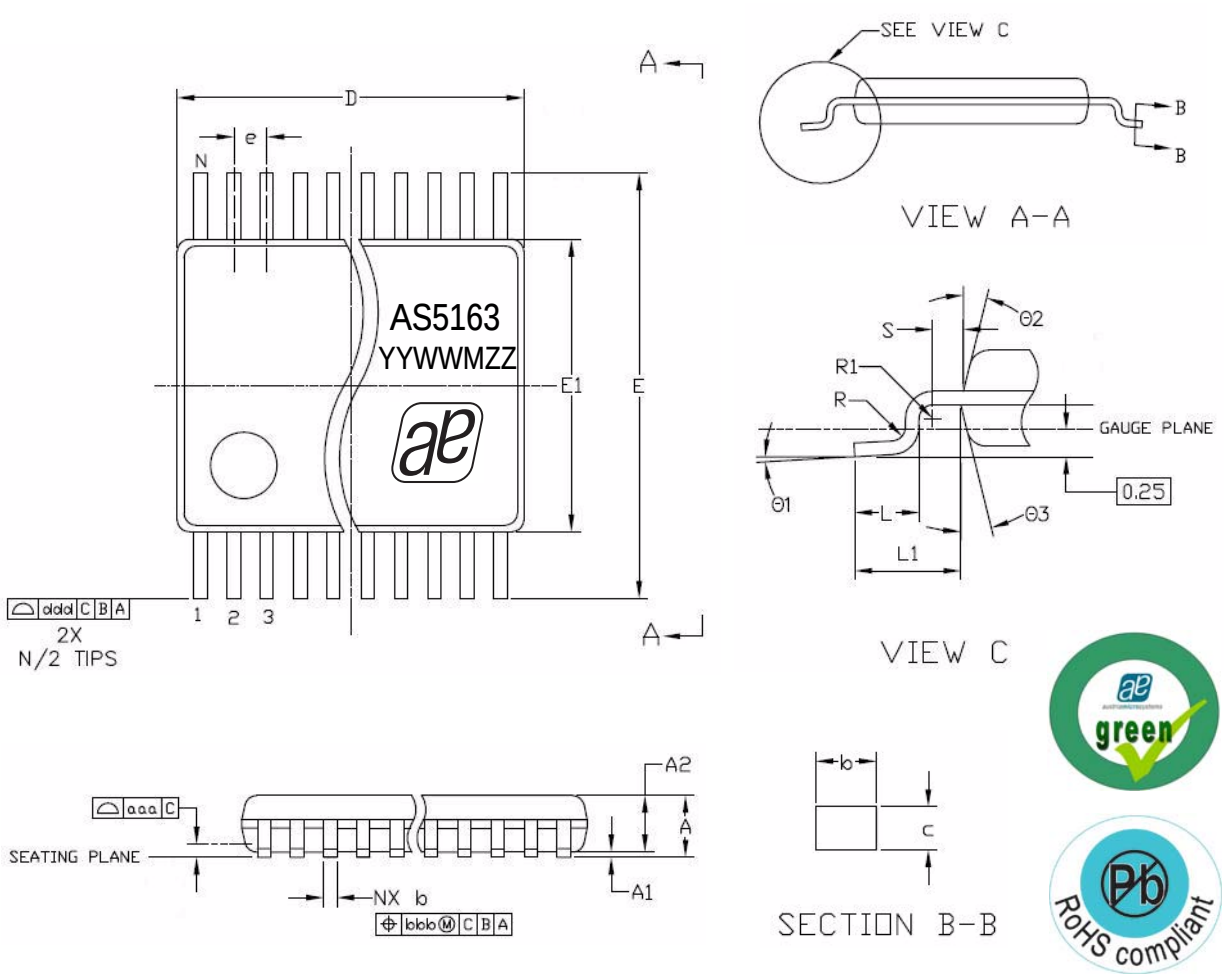
Figure 27. Vertical Placement of the Magnet



9 Package Drawings and Markings

The device is available in a 14-Lead Thin Shrink Small Outline Package.

Figure 28. Package Drawings and Dimensions



Symbol	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	5.00	5.10
E	-	6.40 BSC	-
E1	4.30	4.40	4.50
e	-	0.65 BSC	-
L	0.45	0.60	0.75
L1	-	1.00 REF	-

Symbol	Min	Typ	Max
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
Θ1	0°	-	8°
Θ2	-	12 REF	-
Θ3	-	12 REF	-
aaa	-	0.10	-
bbb	-	0.10	-
ccc	-	0.05	-
ddd	-	0.20	-
N	14		

Notes:

1. Dimensions and tolerancing confirm to *ASME Y14.5M-1994*.
2. All dimensions are in miilimeters. Angles are in degrees.

Marking: YYWWMZZ.

YY	WW	M	ZZ
Year (i.e. 04 for 2004)	Week	Assembly plant identifier	Assembly traceability code

JEDEC Package Outline Standard: MO - 153

Thermal Resistance $R_{th(j-a)}$: 89 K/W in still air, soldered on PCB

Revision History

Revision	Date	Owner	Description
0.1	Oct 06, 2008	apg	Initial version
1.1	Nov 04, 2008		Added package drawings and dimensions
2.4	May 31, 2010		Updated according to 2.4 specification document
	Jun 18, 2010		Changed DITH_DISABLE to DAC_MODE, updated Ordering Information.
2.5	Sep 21, 2010	rfu	Updated Absolute Maximum Ratings, Operating Conditions, Magnetic Input Specification, Electrical System Specifications, Figure 4, Table 9, Table 10, Table 14, Figure 11, Programming Procedure, Figure 28, Ordering Information. Deleted chapter on “Choosing the Proper Magnet”.
2.6	Oct 14, 2010	mub	Updated Section 6.3
2.7	Oct 28, 2010		Updated Table 5, Table 6, Table 10, Table 14, Table 15, page 29, Figure 28.

Note: Typos may not be explicitly mentioned under revision history.

10 Ordering Information

The devices are available as the standard products shown in Table 18.

Table 18. Ordering Information

Ordering Code	Description	Delivery Form	Package
AS5163-HTSV	12-Bit High Voltage Rotary Magnetic Encoder	Tubes	14-pin TSSOP
AS5163-HTSP		Tape & Reel	

Note: All products are RoHS compliant and austriamicrosystems green.
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