V105AJ8/9
(256K x 8, 256K x 9) CMOS WRITE-PER-BIT MEMORY MODULE

Features

- 262,144 x 8 (or x 9) bit organization
- Utilizes 256K x 4 (Write/Bit) and 256K x 1 CMOS DRAMs
- Fast Page mode operation
- Write-Per-Bit feature
- Fast access times 70 ns, 80 ns and 100 ns
- Low power dissipation
- Common $\overline{CAS}$ control for eight common Data-in and Data-out lines
- Separate $\overline{CAS}$ control for one separate pair of Data-in and Data-out (x 9 organization)
- Single 5 V ±10% supply
- All I/O are fully TTL compatible
- Standard 30-lead single-in-line module

Description

The V105AJ8/9 Memory Module is organized as 262,144 x 8 (or 9) bits in a 30-lead single-in-line module. The 256K x 8 memory module uses two Vitelic 256K x 4 (Write/Bit) DRAMs. The 256K x 9 memory module uses two Vitelic 256K x 4 (Write/Bit) DRAMs and one Vitelic 256K x 1 DRAM. The V105AJ8/9 has the Write-Per-Bit feature, allowing selected I/O bits to be written into memory while the unselected (masked) I/O bits are not written.

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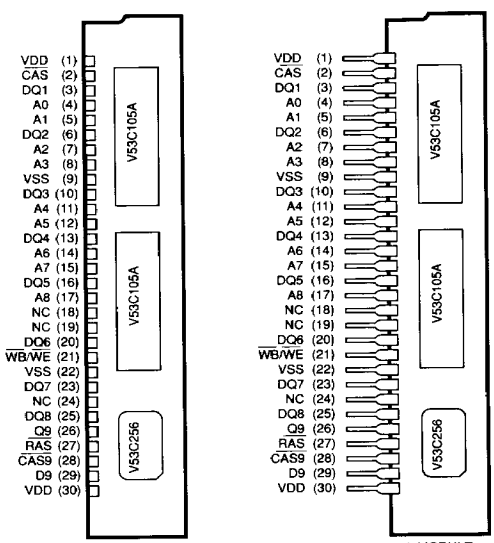
V105AJ
Pin Configuration
x 9 Organization



NOTE: *x 8 Organization*
Pins 26, 28, 29 are not connected

Device Usage Chart

Operating Temperature Range	Bit Organization		Module Type		Access Time (ns)			Power
	x 8	x 9	S	L	70	80	100	Std
0°C–70°C	•	•	•	•	•	•	•	•

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Part Number Information