ES25P80

8Mbit CMOS 3.0 Volt Flash Memory with 75Mhz SPI Bus Interface

ARCHITECTURAL ADVANTAGES

- **Single power supply operation**
  - 2.7V -3.6V for read and program operations
- **Memory Architecture**
  - Sixteen sectors with 512 Kb each
- **Program**
  - Page program (up to 256 bytes) in 1.5ms (typical)
  - Program cycles are on a page by page basis
- **Erase**
  - 0.5s typical sector erase time
  - 6s typical bulk erase time
- **Endurance**
  - 100,000 cycles per sector (typical)
- **Data Retention**
  - 20 years (typical)
- **Parameter Page**
  - 256 Byte page independent from main memory for parameter storage
  - Seperate from array, erase time < 20ms
- **Device ID**
  - JEDEC standard two-byte electronic signature
  - RES instruction one-byte electronic signature for backward compatibility
  - Manufacturer and device type ID
- **Process Technology**
  - Manufactured on 0.18um process technology
- **Package Option**
  - Industry Standard Pinouts
  - 8-pin SO (208mil) package
  - All Pb-Free devices are RoHS Compliant

PERFORMANCE CHARACTERISTICS

- **Speed**
  - 75Mhz clock rate (maximum)
- **Power Saving Standby Mode**
  - Standby mode 50uA (max)
  - Deep Power Down Mode 1uA (typical)

MEMORY PROTECTION FEATURES

- **Memory Protection**
  - W# pin works in conjunction with Status Register Bits to protect specified memory areas
  - Status Register Block Protection Bits (BP2, BP1, BP0) in status register configure parts of memory as read only

SOFTWARE FEATURES

- **SPI Bus Compatible Serial Interface**

GENERAL PRODUCT DESCRIPTION

The ES25P80 device is a 3.0 volt (2.7V to 3.6V) single power flash memory device. ES25P80 consists of Sixteen sectors, each with 512 Kb memory.

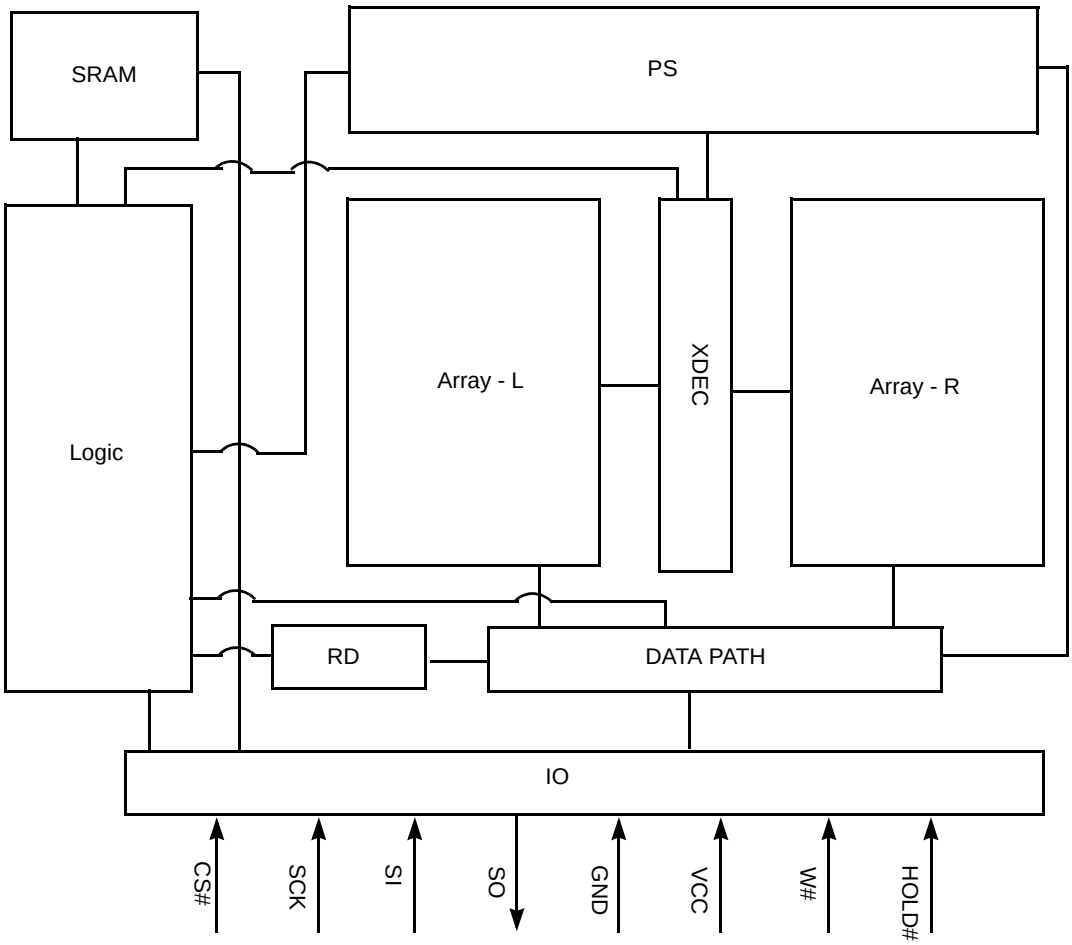
Data appears on SI input pin when inputting data into the memory and on the SO output pin when outputting data from the memory. The devices are designed to be programmed in-system with the standard system 3.0 volt Vcc supply.

The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction.

The memory supports Sector Erase and Bulk Erase instructions.

Each device requires only a 3.0 volt power supply (2.7V to 3.6V) for both read and write functions. Internally generated and regulated voltages are provided for program operations. This device does not require Vpp supply.

BLOCK DIAGRAM

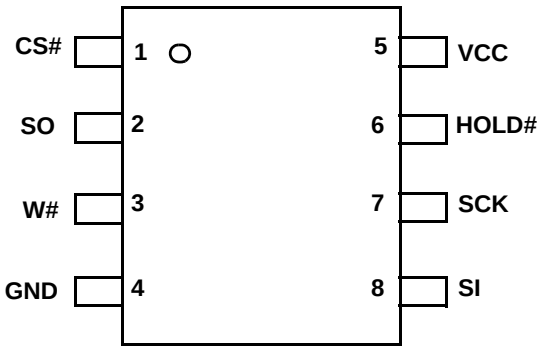


PIN DESCRIPTIONS

Pin	Description
SCK	Serial Clock Input
SI	Serial Data Input
SO	Serial Data Output
CS#	Chip Select Input
W#	Write Protect Input
HOLD#	Hold Input
Vcc	Supply Voltage Input
GND	Ground Input

Connection Diagrams

8-pin Plastic Small Outline Package (SO)



SIGNAL DESCRIPTION

Serial Data Output (SO)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (SCK).

Serial Data Input (SI)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of Serial Clock (SCK).

Serial Clock (SCK)

This input signal provides the timing of the serial interface. Instructions, addresses, and data present at the Serial Data Input (SI) are latched on the rising edge of Serial Clock (SCK). Data on Serial Data Output (SO) changes after the falling edge of Serial Clock (SCK).

Chip Select (CS#)

When this input signal is high, the device is deselected and Serial Data Output (SO) is at high impedance. Unless an internal Program, Erase or Write Status Register cycle is in progress, the device will be in Standby mode. Driving Chip Select (CS#) Low enables the device, placing it in the active power mode.
After power-up, a falling edge on Chip Select (CS#) is required prior to the start of any instruction.

Hold (HOLD#)

The Hold (HOLD#) signal is used to pause any serial communications with the device without deselecting the device.
During the Hold instruction, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (SCK) are Don't Care.
To start the Hold condition, the device must be selected, with Chip Select (CS#) driven Low.

Write Protect (W#)

The main purpose of this input signal is to freeze the size of the area of memory that is protected against program or erase instructions (as specified by the values in the BP2, BP1 and BP0 bits of the Status Register).

SPI MODES

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes :

CPOL = 0, CPHA = 0
CPOL = 1, CPHA = 1

For these two modes, input data is latched in on the rising edge of Serial Clock (SCK), and output data is available from the falling edge of Serial Clock (SCK).

The difference between the two modes, as shown in Figure 1, is the clock polarity when the bus master is in Standby and not transferring data:

SCK remains at 0 for (CPOL = 0, CPHA = 0)
SCK remains at 1 for (CPOL = 1, CPHA = 1)

OPERATING FEATURES

All data into and out of the device is shifted in 8-bit chunks.

Page Programming

To program one data byte, two instructions are required : Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. This is followed by the internal program cycle. To spread this overhead, the Page Program (PP) instruction allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0), provided that they lie in consecutive addresses on the same page of memory.

Sector Erase, or Bulk Erase

The Page Program (PP) instruction allows bits to be programmed from 1 to 0. Before this can be applied, the bytes of the memory need to be first erased to all 1's (FFh) before any programming. This can be achieved in two ways :1) a sector at a time using the Sector Erase (SE) instruction, or 2) throughout the entire memory, using the Bulk Erase (BE) instruction.

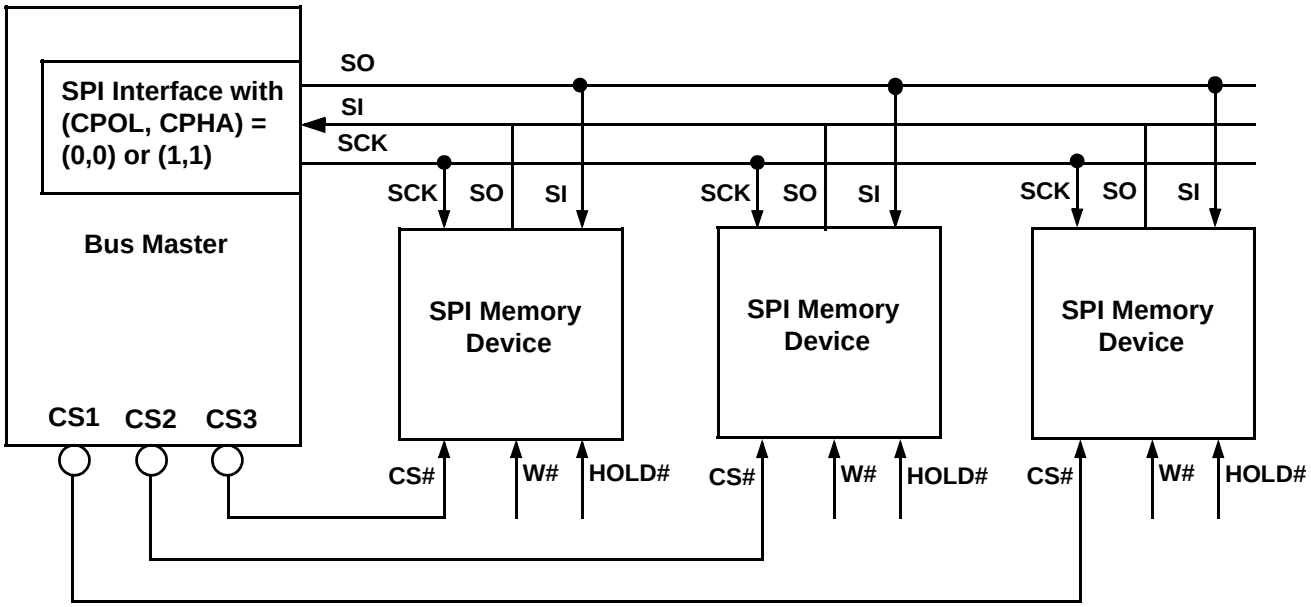


Figure 1. Bus Master and Memory Devices on the SPI Bus

Note : *The Write Protect (W#) and Hold (HOLD#) signals should be driven, High or Low as appropriate*

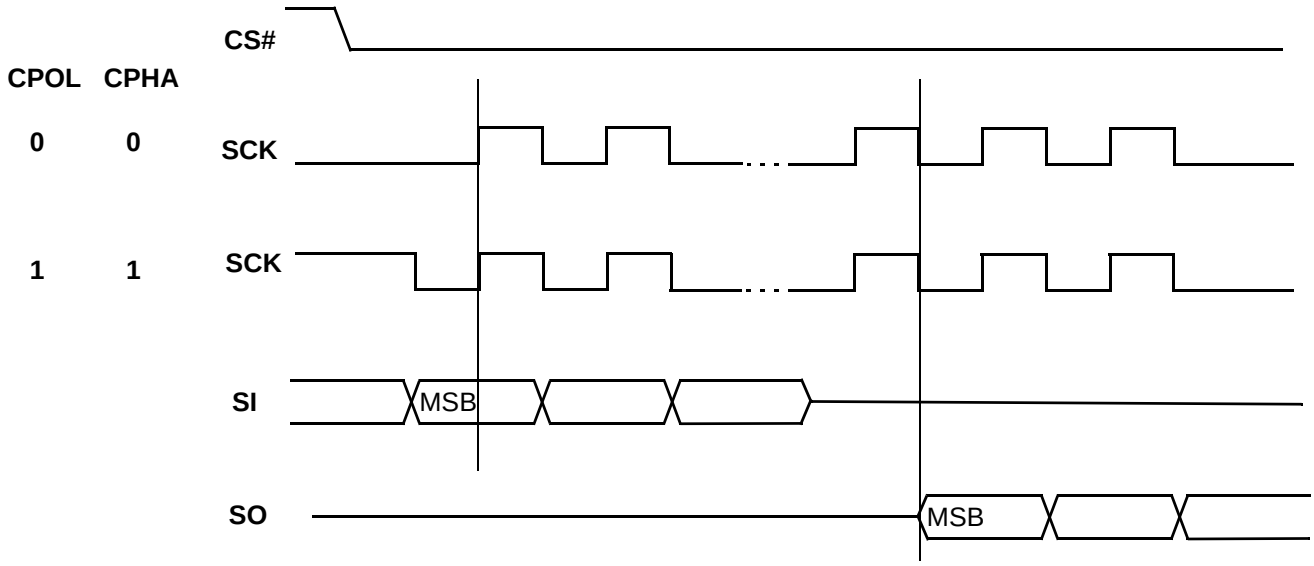


Figure 2. SPI Modes Supported

Polling During a Write, Program, or Erase Cycle

A further improvement in the time to Write Status Register (WRSR), Program(PP) or Erase (SE or BE) can be achieved by not waiting for the worst-case delay. The Write in Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous Write cycle, Program cycle, or Erase cycle is complete.

Active Power and Standby Power Modes

When Chip Select (CS#) is Low, the device is enabled, and in the Active Power mode. When Chip Select (CS#) is High, the device is disabled, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, Write Status Register). The device then goes into the Standby Power mode. The device consumption drops to I_{SB}. This can be used as an extra Deep Power Down on mechanism, when the device is not in active use, to protect the device from inadvertent Write, Program, or Erase instructions.

Status Register

The Status Register contains a number of status and control bits, as shown in Figure 7, that can be read or set (as appropriate) by specific instructions

WIP bit
The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle.

WEL bit
The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch.

BP2, BP1, BP0 bits
The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions.

SRWD bit
The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect (W#) signal. The Status Register Write Disable (SRWD) bit and Write Protect (W#) signal allow the device to be put in the Hardware Protected mode. In this mode, the non-volatile bits of the Status Register (SRWD, BP2, BP1, BP0) become read-only bits.

Hold Condition Modes

The Hold (HOLD#) signal is used to pause any serial communications with the device without resetting the clocking sequence. Hold (HOLD#) signal gates the clock input to the device. However, taking this signal Low does not terminate any Write Status Register, Program or Erase cycle that is currently in progress.

To enter the Hold condition, the device must be selected, with Chip Select (CS#) Low. The Hold condition starts on the falling edge of the Hold (HOLD#) signal, provided that this coincides with Serial Clock (SCK) being Low (as shown in Figure 3).

The Hold condition ends on the rising edge of the Hold (HOLD#) signal, provided that this coincides with Serial Clock (SCK) being Low.

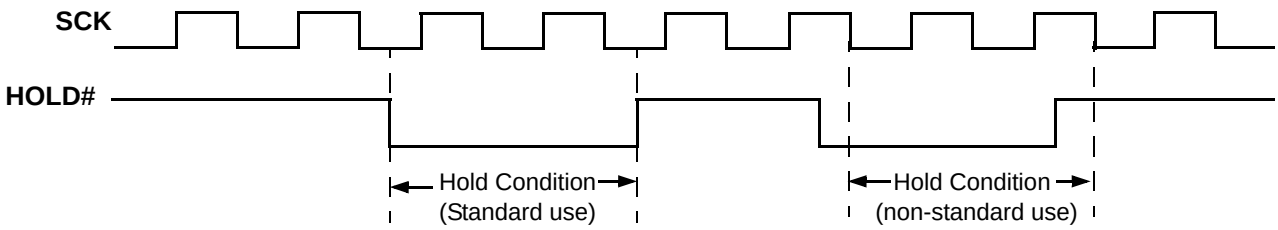


Figure 3. Hold Condition Activation

If the falling edge does not coincide with Serial Clock (SCK) being Low, the Hold condition starts after Serial Clock (SCK) next goes Low. Similarly, If the rising edge does not coincide with Serial Clock (SCK) being Low, the Hold condition ends after Serial Clock (SCK) next goes Low (Figure 3).

During the Hold condition, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (SCK) are Don't Care.

Normally, the device remains selected, with Chip Select (CS#) driven Low, for the entire duration of the Hold condition. This ensures that the state of the internal logic remains unchanged from the moment of entering the Hold condition.

If Chip Select (CS#) goes High while the device is in the Hold condition, this has the effect of resetting the internal logic of the device. To restart communication with the device, it is necessary to drive Hold (HOLD#) High, and then to drive Chip Select (CS#) Low. This prevents the device from going back to the Hold condition.

Protection Modes

The SPI memory device boasts the following data protection mechanisms

1) All instructions that modify data must be preceded by a Write Enable(WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events :

- Power-up
- WRDI instruction completion
- WRSR instruction completion
- PP instruction completion
- SE instruction completion
- BE instruction completion

2) The Block Protect (BP2, BP1, BP0) bits allow part of the memory to be configured as read-only. This is the Software Protected Mode (SPM).

3) The Write Protect (W#) signal works in cooperation with the Status Register Write Disable (SRWD) bit to enable write-protection. This is the Hardware Protected Mode (HPM).

4) Program, Erase and Write Status Register instructions are checked to verify that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.

Table 1. Protected Area Sizes

Protected Memory Area (Top Level)	Status Register Content			Memory Content	
	BP2 Bit	BP1 Bit	BP0 Bit	Protected Area	Unprotected Area
0	0	0	0	none	00000 ~ FFFFF
1 / 16	0	0	1	F0000 ~ FFFFF	00000 ~ EFFFF
1 / 8	0	1	0	E0000 ~ FFFFF	00000 ~ DFFFF
1 / 4	0	1	1	C0000 ~ FFFFF	00000 ~ BFFFF
1 / 2	1	0	0	80000 ~ FFFFF	00000 ~ 7FFFF
All	1	0	1	00000 ~ FFFFF + parameter page	none
All	1	1	0	00000 ~ FFFFF + parameter page	none
All	1	1	1	00000 ~ FFFFF + parameter page	none

MEMORY ORGANIZATION

The memory is organized as :

- ES25P80 : Sixteen sectors of 512 Kbit each
- Each page can be individually programmed (bits are programmed from 1 to 0).
- The device is Sector or Bulk erasable (bits are erased from 0 to 1)

Table 2. Sector Address

Sector	Address Range	
SA15	F0000h	FFFFFh
SA14	E0000h	EFFFFh
SA13	D0000h	DFFFFh
SA12	C0000h	CFFFFh
SA11	B0000h	BFFFFh
SA10	A0000h	AFFFFh
SA9	90000h	9FFFFh
SA8	80000h	8FFFFh
SA7	70000h	7FFFFh
SA6	60000h	6FFFFh
SA5	50000h	5FFFFh
SA4	40000h	4FFFFh
SA3	30000h	3FFFFh
SA2	20000h	2FFFFh
SA1	10000h	1FFFFh
SA0	00000h	0FFFFh

INSTRUCTIONS

All instructions, addresses, and data are shifted in and out of the device, starting with the most significant bit. Serial Data Input (SI) is sampled on the first rising edge of Serial Clock (SCK) after Chip Select (CS#) is driven Low. Then, the one byte instruction code must be shifted in to the device, most significant bit first, on Serial Data Input (SI), each bit being latched on the rising edges of Serial Clock (SCK). The instruction set is listed in Table 3.

Every instruction sequence starts with a one byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none. Chip Select (CS#) must be driven High after the last bit of the instruction sequence has been shifted in.

In the case of a Read Data Bytes (READ), Read Status Register (RDSR), Read Data Bytes at higher speed (FAST_READ), Read Identification (RDID) , Read Manufacturer and Device ID (RDMD), Read Parameter Page (RDPARA) and Fast Read Parameter Page (FRDPARA) instructions, the shifted-in instruction sequence is followed by a data-out sequence.

Chip Select (CS#) can be driven High after any bit of the data-out sequence is being shifted out to terminate the transaction.

In the case of a Page Program (PP), Program Parameter Page (PPP), Sector Erase (SE), Bulk Erase (BE), Parameter Page Erase(PE), Write Status Register (WRSR), Write Enable (WREN), Deep Power Down (DP) or Write Disable (WRDI) instruction, Chip Select (CS#) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select (CS#) must driven High when the number of clock pulses after Chip Select (CS#) being driven Low is an exact multiple of eight.

All attempts to access the memory array during a Write Status Register cycle, Program cycle or Erase cycle are ignored, and the internal Write Status Register cycle, Program cycle or Erase cycle continues unaffected.

Table 3. Instruction Set

Instruction	Description	One-Byte Instruction Code	Address Bytes	Dummy Byte	Data Bytes
Status Register Operations					
WREN	Write Enable	06H (0000 0110)	0	0	0
WRDI	Write Disable	04H (0000 0100)	0	0	0
RDSR	Read from Status Register	05H (0000 0101)	0	0	1 to Infinity
WRSR	Write to Status Register	01H (0000 0001)	0	0	1
Read Operations					
READ	Read Data Bytes	03H (0000 0011)	3	0	1 to Infinity
FAST_READ	Read Data Bytes at Higher Speed	0BH (0000 1011)	3	1	1 to Infinity
RDID	Read Identification	9FH (1001 1111)	0	0	1 to 3
RDMD	Read Manufacturer and Device ID	90H (1001 0000)	0	3	1 to Infinity
RDPARA	Read Parameter Page	53H (0101 0011)	3	0	1 to Infinity
FRDPARA	Fast Read Parameter Page	5BH (0101 1011)	3	1	1 to Infinity
Erase Operations					
SE	Sector Erase	D8H (1101 1000)	3	0	0
BE	Bulk (Chip) Erase	C7H (1100 0111)	0	0	0
PE	Erase Parameter Page	D5H (1101 0101)	0	0	0
Program Operations					
PP	Page Program	02H (0000 0010)	3	0	1 to 256
PPP	Program Parameter Page	52H (0101 0010)	3	0	1 to 256
Deep Power Down Savings Mode Operations					
DP	Deep Power Down	B9H (1011 1001)	0	0	0
RES	Release from Deep Power Down	ABH (1010 1011)	0	0	0
	Release from Deep Power Down and Read Electronic Signature	ABH (1010 1011)	0	3	1 to Infinity

Write Enable (WREN)

The Write Enable (WREN) instruction (Figure 4) sets the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP or PPP), Erase (SE, BE or PE) and Write Status Register (WRSR) instruction. The Write Enable (WREN) instruction is entered by driving Chip Select (CS#) Low, sending the instruction code, and then driving Chip Select (CS#) High.

Write Disable (WRDI)

The Write Disable (WRDI) instruction (Figure 5) resets the Write Enable Latch (WEL) bit. The Write Disable (WRDI) instruction is entered by driving Chip Select (CS#) Low, sending the instruction code, and then driving Chip Select (CS#) High.

The Write Enable (WEL) bit is reset under the following conditions :

- Power-up
- WRDI instruction completion
- WRSR instruction completion
- PP instruction completion
- SE instruction completion
- BE instruction completion

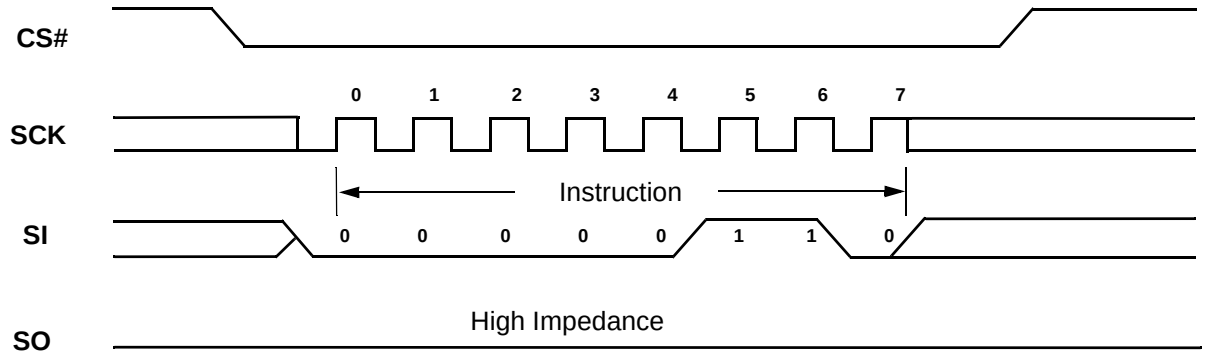


Figure 4. Write Enable (WREN) Instruction Sequence

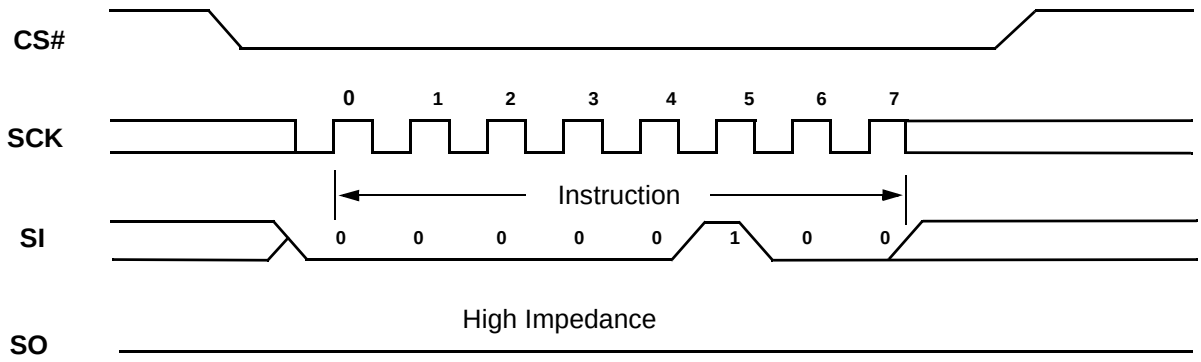


Figure 5. Write Disable (WRDI) Instruction Sequence

Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Program, Erase, or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in Figure 6.

The status and control bits of the Status Register are as follows :

WIP bit
The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle. This bit is a read only bit and is read by executing a RDSR instruction. If this bit is 1, such a cycle is in progress, if it is 0, no such cycle is in progress.

WEL bit
The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1, the internal Write Enable Latch is set; when set to 0, the internal Write Enable Latch is reset and no Write Status Register, Program or Erase instruction is accepted.

BP2, BP1, BP0 bits
The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP2, BP1, BP0) bits is set to 1, the relevant memory area (as defined in Table 1) becomes protected against Page Program (PP), and Sector Erase (SE) instructions. The Block Protect (BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Bulk Erase (BE) instruction is executed if, and only if, all Block Protect (BP2, BP1, BP0) bits are 0.

SRWD bit
The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect (W#) signal. The Status Register Write Disable (SRWD) bit and Write Protect (W#) signal allow the device to be put in the Hardware Protected mode (when the Status Register Write Disable (SRWD) bit is set to 1, and Write Protect (W#) is driven Low). In this mode, the non-volatile bits of the Status Register (SRWD, BP2, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

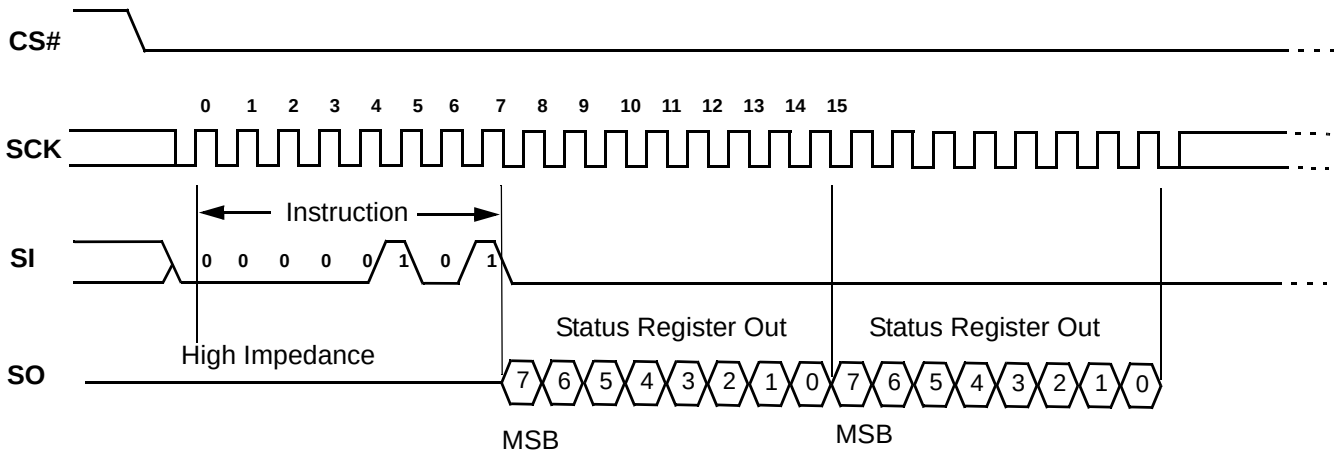


Figure 6. Read Status Register (RDSR) Instruction Sequence

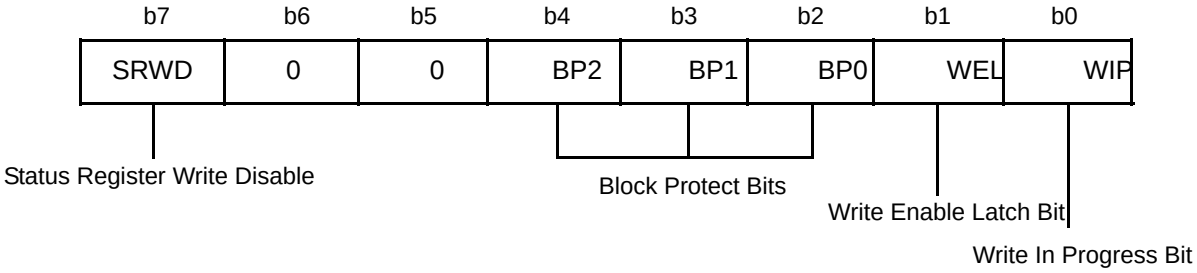


Figure 7. Status Register Format

Write Status Register (WRSR)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code and the data byte on Serial Data Input (SI).

The instruction sequence is shown in Figure 8.

The Write Status Register (WRSR) instruction has no effect on bits b6, b5, b1 and b0 of the Status Register. Bits b6, b5 are always read as 0.

Chip Select (CS#) must be driven High after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) instruction is not executed.

As soon as Chip Select (CS#) is driven High, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) instruction allows the user to change the values of the Block Protect (BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table 1. The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Write Disable (SRWD) bit in accordance with the Write Protect (W#) signal. The Status Register Write Disable (SRWD) bit and Write Protect (W#) signal allow the device to be put in the Hardware Protected Mode (HPM). The Write Status Register (WRSR) instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

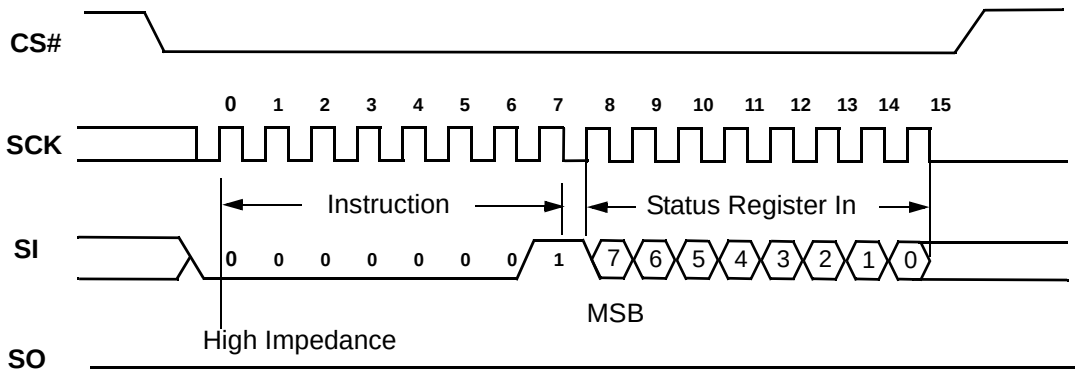


Figure 8. Write Status Register (WRSR) Instruction Sequence

Table 4. Protection Modes

W# Signal	SRWD Bit	Mode	Write Protection of the Status Register	Protected Area (See Note)	Unprotected Area (See Note)
1	1	Software Protected (SPM)	Status Register is Writable (if the WREN instruction has set the WEL bit). The values in the SRWD, BP2, BP1 and BP0 bits can be changed.	Protected against Page Program and Erase(SE, BE,PE)	Ready to accept Page Program and Sector Erase Instructions
1	0				
0	0				
0	1	Hardware Protected (HPM)	Status Register is Hardware write protected. The values in the SRWD, BP2, BP1 and BP0 bits cannot be changed	Protected against Page Program and Erase (SE,BE,PE)	Ready to accept Page Program and Sector Erase Instructions

Note:

1. As defined by the values in the Block Protected (BP2, BP1, BP0) bits of the Status Register, as shown in Table 1.

The protection features of the device are summarized in Table 4.

When the Status Register Write Disable (SRWD) bit of the Status Register is 0 (its initial delivery state), it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction, regardless of the whether Write Protect (W#) is driven High or Low.

When the Status Register Write Disable (SRWD) bit of the Status Register is set to 1, two cases need to be considered, depending on the state of Write Protect (W#).

1) If Write Protect (W#) is driven High, it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction.

2) If Write Protect (W#) is driven Low, it is not possible to write to the Status Register even if the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction. (Attempts to write to the Status Register are rejected, and are not accepted for execution).

As a consequence, all the data bytes in the memory area that are software protected (SPM) by the Block Protect (BP2, BP1, BP0) bits of the Status Register, are also hardware protected against data modification.

Regardless of the order of the two events, the Hardware Protected Mode (HPM) can be entered :

1) by setting the Status Register Write Disable (SRWD) bit after driving Write Protect (W#) Low

2) or by driving Write Protect (W#) Low after setting the Status Register Write Disable (SRWD) bit.

The only way to exit the Hardware Protected Mode (HPM) once entered is to pull Write Protect (W#) High.

If Write Protect (W#) is permanently tied High, the Hardware Protected Mode (HPM) can never be activated, and only the Software Protected Mode (SPM), using the Block Protect (BP2, BP1, BP0) bits of the Status Register, can be used.

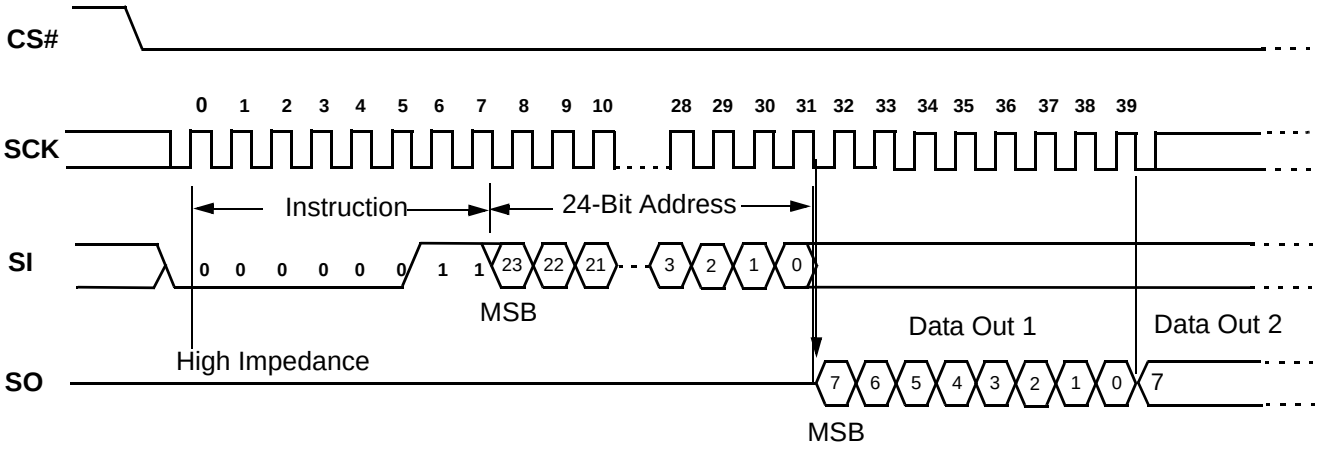


Figure 9. Read Data Bytes (READ) Instruction Sequence

Read Data Bytes (READ)

The READ instruction reads the memory at the specified SCK frequency (fsck) with a maximum speed of 40MHz.

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23 - A0), each bit being latched-in during the rising edge of Serial Clock (SCK). Then the memory contents, at the address, are shifted out on Serial Data Output (SO), each bit being shifted out, at a frequency fsck, during the falling edge of Serial Clock (SCK).

The instruction sequence is shown in Figure 9. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 00000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes (READ) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes (READ) instruction, while a Program, Erase, or Write cycle is in progress, is rejected without having any effect on the cycle that is in progress.

Read Data Bytes at Higher Speed (FAST_ READ)

The FAST_READ instruction reads the memory at the specified SCK frequency (fsck) with a maximum speed of 75 MHz. The device is first selected by driving Chip Select (CS#) Low. The instruction code for FAST_READ instruction is followed by a 3-byte address (A23 - A0) and a dummy byte, each bit being latched in during the rising edge of Serial Clock (SCK). Then the memory contents, at that address, are shifted out on Serial Data Output (SO), each bit being shifted out. at a maximum frequency Fsck, during the falling edge of Serial Clock (SCK).

The instruction sequence is shown in Figure 10. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single FAST_READ instruction.
When the highest address is reached, the address counter rolls over to 00000h, allowing the read sequence to be continued indefinitely

The FAST_READ instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any FAST_READ instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

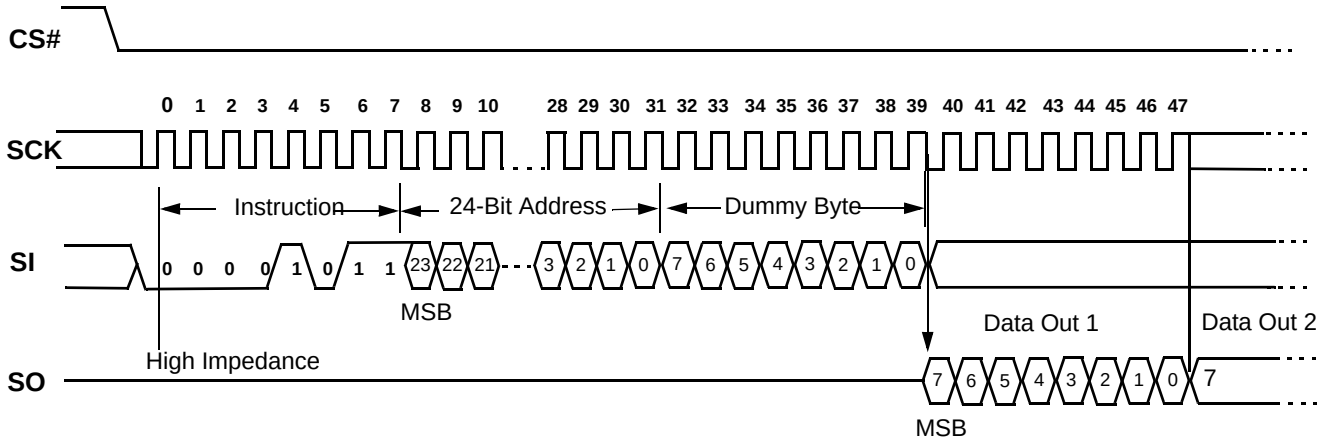


Figure 10. Read Data Bytes at Higher Speed (FAST_READ) Instruction Sequence

Read Identification (RDID)

The Read Identification (RDID) instruction allows the 8-bit manufacturer identification to be read, followed by two bytes of the device identification.

The manufacturer identification byte is assigned by JEDEC, and has a value of 4Ah for ESI products. The device identification is assigned by the device manufacturer, and indicates the memory type in the first byte (20h), and the memory capacity of the device in the second byte (14h).

Any Read Identification (RDID) instruction executed while an Erase, Program, or Write Status Register cycle is in progress is not decoded, and has no effect on the cycle that is in progress.

The device is first selected by driving Chip Select (CS#) Low. Then, the 8-bit instruction code for the instruction is shifted in, with each bit being latched in on SI during the rising edge of SCK.

This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output (SO), with each bit being shifted out during the falling edge of Serial Clock (SCK).

The instruction sequence is shown in Figure 11.

Driving CS# high after the Device Identification has been read at least once terminates the READ_ID instruction. The Read Identification (RDID) instruction can also be terminated by driving CS# High at any time during data output. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions

Manufacturer Identification	Device Identification	
	Memory Type	Memory Capacity
4Ah	20h	14h

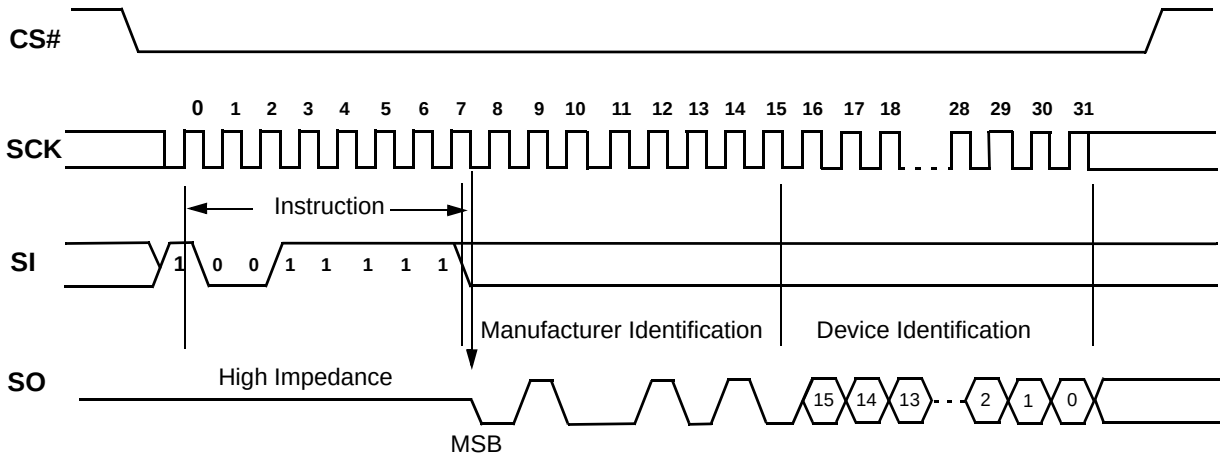


Figure 11. Read Identification (RDID) Instruction Sequence and Data-Out Sequence

Read Manufacturer ID & Device ID (RDMD)

The Read Manufacturer ID & Device ID (RDMD) instruction is an alternative to the Release from Power-down/Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer ID & Device ID (RDMD) instruction is very similar to the Release from Power-down/Device ID instruction.

The instruction is initiated by driving the CS# pin low and shift the instruction code “90h” followed by three dummy bytes. After which, the Manufacturer ID for ESI (4Ah) and the Device ID (13h) are shifted out on the falling edge SCLK with most significant bit (MSB) first as shown in Figure 12. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# pin.

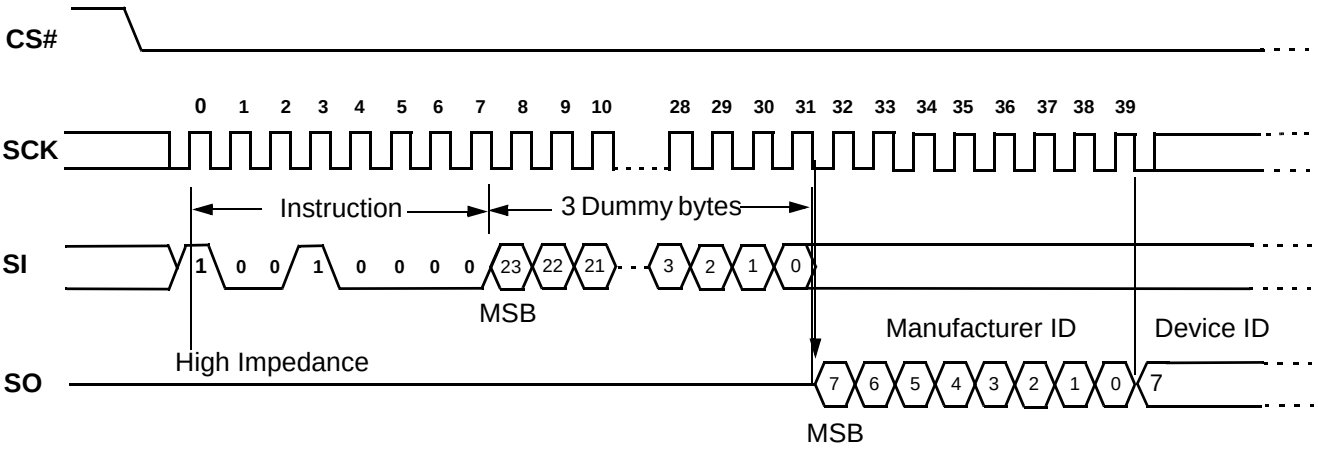


Figure 12. Read Manufacturer ID & Device ID (RDMD) Instruction Sequence and Data-Out Sequence

Page Program (PP)

The Page Program (PP) instruction allows bytes to be programmed in the memory (changing from 1 to 0). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Program (PP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, three address bytes and at least one data byte on Serial Data Input (SI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 13.

If more that 256 data bytes are sent to the device, the addressing will wrap to the beginning of the same page, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page.

If fewer than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

Chip Select (CS#) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Page Program (PP) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) instruction applied to a page that is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 1) is not executed.

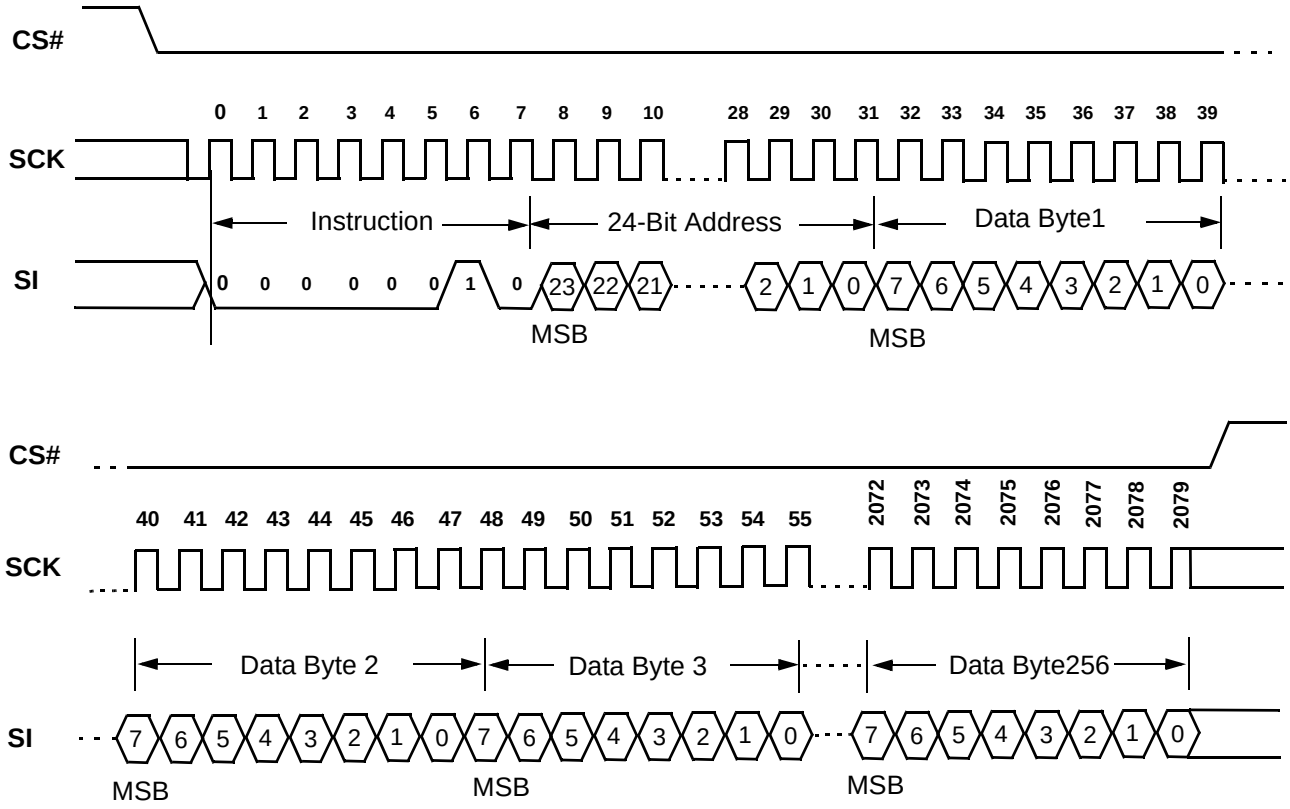


Figure 13. Page Program (PP) Instruction Sequence

Sector Erase (SE)

The Sector Erase (SE) instruction sets to 1 (FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Sector Erase (SE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three address bytes on Serial Data Input (SI). Any address inside the Sector (see Table 1) is a valid address for the Sector Erase (SE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 14.

Chip Select (CS#) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Sector Erase (SE) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Sector Erase (SE) instruction applied to any memory area that is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 1) is not executed.

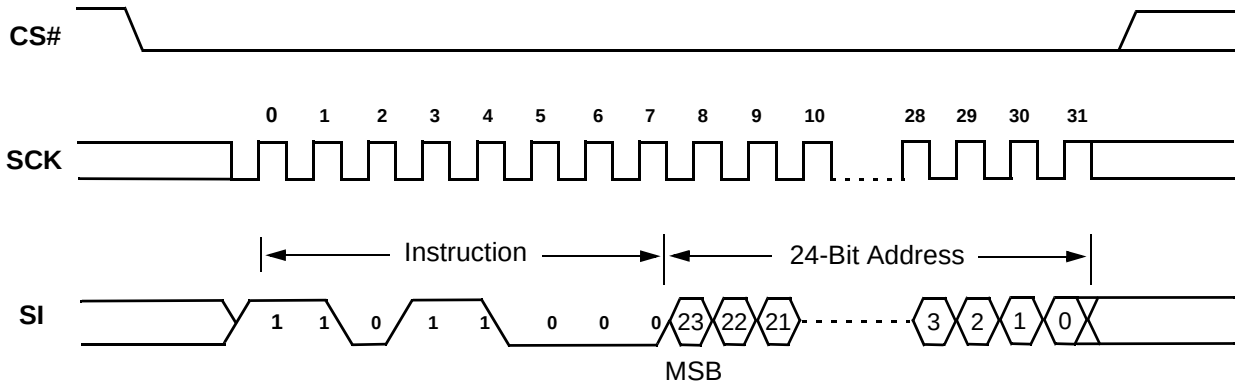


Figure 14. Sector Erase (SE) Instruction Sequence

Bulk Erase (BE)

The Bulk Erase (BE) instruction sets to 1(FFh) all bits inside the entire memory. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Bulk Erase (BE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, Serial Data Input (SI). No address is required for the Bulk Erase (BE). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 15.

As soon as Chip Select (CS#) is driven High, the self-timed Bulk Erase cycle (whose duration is t_{BE}) is initiated. While the Bulk Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Bulk Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Bulk Erase (BE) instruction is executed only if all the Block Protect (BP2, BP1, BP0) bits (see Table 1) are set to 0. The Bulk Erase (BE) instruction is ignored if one or more sectors are protected.

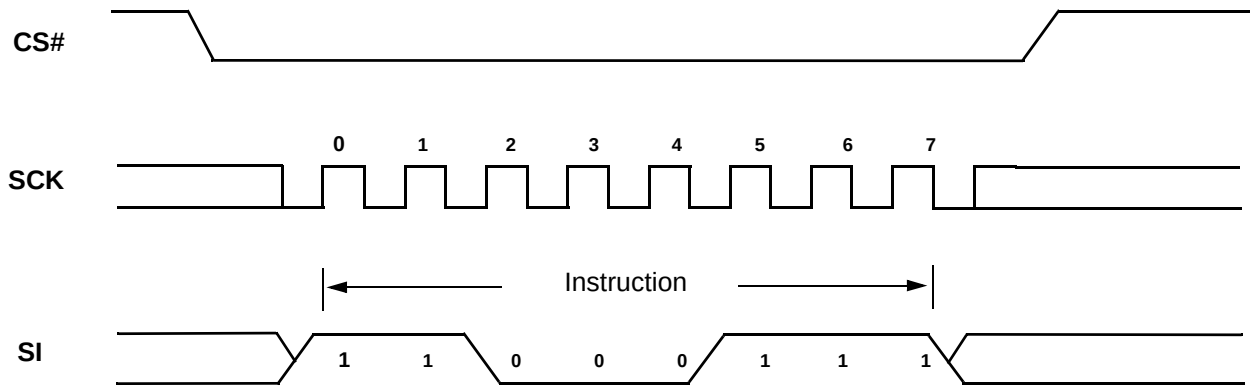


Figure 15. Bulk Erase (BE) Instruction Sequence

Deep Power Down (DP)

The Deep Power Down (DP) instruction puts the device in the lowest current mode of 1uA typical.

It is recommended that the standard Standby mode be used for the lowest power current draw, as well as the Deep Power Down (DP) as an extra software protection mechanism when this device is not in active use. In this mode, the device ignores all Write, Program and Erase instructions. Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The Deep Power Down (DP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (SI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 16.

Driving Chip Select (CS#) High after the eighth bit of the instruction code has been latched puts the device in Deep Power Down mode.

The Deep Power Down mode can only be entered by executing the Deep Power Down (DP) instruction to reduce the standby current (from I_{SB} to I_{DP} as specified in Table 6). As soon as Chip Select (CS#) is driven high, it requires a delay of t_{DP} currently in progress before Deep Power Down mode is entered.

Once the device has entered the Deep Power Down mode, all instructions are ignored except the Release from Deep Power Down (RES) and Read Electronic Signature. This releases the device from the Deep Power Down mode. The Release from Deep Power Down and Read Electronic Signature (RES) instruction also allows the Electronic Signature of the device to be output on Serial Data Output (SO).

The Deep Power Down mode automatically stops at Power-down, and the device always powers up in the Standby mode.

Any Deep Power Down (DP) instruction, while an Erase, Program or WRSR cycle is in progress, is rejected without having any effect on the cycle in progress.

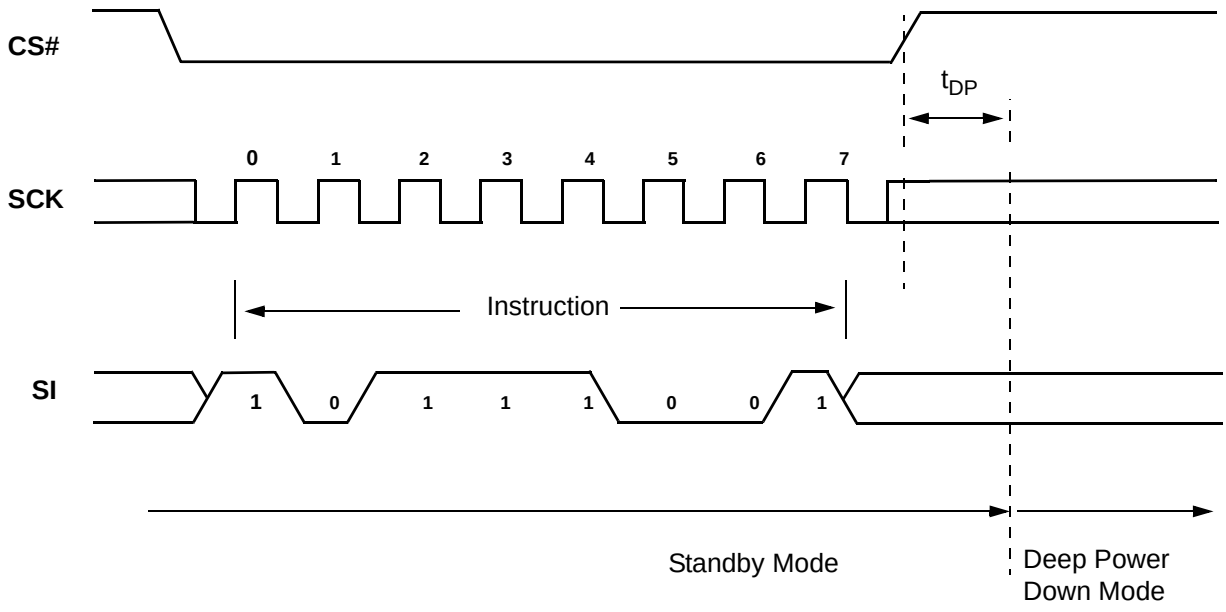


Figure 16. Deep Power Down (DP) Instruction Sequence

Release from Deep Power Down (RES)

The Release from Deep Power Down (RES) instruction provides the only way to exit the Deep Power Down mode. Once the device has entered the Deep Power Down mode, all instructions are ignored except the Release from Deep Power Down (RES) instruction. Executing this instruction takes the device out of Deep Power Down mode.

The Release from Deep Power Down (RES) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (SI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 17.

Driving Chip Select (CS#) High after the 8-bit instruction byte has been received by the device, but before the whole of the 8-bit Electronic Signature has been transmitted for the first time, still insures that the device is put into Standby mode. If the device was previously in the Deep Power Down mode, though, the transition to the Stand-by Power mode is delayed by t_{RES}, and Chip Select (CS#) must remain High for at least $t_{RES(max)}$, as specified in Table 8. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Release from Deep Power Down and Read Electronic Signature (RES)

Once the device has entered Deep Power Down mode, all instructions are ignored except the RES instruction. The RES instruction can also be used to read the old style 8-bit Electronic Signature of the device on the SO pin. The RES instruction always provides access to the Electronic Signature of the device (except while an Erase, Program or WRSR cycle is in progress), and can be applied even if DP mode has not been entered. Any RES instruction executed while an Erase, Program or WRSR cycle is in progress is not decoded, and has no effect on the cycle in progress.

The device features an 8-bit Electronic Signature, whose value for the ES25P80 is 13h. This can be read using RES instruction.

The device is first selected by driving Chip Select (CS#) Low. The instruction code is followed by 3 dummy bytes, each bit being latched-in on Serial Data Input (SI) during the rising edge of Serial Clock (SCK). Then, the 8-bit Electronic Signature, stored in the memory, is shifted out on Serial Data Output (SO), each bit being shifted out during the falling edge of Serial Clock (SCK).

The instruction sequence is shown in Figure 18.

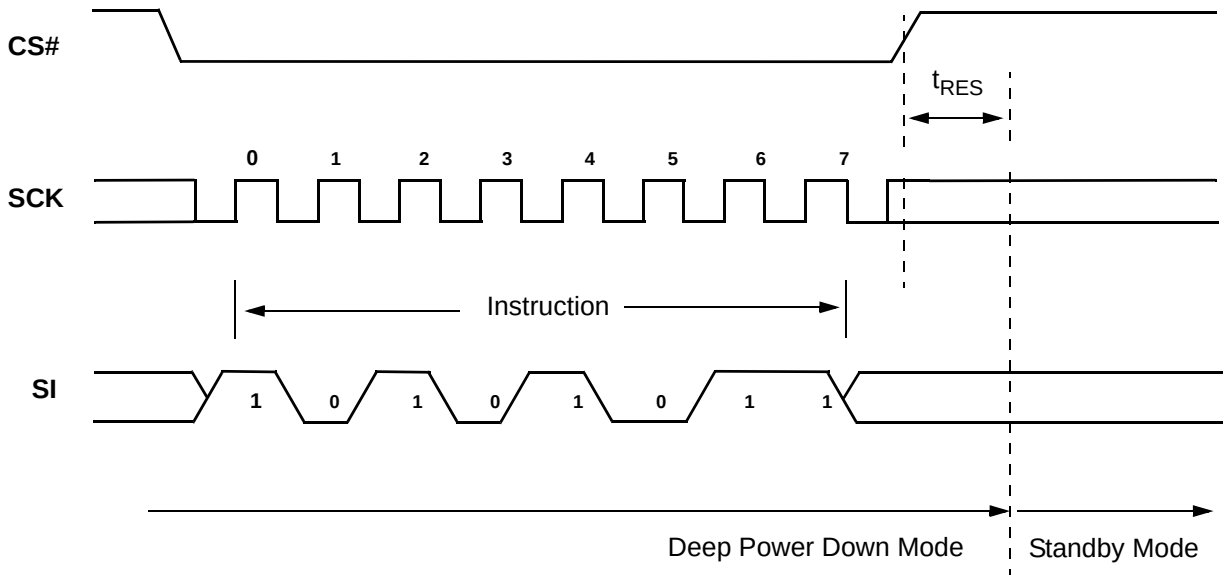


Figure 17. Release from Deep Power Down Instruction Sequence

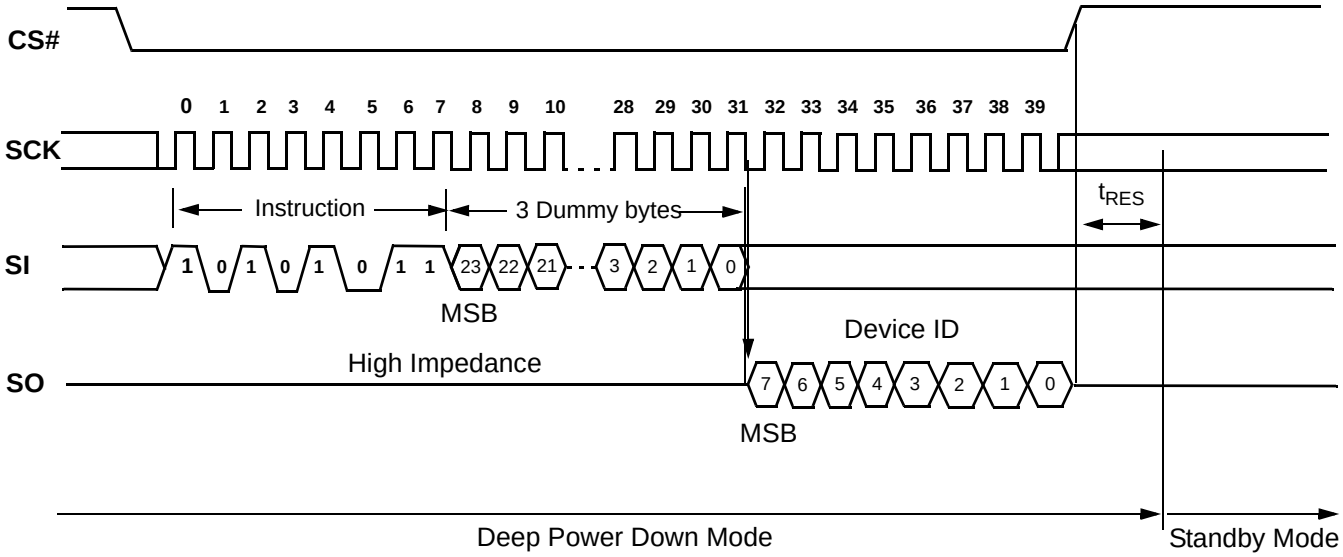


Figure 18. Release from Deep Power Down and Read Electronic Signature (RES) Instruction Sequence

The Release from Deep Power Down and Read Electronic Signature (RES) is terminated by driving Chip Select (CS#) High after the Electronic Signature has been read at least once. Sending additional clock cycles on Serial Clock (SCK), while Chip Select (CS#) is driven Low, causes the Electronic Signature to be output repeatedly.

When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power Down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power Down mode, though, the transition to the Stand-by mode is delayed by t_{RES}, and Chip Select (CS#) must remain High for at least $t_{RES(max)}$, as specified in Table 8. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Read Parameter Page(RDPARA)

The Parameter Page is a 256-byte page of Flash Memory that can be used for storing serial numbers, revision information and configuration data that might typically be stored in an additional memory. Because the Parameter Page is relatively small and separate from the array, the erase time is significantly shorter than that of a sector erase (see t_{PE} in Table.8)

This makes it convenient for more frequent updates.

The Read Parameter Page instruction allows one or more bytes of the Parameter page to be read. The instruction is initiated by driving the CS# low and then shifting the instruction code “53h” followed by a 24-bit address (A23-A0) into the SI pin. Only the lower 8 address bits (A7-A0) are used, the 16 upper most address bis (A23-A8) are ignored. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the SO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. When the end of the Parameter page is reached the address will wrap to the beginning. The Read Parameter Page instruction is shown in Figure 19. The Read Parameter Page (RDPARA) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Parameter Page (RDPARA) instruction, while a Program, Erase, or Write cycle is in progress, is rejected without having any effect on the cycle that is in progress.

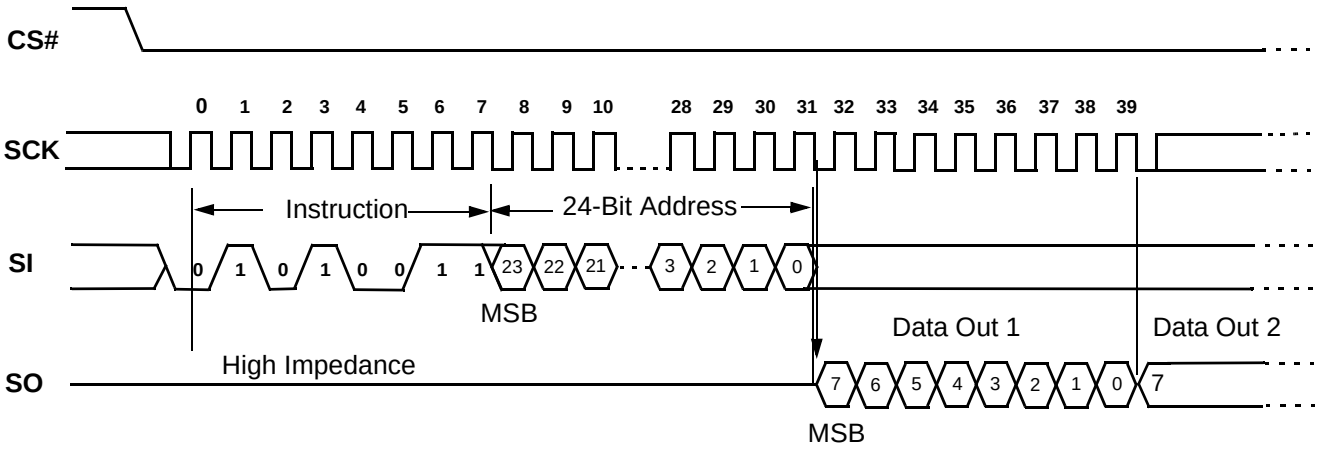


Figure 19. Read Parameter Page (RDPARA) Instruction Sequence

Fast Read Parameter Page(FRDPARA)

The Fast Read Parameter Page instruction is basically the same as the Read Parameter Page instruction except that it allows for a faster clock rate to be used. The Fast Read Parameter Page instruction can opperate at clock frequency D.C. to a maximum of F_{SCK} .

This is accomplished by adding a dummy byte after the 24-bit address, as shown in figure 20. The dummy byte allows the devices internal circuits additional time for setting up the initial address. the dummy byte data value on the SI pin is a don't care.

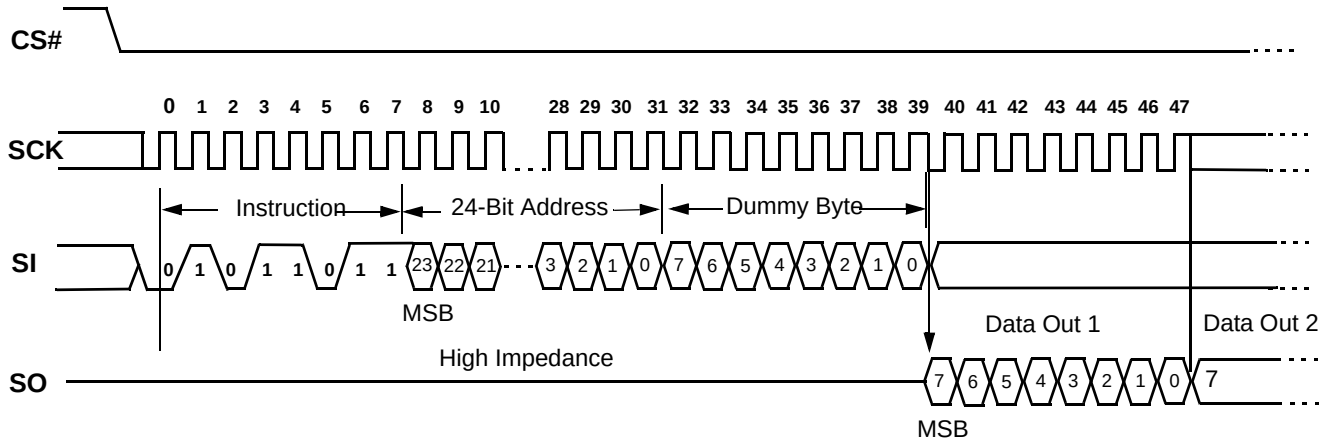


Figure 20. Fast Read Parameter Page (FRDPARA) Instruction Sequence

Program Parameter Page (PPP)

The Program Parameter Page instruction allows up to 256 bytes to be programmed at memory word locations that have been previously erased to all 1s “FFFFh” A Write Enable(WREN) instruction must be executed before the device will accept the Program Parameter Page instruction(Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low then shifting the instruction code “52h” followed by a 24-bit address(A23-A0) and at least one bytes, into the SI pin. Only the lower 8 address bits (A7-A0) are used, the 16 upper most address bit (A23-A8) are ignored. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. The Program Parameter Page instruction sequence is shown in Figure 21.

Less than 256 bytes can be programmed without having any effect on other data within the page. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page. If previously written data bytes are over-written the data will not be valid.

In most application it is best to read the full 256-byte contents of the page into a temporary RAM. Data can then be modified as needed and the entire 256 bytes can then be reprogrammed into the Parameter Page at one time.

As with the write and erase instruction, the CS# must be driven high after the eighth bit of the last byte has been latched. If this is not doen the Parameter Page Program instruction will not be executed. After CS# is driven high, the self timed Page Program instruction will commence for a time duration of t_{PP}, as specified in Table 8. While The Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instruction again. After the program cycle has started the Write Enable Latch(WEL) bit in the Status Register is cleared to 0. The Program Parameter Page instruction will not be excecuted if the addressed page is protected by the Block Protect(BP2, BP1, BP0) bits

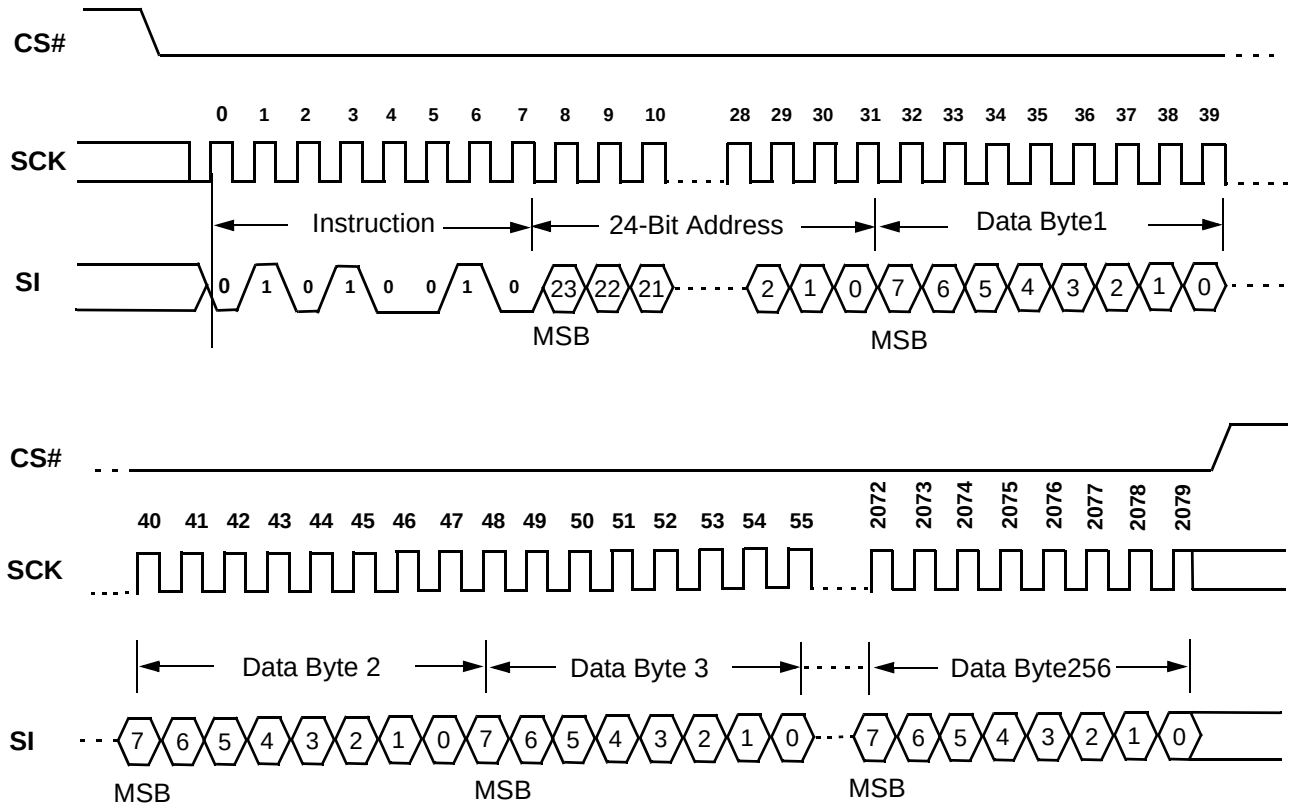


Figure 21. Program Parameter Page (PPP) Instruction Sequence

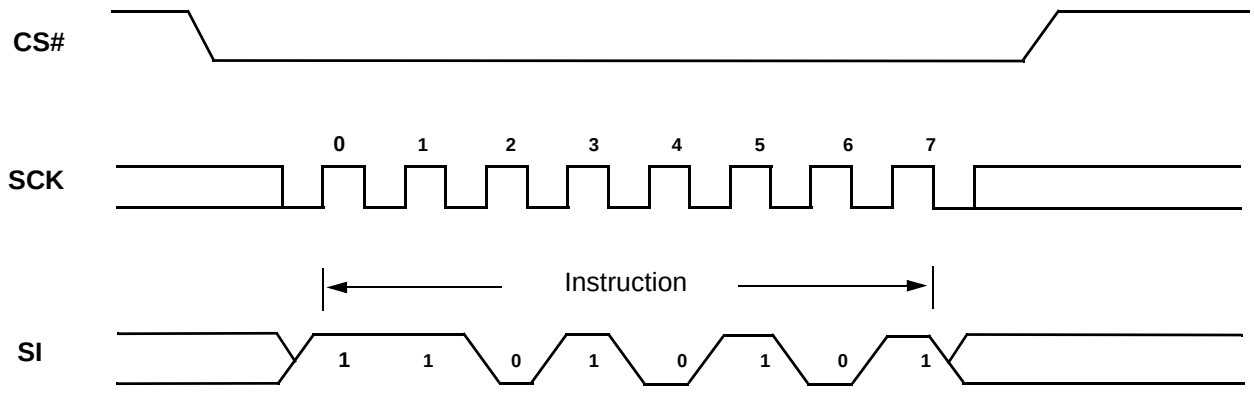


Figure 22. Erase Parameter Page(PE) Instruction Sequence

Erase Parameter Page(PE)

The Erase Parameter Page Instruction sets all 256 bytes of memory in the Parameter Page to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Erase Parameter Page instruction(Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “D5h”. The Erase Parameter Page instruction sequence is shown in Figure 22.

The CS# pin must be driven high after the eighth has been latched. If this is not done the Erase Parameter Page instruction will not be executed. After CS# is driven high, the self-timed Erase Parameter Page instuction will commence for a time duration of t_{PE}.

While the Erase Parameter Page Cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the WIP bit. The WIP bit is a 1 during the Erase Parameter Page cycel and becomes a 0 when finished and the device is ready to accept other instructions again. After the Erase Parameter Page cycle has started the Write Enable Latch(WEL) bit in the Status Register is cleared to 0. The Erase Parameter Page instruction will not be executed if any page is protected by the Block Protect(BP2, BP1, BP0) bits.

Power-up and Power-down

The device must not be selected at power-up or power-down (that is, CS# must follow the voltage applied on Vcc) until Vcc reaches the correct value as follows:

1) Vcc (min) at power-up, and then for a further delay of t_{PU} (as described in Table 5)
2) Vss at power-down

A simple pull-up resistor on Chip Select (CS#) can usually be used to insure safe and proper power-up and power-down.

The device ignores all instructions until a time delay of t_{PU} (as described in Table 5) has elapsed after the moment that Vcc rises above the minimum Vcc threshold. However, correct operation of the device is not guaranteed if by this time Vcc is still below Vcc (min). No Write Status Register, Program or Erase instructions should be sent until t_{PU} after Vcc reaches the minimum Vcc threshold (See Figure 23).

At power-up, the device is in Standby mode (not Deep Power Down mode) and the WEL bit is reset.

Normal precautions must be taken for supply rail decoupling to stabilize the Vcc feed. Each device in a system should have the Vcc rail decoupled by a suitable capacitor close to the package pins (this capacitor is generally of the order of 0.1uF).

At power-down, when Vcc drops from the operating voltage to below the minimum Vcc threshold, all operations are disabled and the device does not respond to any instructions. (The designer needs to be aware that if a power-down occurs while a Write, Program or Erase cycle is in progress, data corruption can result.)

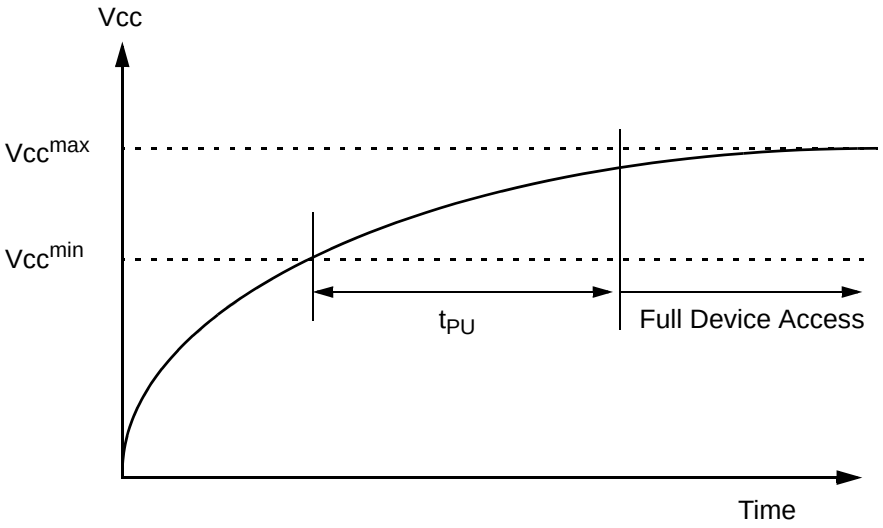


Figure 23. Power-Up Timing

Table 5. Power-Up Timing

Symbol	Parameter	Min.	Max.	Unit
Vcc (min)	Vcc (minimum)	2.7		V
t_{PU}	Vcc (min) to device operation	10		ms

Initial Delivery State

The device is delivered with all bits set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

Maximum Rating

Stressing the device above the rating listed in the Absolute Maximum Ratings section below may cause permanent damage to the device. Theses are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Absolute Maximum Ratings

Ambient Storage Temperature .... -65°C to +150°C

Voltage with Respect to Ground
All inputs and I/Os ..... - 0.3V to 4.5V

Operating Ranges

Ambient Operating Temperature (T_A)

Commercial ..... 0°C to +70°C
Industrial ..... -40°C to +85°C

Positive Power Supply

Voltage Range ..... 2.7V to 3.6V

***Note**:Operating ranges define those limits between which the functionality of the device is guaranteed*

DC CHARACTERISTICS

This section summarizes the DC and AC Characteristics of the device. Designers should check that the operating conditions in their circuit match the measurement conditions specified in the Test Specifications in Table 7, when relying on the quoted parameters.

Table.6 DC Characteristics

Symbol	Description	Test Conditions		Min.	Typ.	Max.	Unit
Vcc	Supply Voltage			2.7	3	3.6	V
I_{LI}	Input Leakage Current	V_{IN} = GND to Vcc				1	uA
I_{SB}	Standby Current	CS# = Vcc				50	uA
I_{DP}	Deep Power Down Current	CS# = Vcc			1	10	uA
I_{LO}	Output Leakage Current	V_{IN} = GND to Vcc				1	uA
I_{CCI}	Active Read Current	SCK = 0.1 Vcc / 0.9 Vcc SO = Open	40MHz			6	mA
		SCK = 0.1Vcc / 0.9 Vcc SO= Open	75 MHz			12	
I_{CC2}	Active Page Program Current	CS# = Vcc				24	mA
I_{CC3}	Active WRSR Current	CS# = Vcc				24	mA
I_{CC4}	Active Sector Erase Current	CS# = Vcc				24	mA
I_{CC5}	Active Bulk Erase Current	CS# = Vcc				24	mA
V_{IL}	Input Low Voltage			- 0.3		0.3 Vcc	V
V_{IH}	Input High Voltage			0.7 Vcc		Vcc + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA, Vcc = Vcc min				0.4	V
V_{OH}	Output High Voltage	I_{OH} = -0.1mA,		Vcc - 0.2			V

Notes:

1. Typical values are at T_A ***= 25°C and Vcc = 3V***

TEST CONDITIONS

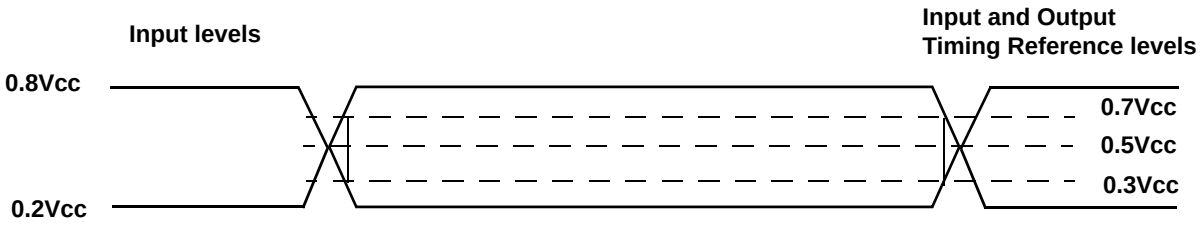


Figure 24. AC Measurements I/O Waveform

Table 7. Test Specifications

Symbol	Parameter	Min	Max	Unit
C_L	Load Capacitance	30		pF
	Input Rise and Fall Times		5	ns
	Input Pulse Voltage	0.2Vcc to 0.8Vcc		V
	Input Timing Reference Voltage	0.3Vcc to 0.7Vcc		V
	Output Timing Reference Voltage	0.5Vcc		V

AC CHARACTERISTICS

Table 8. AC Characteristics

Symbol	Description	Min	Typ	Max	Unit
F_{SCK}	SCK Clock Frequency READ instruction	D.C		40	MHz
F_{SCK}	SCK Clock Frequency for Fast Read and all other instructions except Read instruction	D.C		75	MHz
t_{CRT}	Clock Rise Time (Slew Rate)	0.1			V/ns
t_{CFT}	Clock Fall Time (Slew Rate)	0.1			V/ns
t_{WH}	SCK High Time	6			ns
t_{WL}	SCK Low Time	6			ns
t_{CS}	CS# High Time	100			ns
t_{CSS} (Note 3)	CS# Setup Time	5			ns
t_{CSH} (Note 3)	CS# Hold Time	5			ns
t_{HD} (Note 3)	HOLD# Setup Time (relative to SCK)	5			ns
t_{CD} (Note 3)	HOLD# Hold Time (relative to SCK)	5			ns
t_{HC}	HOLD# Setup Time (relative to SCK)	5			ns
t_{CH}	HOLD# Hold Time (relative to SCK)	5			ns
t_{V}	Output Valid			6	ns
t_{HO}	Output Hold Time	0			ns
$t_{HD:DAT}$	Data in Hold Time	3			ns
$t_{SU:DAT}$	Data in Setup Time	3			ns
t_{R}	Input Rise Time			5	ns
t_{F}	Input Fall Time			5	ns
t_{LZ} (Note 3)	HOLD# to Output Low Z			6	ns
t_{HZ} (Note 3)	HOLD# to Output High Z			6	ns
t_{DIS} (Note 3)	Output Disable Time			8	ns
t_{WPS} (Note 3)	Write Protect Setup Time	15			ns
t_{WPH} (Note 3)	Write Protect Hold Time	15			ns
t_{RES}	Release DP Mode			3	us
t_{DP}	CS# High to Deep Power Down Mode			3	us
t_{W}	Write Status Register Time			5	ms
t_{PP}	Page Programming Time		1.5 (Note 1)	3 (Note 2)	ms
t_{SE}	Sector Erase Time		0.5 (Note 1)	3 (Note 2)	sec
t_{BE}	Bulk Erase Time		6 (Note 1)	12 (Note 2)	sec
t_{PE}	Parameter Page Erase Time		20 (Note 1)	100 (Note 2)	ms

Notes:

1. Typical program and erase times assume the following conditions : 25'C, Vcc = 3.0V ; 10,000 cycles ; checkerboard data pattern

2. Under worst-case conditions of 90'C ; Vcc = 2.7V ; 100,000 cycles.

3. Not 100% tested.

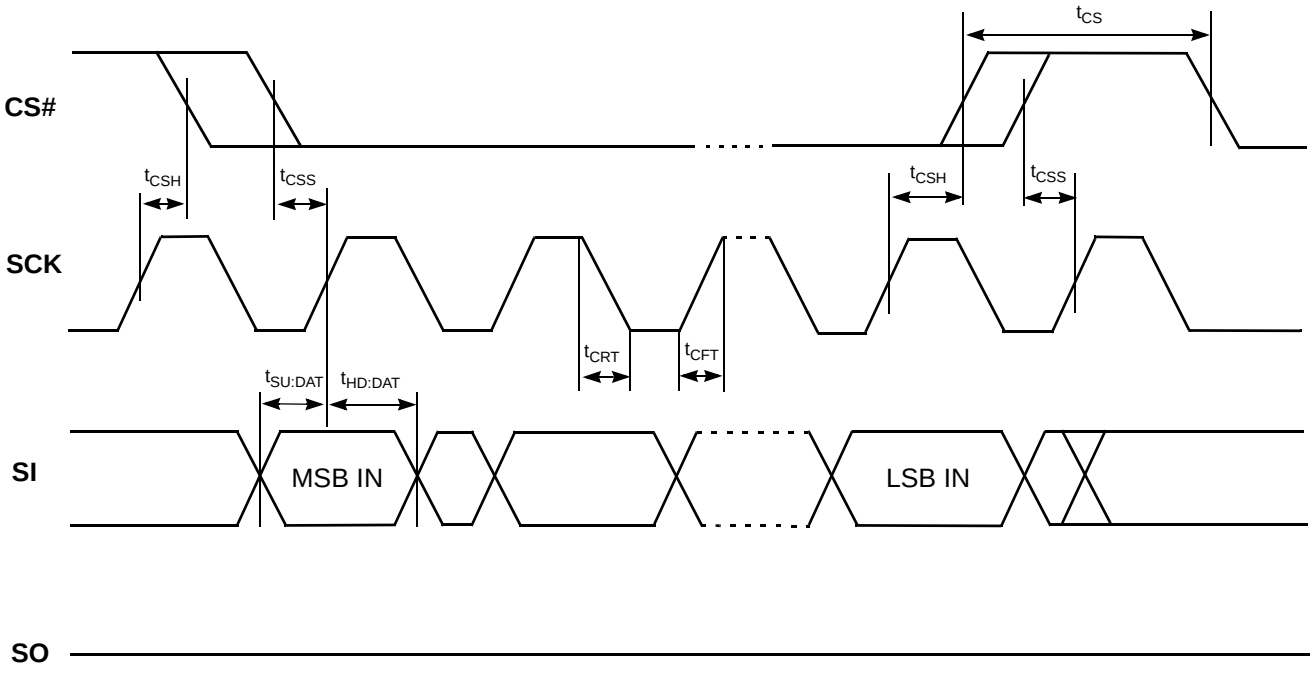


Figure 25. SPI Mode 0 (0,0) Input Timing

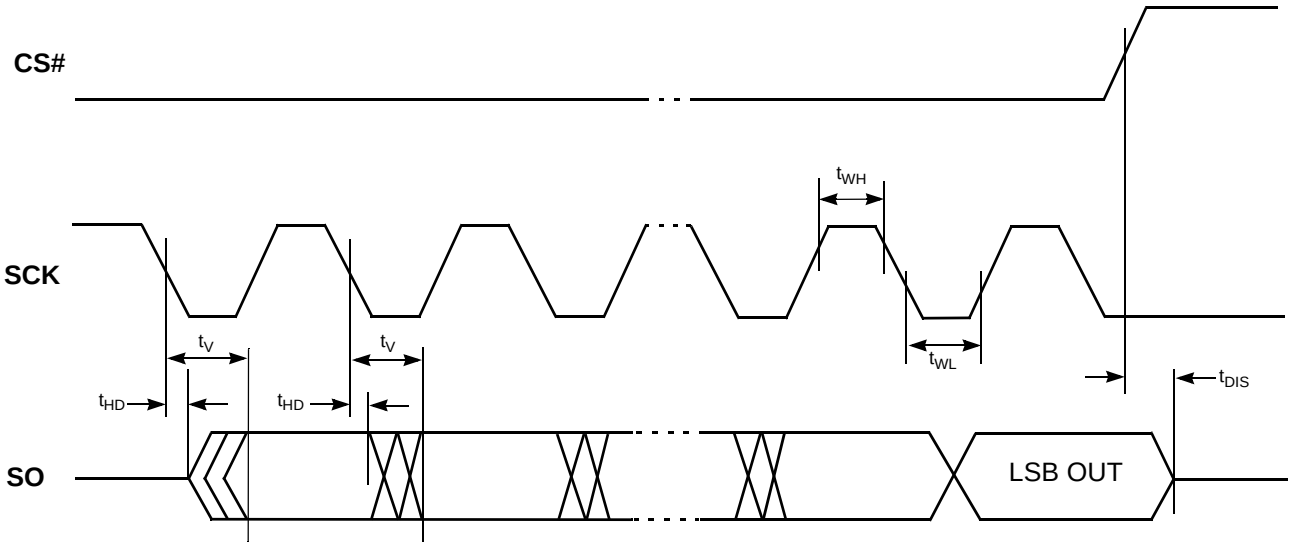


Figure 26. SPI Mode 0 (0,0) Output Timing

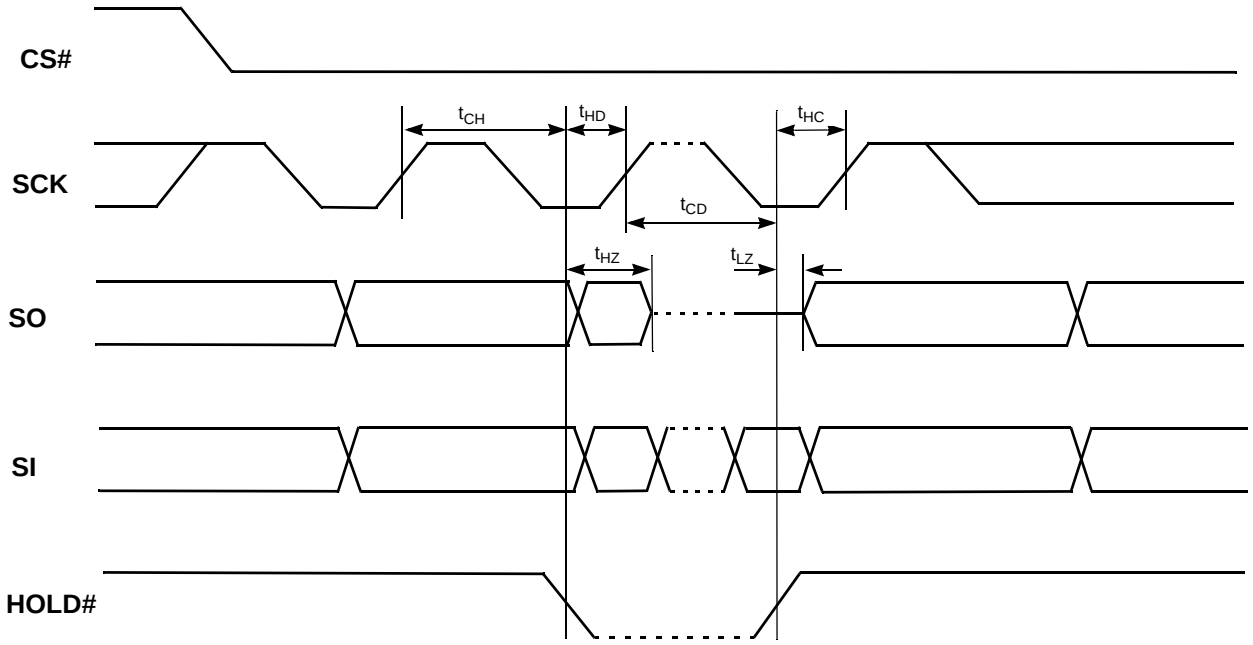


Figure 27. HOLD# Timing

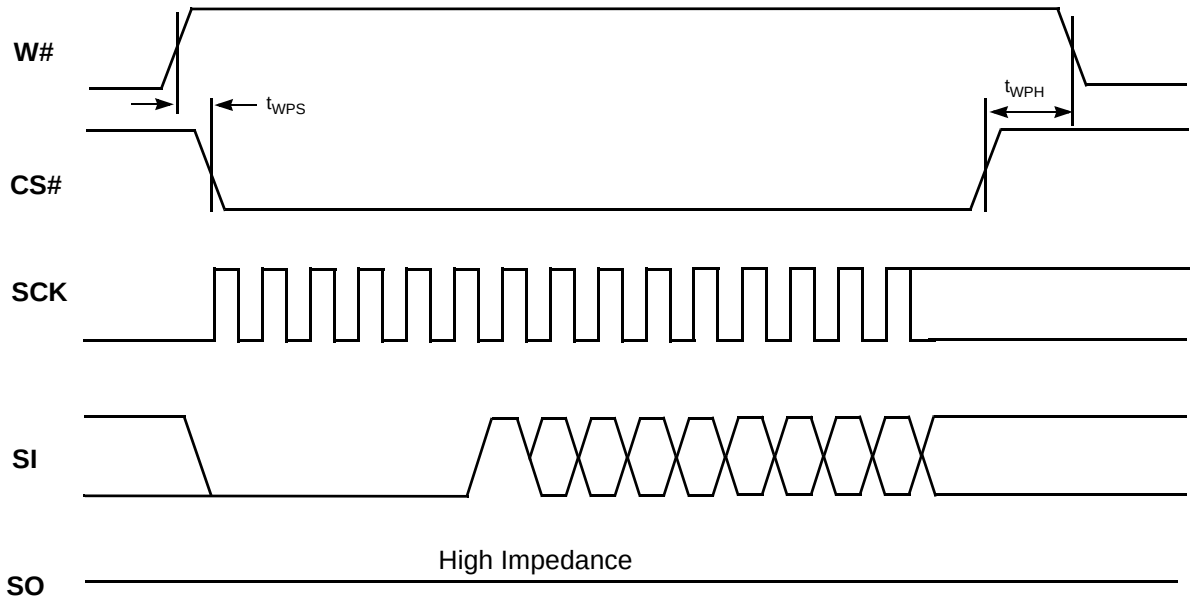
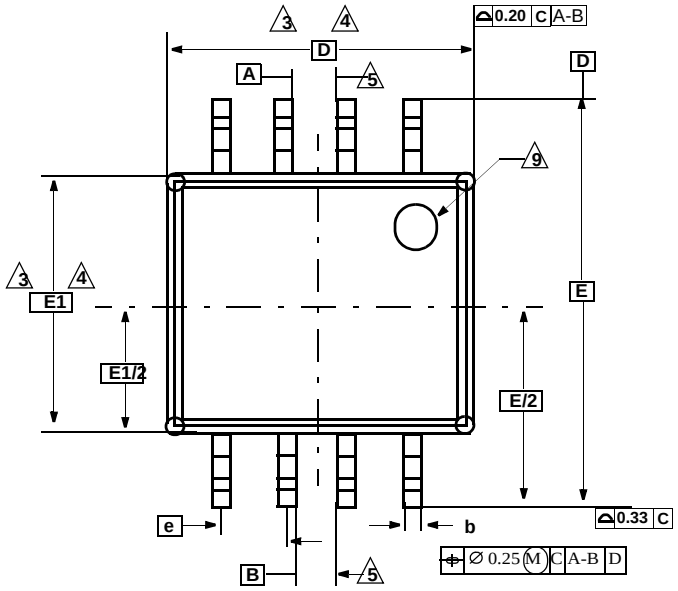
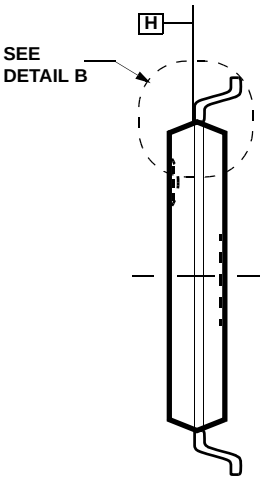
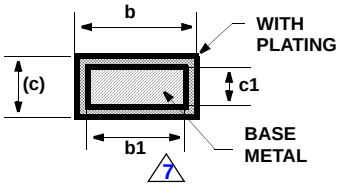


Figure 28. Write Protect Setup and Hold Timing during WRSR when SRWD = 1

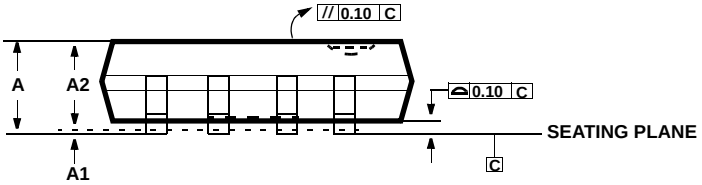
PHYSICAL DIMENSIONS
S08 wide - 8 pin Plastic Small Outline 208 mils Body Width Package

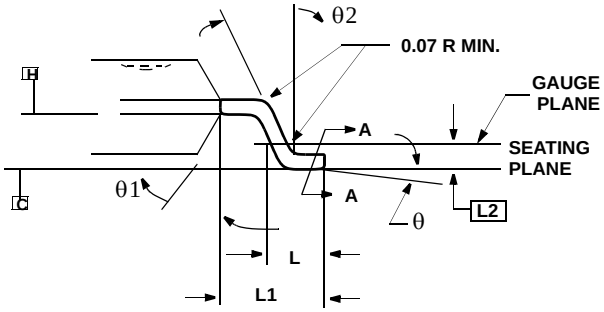






SECTION A-A





DETAIL B

Package	SOC 008 (inches)		SOC 008 (mm)	
JEDEC				
Symbol	MIN	MAX	MIN	MAX
A	0.069	0.085	1.753	2.159
A1	0.002	0.0098	0.051	0.249
A2	0.067	0.075	1.70	1.91
b	0.014	0.018	0.356	0.483
b1	0.013	0.018	0.330	0.457
c	0.0075	0.0095	0.191	0.241
c1	0.006	0.008	0.152	0.203
D	0.208 BSC		5.283 BSC	
E	0.315 BSC		8.001 BSC	
E1	0.208 BSC		5283 BSC	
e	0.050 BSC		1.27 BSC	
L	0.020	0.030	0.508	0.762
L1	0.055 REF		1.40 REF	
L2	0.010 BSC		0.25 BSC	
N	8		8	
θ	0’	8’	0’	8’
θ1	5’	15’	5’	15’
θ2	0’		0’	

NOTES:

1. *All dimensions are in both inches and millimeters.*
2. *Dimensioning and tolerancing per ASME Y 14.5M - 1994.*
3. *Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion interlead flash or protrusion shall not exceed 0.25mm per side. D and E1 dimensions are determined at datum H.*
4. *The package top may be smaller than the package bottom. Dime--nsions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash. But including any mismatch between the top and bottom of the plastic body.*
5. *Datums A and B to be determined at datum H.*
6. *“N” is the maximum number of terminal positions for the specified package length H.*
7. *The dimensions apply to the flat section of the lead between 0.10 to 0.25 mm from the lead tip.*
8. *Dimension “b” does not include dambar protrusion. Allowable dam-bar protrusion shall be 0.10 mm total in excess of the “b” dimension at maximum material condition. The dambar cannot not be located on the lower radius of the lead foot.*
9. *This chamfer feature is optional. If it is not present, then a pin 1 idenfifier must be located within the index area indicated.*
10. *Lead coplanarity shall be within 0.10 mm. As measured from the seating plane.*

ORDERNG INFORMATION

Standard Products

ESI standard products are available in several package and operating ranges. The order number (Valid Combination) is formed by a combination of the following:

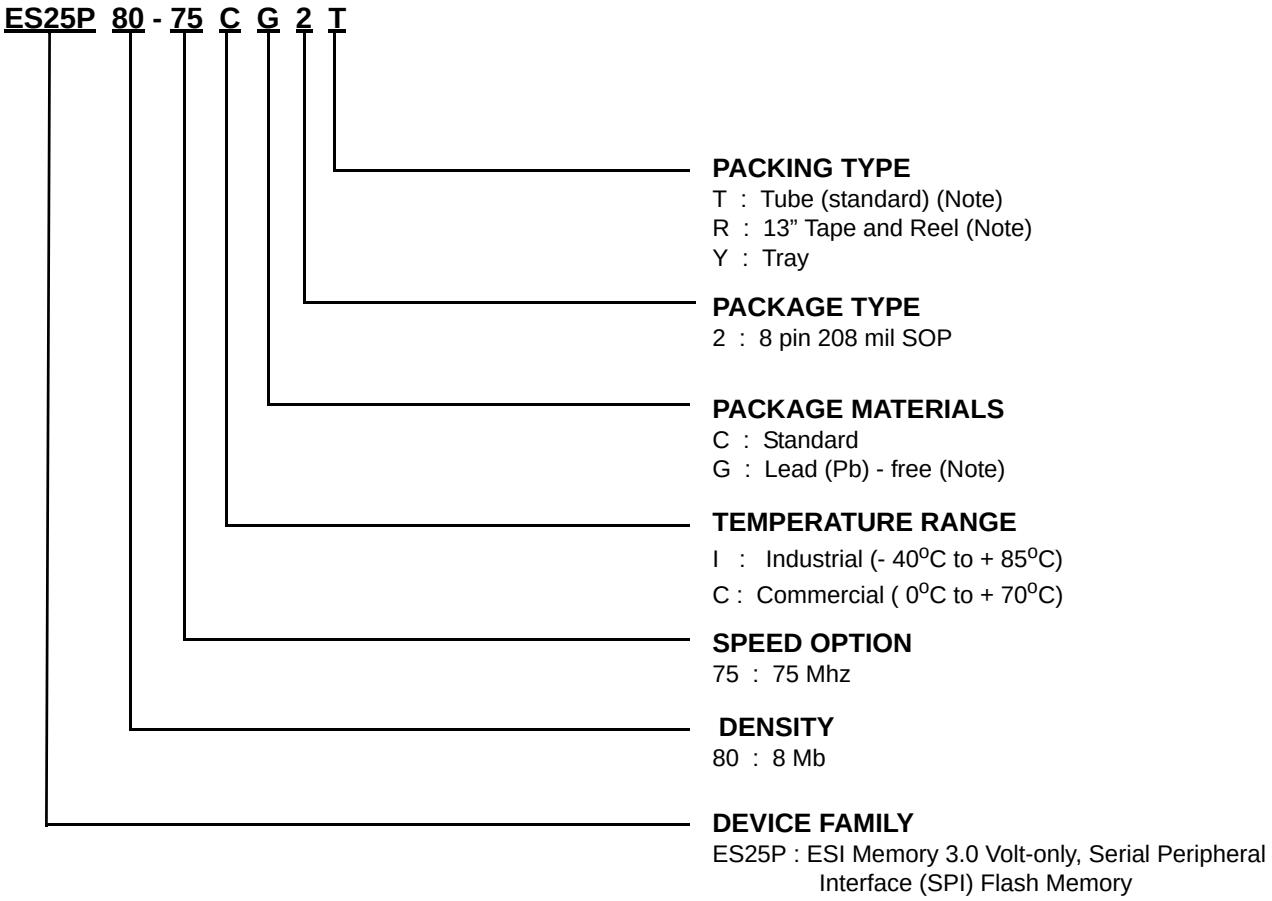


Table 1. ES25P Valid Combinations

ES25P Valid Combinations					
Base Ordering Part Number	Speed Option	Temperature & Package Material	Package Type	Packing Type	Package Marking
ES25P80	75	CG, CC, IG,IC (Note)	2, 7	T, R,Y (Note)	P80 + (Speed) + (Temp) + (Package Material)

Notes:

Contact your local sales office for availability.

Document Title

8M Serial FlashMemory

Revision History

Revision Number	Data	Items
Rev. 0A	JAN. 03,2006	Initial Release Version.
Rev.0B	MAR.14,2006	Device Name changed
Rev.0C	May. 01, 2006	The Clock Frequency was changed from 66MHz to 75MHz.
Rev.0D	May.11, 2006	WSON package not supported

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