18Mb 1x1Dp LVCMOS High Speed Synchronous SRAMs (256Kb x 72 or 512Kb x 36 or 1Mb x 18) **Preliminary**

Description

The CXK79M72C165GB (organized as 262,144 words by 72 bits), CXK79M36C165GB (organized as 524,288 words by 36 bits), and the CXK79M18C165GB (organized as 1,048,576 words by 18 bits) are high speed CMOS synchronous static RAMs with common I/O pins. They are manufactured in compliance with the JEDEC-standard 209 pin BGA package pinouts defined for SigmaRAMs. They integrate input registers, high speed RAM, output registers, and a two-deep write buffer onto a single monolithic IC. Single Data Rate (SDR) Pipelined (PL) read operations and Double Late Write (DLW) write operations are supported, providing a high-performance user interface. Positive and negative output clocks are provided for applications requiring source-synchronous operation.

All address and control input signals are registered on the rising edge of the CK input clock.

During read operations, output data is driven valid once, from the rising edge of CK, one full cycle after the address and control signals are registered.

During write operations, input data is registered once, on the rising edge of CK, two full cycles after the address and control signals are registered.

Output drivers are series-terminated, and output impedance is selectable via the ZQ control pin. When ZQ is tied “low”, the impedance of the SRAM’s output drivers is set to ~25Ω. When ZQ is tied “high” or left unconnected, the impedance of the SRAM’s output drivers is set to ~50Ω.

300 MHz operation (300 Mbps) is obtained from a single 1.8V power supply. JTAG boundary scan interface is provided using a subset of IEEE standard 1149.1 protocol.

Features

- 3 Speed Bins

3 Speed Bins	Cycle Time / Data Access Time
-33	3.3ns / 1.8ns
-4	4.0ns / 2.1ns
-5	5.0ns / 2.3ns

- Single 1.8V power supply (V_{DD}): 1.7V (min) to 1.95V (max)
- Dedicated output supply voltage (V_{DDQ}): 1.4V (min) to V_{DD} (max)
- LVCMOS-compatible I/O interface
- Common I/O
- Single Data Rate (SDR) data transfers
- Pipelined (PL) read operations
- Double Late Write (DLW) write operations
- Burst capability with internally controlled Linear Burst address sequencing
- Burst length of two, three, or four, with automatic address wrap
- Full read/write data coherency
- Byte write capability
- Single-ended input clock (CK)
- Data-referenced output clocks (CQ1, $\overline{CQ1}$, CQ2, $\overline{CQ2}$)
- Selectable output driver impedance via dedicated control pin (ZQ)
- Depth expansion capability (2 or 4 banks) via programmable chip enables (E2, E3, EP2, EP3)
- JTAG boundary scan (subset of IEEE standard 1149.1)
- 209 pin (11x19), 1mm pitch, 14mm x 22mm Ball Grid Array (BGA) package

256Kb x 72 Pin Assignment (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	DQg	DQg	A	E2	A	ADV	A	E3	A	DQb	DQb
B	DQg	DQg	$\overline{Bc}$	$\overline{Bg}$	NC (x36)	$\overline{W}$	A	$\overline{Bb}$	$\overline{Bf}$	DQb	DQb
C	DQg	DQg	$\overline{Bh}$	$\overline{Bd}$	NC (144M)	$\overline{E1}$	NC (x18)	$\overline{Be}$	$\overline{Ba}$	DQb	DQb
D	DQg	DQg	V_{SS}	NC	NC	MCL	NC	NC	V_{SS}	DQb	DQb
E	DQg	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQf	DQb
F	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	ZQ	V_{SS}	V_{SS}	V_{SS}	DQf	DQf
G	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	EP2	V_{DD}	V_{DDQ}	V_{DDQ}	DQf	DQf
H	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	EP3	V_{SS}	V_{SS}	V_{SS}	DQf	DQf
J	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	DQf	DQf
K	CQ2	$\overline{CQ2}$	CK	NC	V_{SS}	MCL	V_{SS}	NC	NC	$\overline{CQ1}$	CQ1
L	DQh	DQh	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
M	DQh	DQh	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
N	DQh	DQh	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
P	DQh	DQh	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
R	DQd	DQh	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQe
T	DQd	DQd	V_{SS}	NC	NC	MCL	NC	NC	V_{SS}	DQe	DQe
U	DQd	DQd	NC	A	NC (72M)	A	NC (36M)	A	NC	DQe	DQe
V	DQd	DQd	A	A	A	A1	A	A	A	DQe	DQe
W	DQd	DQd	TMS	TDI	A	A0	A	TDO	TCK	DQe	DQe

512Kb x 36 Pin Assignment (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	A	E2	A	ADV	A	E3	A	DQb	DQb
B	NC	NC	$\overline{Bc}$	NC	A (x36)	$\overline{W}$	A	$\overline{Bb}$	NC	DQb	DQb
C	NC	NC	NC	$\overline{Bd}$	NC (144M)	$\overline{E1}$	NC (x18)	NC	$\overline{Ba}$	DQb	DQb
D	NC	NC	V_{SS}	NC	NC	MCL	NC	NC	V_{SS}	DQb	DQb
E	NC	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	NC	DQb
F	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	ZQ	V_{SS}	V_{SS}	V_{SS}	NC	NC
G	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	EP2	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
H	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	EP3	V_{SS}	V_{SS}	V_{SS}	NC	NC
J	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
K	CQ2	$\overline{CQ2}$	CK	NC	V_{SS}	MCL	V_{SS}	NC	NC	$\overline{CQ1}$	CQ1
L	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
M	NC	NC	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
N	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
P	NC	NC	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
R	DQd	NC	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	NC
T	DQd	DQd	V_{SS}	NC	NC	MCL	NC	NC	V_{SS}	NC	NC
U	DQd	DQd	NC	A	NC (72M)	A	NC (36M)	A	NC	NC	NC
V	DQd	DQd	A	A	A	A1	A	A	A	NC	NC
W	DQd	DQd	TMS	TDI	A	A0	A	TDO	TCK	NC	NC

1Mb x 18 Pin Assignment (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	A	E2	A	ADV	A	E3	A	NC	NC
B	NC	NC	$\overline{Bb}$	NC	A (x36)	$\overline{W}$	A	NC	NC	NC	NC
C	NC	NC	NC	NC	NC (144M)	$\overline{E1}$	A (x18)	NC	$\overline{Ba}$	NC	NC
D	NC	NC	V_{SS}	NC	NC	MCL	NC	NC	V_{SS}	NC	NC
E	NC	DQb	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
F	DQb	DQb	V_{SS}	V_{SS}	V_{SS}	ZQ	V_{SS}	V_{SS}	V_{SS}	NC	NC
G	DQb	DQb	V_{DDQ}	V_{DDQ}	V_{DD}	EP2	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
H	DQb	DQb	V_{SS}	V_{SS}	V_{SS}	EP3	V_{SS}	V_{SS}	V_{SS}	NC	NC
J	DQb	DQb	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC
K	CQ2	$\overline{CQ2}$	CK	NC	V_{SS}	MCL	V_{SS}	NC	NC	$\overline{CQ1}$	CQ1
L	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
M	NC	NC	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
N	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
P	NC	NC	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
R	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	NC
T	NC	NC	V_{SS}	NC	NC	MCL	NC	NC	V_{SS}	NC	NC
U	NC	NC	NC	A	NC (72M)	A	NC (36M)	A	NC	NC	NC
V	NC	NC	A	A	A	A1	A	A	A	NC	NC
W	NC	NC	TMS	TDI	A	A0	A	TDO	TCK	NC	NC

Pin Description

Symbol	Type	Quantity	Description
A	Input	x72 = 16 x36 = 17 x18 = 18	Address Inputs - Registered on the rising edge of CK.
A1, A0	Input	2	Address Inputs 1,0 - Registered on the rising edge of CK. Initialize burst counter.
DQa, DQb DQc, DQd DQe, DQf DQg, DQh	I/O	x72 = 72 x36 = 36 x18 = 18	Data Inputs / Outputs - Registered on the rising edge of CK during write operations. Driven from the rising edge of CK during read operations. DQa - indicates Data Byte a DQb - indicates Data Byte b DQc - indicates Data Byte c DQd - indicates Data Byte d DQe - indicates Data Byte e DQf - indicates Data Byte f DQg - indicates Data Byte g DQh - indicates Data Byte h
CK	Input	1	Input Clock
CQ1, $\overline{\text{CQ1}}$ CQ2, $\overline{\text{CQ2}}$	Output	4	Output Clocks
$\overline{\text{E1}}$	Input	1	Chip Enable Control Input - Registered on the rising edge of CK. $\overline{\text{E1}}$ = 0 enables the device to accept read and write commands. $\overline{\text{E1}}$ = 1 disables the device. See the Clock Truth Table section for further information.
E2, E3	Input	2	Programmable Chip Enable Control Inputs - Registered on the rising edge of CK. See the Clock Truth Table and Depth Expansion sections for further information.
EP2, EP3	Input	2	Programmable Chip Enable Active-Level Select Inputs - These pins must be tied “high” or “low” at power-up. See the Clock Truth Table and Depth Expansion sections for further information.
ADV	Input	1	Address Advance Control Input - Registered on the rising edge of CK. ADV = 0 loads a new address and begins a new operation when the device is enabled. ADV = 1 increments the address and continues the previous operation when the device is enabled. See the Clock Truth Table section for further information.
$\overline{\text{W}}$	Input	1	Write Enable Control Input - Registered on the rising edge of CK. $\overline{\text{W}}$ = 0 specifies a write operation when ADV = 0 and the device is enabled. $\overline{\text{W}}$ = 1 specifies a read operation when ADV = 0 and the device is enabled. See the Clock Truth Table section for further information.
$\overline{\text{Ba}}$, $\overline{\text{Bb}}$, $\overline{\text{Bc}}$ $\overline{\text{Bd}}$, $\overline{\text{Be}}$, $\overline{\text{Bf}}$ $\overline{\text{Bg}}$, $\overline{\text{Bh}}$	Input	x72 = 8 x36 = 4 x18 = 2	Byte Write Enable Control Inputs - Registered on the rising edge of CK. $\overline{\text{Ba}}$ = 0 specifies write Data Byte a during a write operation $\overline{\text{Bb}}$ = 0 specifies write Data Byte b during a write operation $\overline{\text{Bc}}$ = 0 specifies write Data Byte c during a write operation $\overline{\text{Bd}}$ = 0 specifies write Data Byte d during a write operation $\overline{\text{Be}}$ = 0 specifies write Data Byte e during a write operation $\overline{\text{Bf}}$ = 0 specifies write Data Byte f during a write operation $\overline{\text{Bg}}$ = 0 specifies write Data Byte g during a write operation $\overline{\text{Bh}}$ = 0 specifies write Data Byte h during a write operation See the Clock Truth Table section for further information.
ZQ	Input	1	Output Impedance Control Input - This pin must be tied “high” or “low” at power-up. ZQ = 0 selects ~25Ω output impedance ZQ = 1 selects ~50Ω output impedance Note: This pin can also be left unconnected. It is weakly pulled “high” internally.

Symbol	Type	Quantity	Description
V_{DD}		14	1.8V Core Power Supply - Core supply voltage.
V_{DDQ}		24	Output Power Supply - Output buffer supply voltage.
V_{SS}		30	Ground
TCK	Input	1	JTAG Clock
TMS	Input	1	JTAG Mode Select - Weakly pulled “high” internally.
TDI	Input	1	JTAG Data In - Weakly pulled “high” internally.
TDO	Output	1	JTAG Data Out
MCL	*Input*	5	Must Connect “Low” - May not be actual input pins.
MCH	*Input*	3	Must Connect “High” - May not be actual input pins.
NC		x72 = 18 x36 = 57 x18 = 76	No Connect - These pins are true no-connects, i.e. there is no internal chip connection to these pins. They can be left unconnected or tied directly to V_{DD}, V_{DDQ}, or V_{SS}.

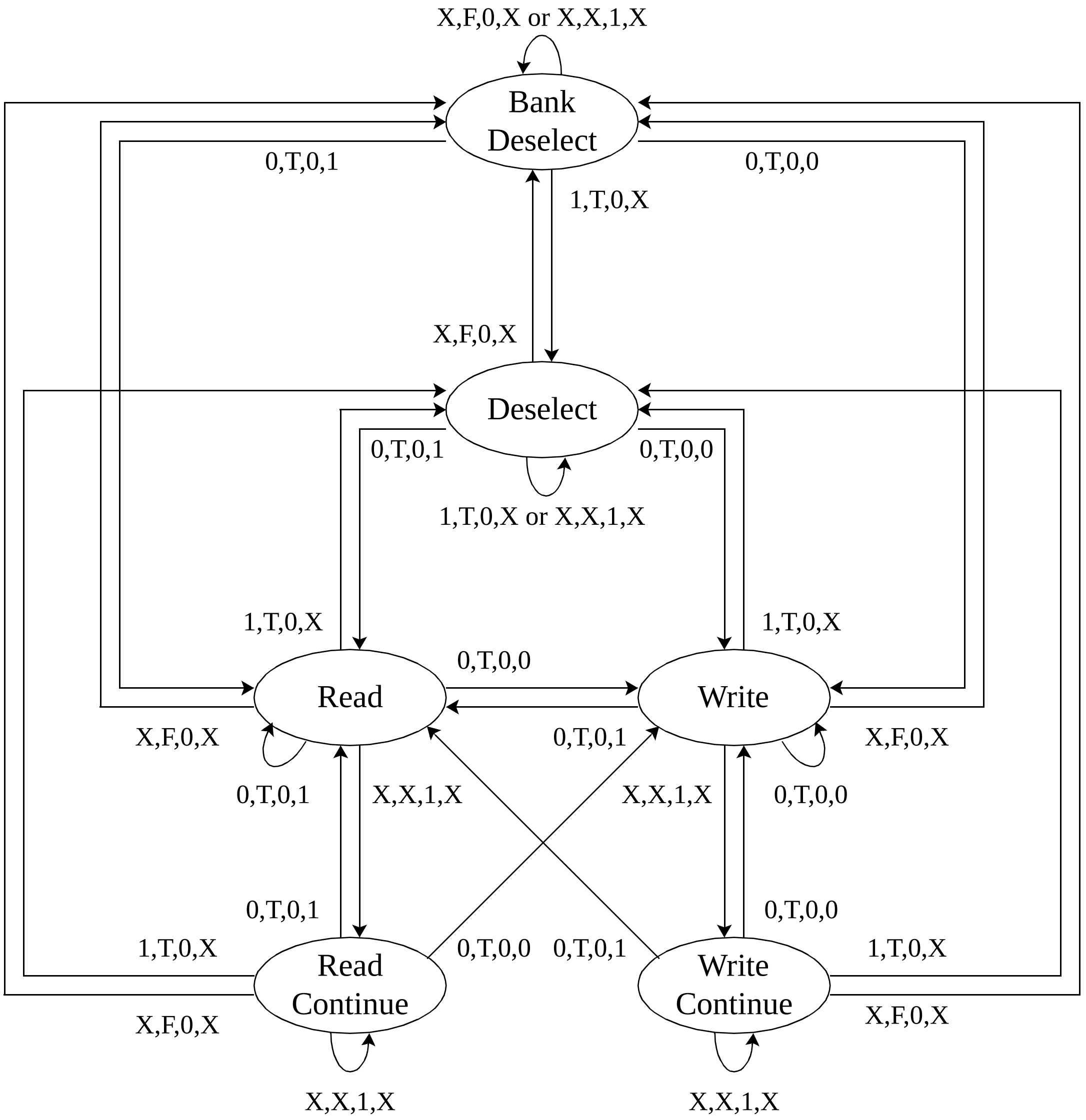
Clock Truth Table

CK	$\overline{\text{E1}}$ (t_n)	E (t_n)	ADV (t_n)	$\overline{\text{W}}$ (t_n)	B (t_n)	Previous Operation	Current Operation	DQ/CQ (t_n)	DQ/CQ (t_{n+1})	DQ/CQ (t_{n+2})
↑	X	F	0	X	X	X	Bank Deselect	***	Hi-Z	---
↑	X	X	1	X	X	Bank Deselect	Bank Deselect (Continue)	Hi-Z	Hi-Z	---
↑	1	T	0	X	X	X	Deselect	***	Hi-Z/CQ	---
↑	X	X	1	X	X	Deselect	Deselect (Continue)	Hi-Z/CQ	Hi-Z/CQ	---
↑	0	T	0	0	T	X	Write Loads new address Stores DQx if $\overline{\text{Bx}}$ = 0	***	Hi-Z/CQ	D1/---
↑	0	T	0	0	F	X	Write (Abort) Loads new address No data stored	***	Hi-Z/CQ	X/---
↑	X	X	1	X	T	Write	Write Continue Increments address by 1 Stores DQx if $\overline{\text{Bx}}$ = 0	Hi-Z/CQ	D1/CQ	D2/---
↑	X	X	1	X	F	Write	Write Continue (Abort) Increments address by 1 No data stored	Hi-Z/CQ	D1/CQ	X/---
↑	0	T	0	1	X	X	Read Loads new address	***	Q1/CQ	---
↑	X	X	1	X	X	Read	Read Continue Increments address by 1	Q1/CQ	Q2/CQ	---

Notes:

1. “1” = input “high”; “0” = input “low”; “X” = input “don’t care”; “T” = input “true”; “F” = input “false”.
2. “***” indicates that the DQ input requirement or output state and the CQ output state are determined by the previous operation.
3. “---” indicates that the DQ input requirement or output state and the CQ output state are determined by the next operation.
4. If E2 = EP2 and E3 = EP3 then E = “T” else E = “F”.
5. If one or more $\overline{\text{Bx}}$ = 0 then B = “T” else B = “F”.
6. DQs are tri-stated in response to Bank Deselect, Deselect, and Write commands, one full cycle after the command is sampled.
7. CQs are tri-stated in response to Bank Deselect commands only, one full cycle after the command is sampled.
8. Up to three (3) Continue operations may be initiated after a Read or Write operation is initiated to burst transfer up to four (4) distinct pieces of data per single external address input. If a fourth (4th) Continue operation is initiated, the internal address wraps back to the initial external (base) address.

State Diagram



Notes:

1. The notation “X,X,X,X” controlling the state transitions above indicate the states of inputs $\overline{\mathrm{E1}}$, E, ADV, and $\overline{\mathrm{W}}$ respectively.
2. “1” = input “high”; “0” = input “low”; “X” = input “don’t care”; “T” = input “true”; “F” = input “false”.
3. If E2 = EP2 and E3 = EP3 then E = “T” else E = “F”.

•Burst (Continue) Operations

Burst operations follow the **Linear Burst** address sequence depicted in the table below:

	A(1:0)				Sequence Key
1st (Base) Address	00	01	10	11	A1, A0
2nd Address	01	10	11	00	(A1 xor A0), $\overline{A0}$
3rd Address	10	11	00	01	$\overline{A1}$, A0
4th Address	11	00	01	10	$\overline{(A1 \text{ xor } A0)}$, $\overline{A0}$

Up to three (3) Continue operations may be initiated after a Read or Write operation is initiated to burst transfer up to four (4) distinct pieces of data per single external address input. If a fourth (4th) Continue operation is initiated, the internal address wraps back to the initial external (base) address.

•Depth Expansion

Depth expansion in these devices is supported via programmable chip enables E2 and E3. The active levels of E2 and E3 are programmable through the static inputs EP2 and EP3 respectively. When EP2 is tied “high”, E2 functions as an active-high input. When EP2 is tied “low”, E2 functions as an active-low input. Similarly, when EP3 is tied “high”, E3 functions as an active-high input. And, when EP3 is tied “low”, E3 functions as an active-low input.

The programmability of E2 and E3 allows four banks of depth expansion to be accomplished with no additional logic. By programming E2 and E3 of four devices in a binary sequence (00, 01, 10, 11), and by driving E2 and E3 with external address signals, the four devices can be made to look like one larger device.

When these devices are deselected via chip enable $\overline{E1}$, the output clocks continue to toggle. However, when these devices are deselected via programmable chip enables E2 or E3, the output clocks are forced to a Hi-Z state. See the Clock Truth Table for further information.

•Output Driver Impedance Control

The impedance of the data and clock output drivers in these devices can be controlled via the static input ZQ. When ZQ is tied “low”, output driver impedance is set to ~25Ω. When ZQ is tied “high” or left unconnected, output driver impedance is set to ~50Ω. See the DC Electrical Characteristics section for further information.

•Power-Up Sequence

For reliability purposes, Sony recommends that power supplies power up in the following sequence: V_{SS}, V_{DD}, V_{DDQ}, and Inputs. V_{DDQ} should never exceed V_{DD}. If this power supply sequence cannot be met, a large bypass diode may be required between V_{DD} and V_{DDQ}. Please contact Sony Memory Application Department for further information.

•Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Supply Voltage	V_{DD}	-0.5 to +2.5	V
Output Supply Voltage	V_{DDQ}	-0.5 to +2.3	V
Input Voltage (Address, Control, Data, Clock)	V_{IN}	-0.5 to V_{DDQ}+0.5 (2.3V max)	V
Input Voltage (EP2, EP3, MCL, MCH, ZQ)	V_{MIN}	-0.5 to V_{DD}+0.5 (2.5V max)	V
Input Voltage (TCK, TMS, TDI)	V_{TIN}	-0.5 to V_{DD}+0.5 (2.5V max)	V
Operating Temperature	T_A	0 to 85	°C
Junction Temperature	T_J	0 to 110	°C
Storage Temperature	T_{STG}	-55 to 150	°C

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions other than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

•BGA Package Thermal Characteristics

Parameter	Symbol	Rating	Units
Junction to Case Temperature	Θ_{JC}	3.6	°C/W

•I/O Capacitance

(T_A = 25°C, f = 1 MHz)

Parameter		Symbol	Test conditions	Min	Max	Units
Input Capacitance	Address	C_{IN}	$V_{IN} = 0V$	---	3.5	pF
	Control	C_{IN}	$V_{IN} = 0V$	---	3.5	pF
	CK Clock	C_{KIN}	$V_{KIN} = 0V$	---	4.0	pF
Output Capacitance	Data	C_{OUT}	$V_{OUT} = 0V$	---	4.5	pF
	CQ Clock	C_{OUT}	$V_{OUT} = 0V$	---	4.5	pF

Note: These parameters are sampled and are not 100% tested.

•DC Recommended Operating Conditions

(V_{SS} = 0V, T_A = 0 to 85^{o}C)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Supply Voltage	V_{DD}	1.7	1.8	1.95	V	
Output Supply Voltage	V_{DDQ}	1.4	---	V_{DD}	V	
Input High Voltage (Address, Control, Data, Clock)	V_{IH}	$V_{DDQ}/2 + 0.3$	---	$V_{DDQ} + 0.3$	V	1
Input Low Voltage (Address, Control, Data, Clock)	V_{IL}	-0.3	---	$V_{DDQ}/2 - 0.3$	V	2
Input High Voltage (EP2, EP3, MCH, ZQ)	V_{MIH}	$V_{DDQ}/2 + 0.4$	---	$V_{DD} + 0.3$	V	
Input Low Voltage (EP2, EP3, MCL, ZQ)	V_{MIL}	-0.3	---	$V_{DDQ}/2 - 0.4$	V	

1. V_{IH} (max) AC = V_{DDQ} + 0.9V for pulse widths less than one-quarter of the cycle time ($t_{CYC}/4$).
2. V_{IL} (min) AC = -0.9V for pulse widths less than one-quarter of the cycle time ($t_{CYC}/4$).

•DC Electrical Characteristics

(V_{DD} = 1.8V ± 0.1V, V_{SS} = 0V, T_A = 0 to 85°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	Notes
Input Leakage Current (Address, Control, Clock)	I_{LI}	$V_{IN} = V_{SS}$ to V_{DDQ}	-5	---	5	uA	
Input Leakage Current (EP2, EP3)	I_{MLI1}	$V_{MIN} = V_{SS}$ to V_{DD}	-10	---	10	uA	
Input Leakage Current (MCH)	I_{MLI2}	$V_{MIN} = V_{MIH}$ (min) to V_{DD}	-10	---	10	uA	
Input Leakage Current (MCL)	I_{MLI3}	$V_{MIN} = V_{SS}$ to V_{MIL} (max)	-10	---	10	uA	
Output Leakage Current	I_{LO}	$V_{OUT} = V_{SS}$ to V_{DDQ}	-10	---	10	uA	
Average Power Supply Operating Current (x72)	I_{DD-33} I_{DD-4} I_{DD-5}	I_{OUT} = 0 mA $V_{IN} = V_{IH}$ or V_{IL}	--- --- ---	--- --- ---	750 650 550	mA	
Average Power Supply Operating Current (x36)	I_{DD-33} I_{DD-4} I_{DD-5}	I_{OUT} = 0 mA $V_{IN} = V_{IH}$ or V_{IL}	--- --- ---	--- --- ---	580 500 420	mA	
Average Power Supply Operating Current (x18)	I_{DD-33} I_{DD-4} I_{DD-5}	I_{OUT} = 0 mA $V_{IN} = V_{IH}$ or V_{IL}	--- --- ---	--- --- ---	490 430 380	mA	
Power Supply Deselect Operating Current	I_{DD2}	I_{OUT} = 0 mA $V_{IN} = V_{IH}$ or V_{IL}	---	---	250	mA	
Output High Voltage	V_{OH}	I_{OH} = -6.0 mA $ZQ = V_{IH}$	V_{DDQ} - 0.4	---	---	V	
Output Low Voltage	V_{OL}	I_{OL} = 6.0 mA $ZQ = V_{IH}$	---	---	0.4	V	
Output Driver Impedance	R_{OUT}	V_{OH}, $V_{OL} = V_{DDQ}/2$ $ZQ = V_{IL}$	17	25	33	Ω	
		V_{OH}, $V_{OL} = V_{DDQ}/2$ $ZQ = V_{IH}$	35	50	65	Ω	

•AC Electrical Characteristics

(V_{DD} = 1.8V ± 0.1V, V_{SS} = 0V, T_A = 0 to 85^{o}C)

Parameter	Symbol	-33		-4		-5		Units	Notes
		Min	Max	Min	Max	Min	Max		
Input Clock Cycle Time	t_{KHKH}	3.3	---	4.0	---	5.0	---	ns	
Input Clock High Pulse Width	t_{KHKL}	1.3	---	1.5	---	2.0	---	ns	
Input Clock Low Pulse Width	t_{KLKH}	1.3	---	1.5	---	2.0	---	ns	
Address Input Setup Time	t_{AVKH}	0.7	---	0.8	---	1.0	---	ns	
Address Input Hold Time	t_{KHAX}	0.4	---	0.5	---	0.5	---	ns	
Control Input Setup Time	t_{BVKH}	0.7	---	0.8	---	1.0	---	ns	1
Control Input Hold Time	t_{KHBX}	0.4	---	0.5	---	0.5	---	ns	1
Data Input Setup Time	t_{DVKH}	0.7	---	0.8	---	1.0	---	ns	
Data Input Hold Time	t_{KHDX}	0.4	---	0.5	---	0.5	---	ns	
Input Clock High to Output Data Valid	t_{KHQV}	---	1.8	---	2.1	---	2.3	ns	
Input Clock High to Output Data Hold	t_{KHQX}	0.5	---	0.5	---	0.5	---	ns	2
Input Clock High to Output Data Low-Z	t_{KHQX1}	0.5	---	0.5	---	0.5	---	ns	2,3
Input Clock High to Output Data High-Z	t_{KHQZ}	---	1.8	---	2.1	---	2.3	ns	2,3
Input Clock High to Output Clock High	t_{KHCH}	0.5	1.8	0.5	2.1	0.5	2.3	ns	
Input Clock High to Output Clock Low-Z	t_{KHCX1}	0.5	---	0.5	---	0.5	---	ns	2,3
Input Clock High to Output Clock High-Z	t_{KHCZ}	---	1.8	---	2.1	---	2.3	ns	2,3
Output Clock High to Output Data Valid	t_{CHQV}	---	0.4	---	0.5	---	0.6	ns	2
Output Clock High to Output Data Hold	t_{CHQX}	-0.4	---	-0.5	---	-0.6	---	ns	2
Output Clock High Pulse Width	t_{CHCL}	$t_{KHKL} \pm 0.2$		$t_{KHKL} \pm 0.2$		$t_{KHKL} \pm 0.2$		ns	2
Output Clock Low Pulse Width	t_{CLCH}	$t_{KLKH} \pm 0.2$		$t_{KLKH} \pm 0.2$		$t_{KLKH} \pm 0.2$		ns	2

All parameters are measured from the mid-point of the object signal to the mid-point of the reference signal, unless otherwise noted.

1. These parameters apply to control inputs $\overline{E1}$, E2, E3, ADV, $\overline{W}$, and $\overline{Bx}$.
2. These parameters are guaranteed by design through extensive corner lot characterization.
3. These parameters are measured at ± 50mV from steady state voltage.

•AC Electrical Characteristics (Note)

The two AC timing parameters listed below are tested according to specific combinations of Output Clocks (CQs) and Output Data (DQs):

1. t_{CHQV} - Output Clock High to Output Data Valid (max)
2. t_{CHQX} - Output Clock High to Output Data Hold (min)

The specific CQ / DQ combinations are defined as follows:

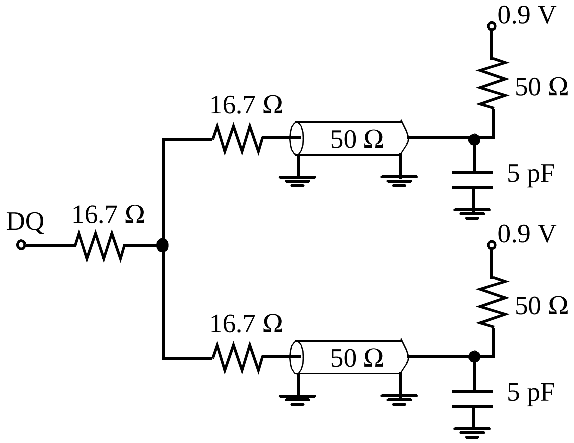
256Kb x 72		512Kb x 36		1Mb x 18	
CQs	DQs	CQs	DQs	CQs	DQs
1K, 2K	1A, 2A, 1B, 2B, 1C, 2C, 1D, 2D, 1E, 2E, 1F, 2F, 1G, 2G, 1H, 2H, 1J, 2J, 1L, 2L, 1M, 2M, 1N, 2N, 1P, 2P, 2R, 1R, 1T, 2T, 1U, 2U, 1V, 2V, 1W, 2W	1K, 2K	2E, 1F, 2F, 1G, 2G, 1H, 2H, 1J, 2J, 1R, 1T, 2T, 1U, 2U, 1V, 2V, 1W, 2W	1K, 2K	2E, 1F, 2F, 1G, 2G, 1H, 2H, 1J, 2J
10K, 11K	10A, 11A, 10B, 11B, 10C, 11C, 10D, 11D, 11E, 10E, 10F, 11F, 10G, 11G, 10H, 11H, 10J, 11J, 10L, 11L, 10M, 11M, 10N, 11N, 10P, 11P, 10R, 11R, 10T, 11T, 10U, 11U, 10V, 11V, 10W, 11W	10K, 11K	10A, 11A, 10B, 11B, 10C, 11C, 10D, 11D, 11E, 10L, 11L, 10M, 11M, 10N, 11N, 10P, 11P, 10R	10K, 11K	10L, 11L, 10M, 11M, 10N, 11N, 10P, 11P, 10R

•AC Test Conditions (V_{DDQ} = 1.8V)

(V_{DD} = 1.8V ± 0.1V, V_{DDQ} = 1.8V ± 0.1V, T_A = 0 to 85°C)

Parameter	Symbol	Conditions	Units	Notes
Input High Level	V_{IH}	1.4	V	
Input Low Level	V_{IL}	0.4	V	
Input Rise & Fall Time		2.0	V/ns	
Input Reference Level		0.9	V	
Clock Input High Voltage	V_{KIH}	1.4	V	
Clock Input Low Voltage	V_{KIL}	0.4	V	
Clock Input Rise & Fall Time		2.0	V/ns	
Clock Input Reference Level		0.9	V	
Output Reference Level		0.9	V	
Output Load Conditions		ZQ = V_{IH}		See Figure 1 below

Figure 1: AC Test Output Load (V_{DDQ} = 1.8V)

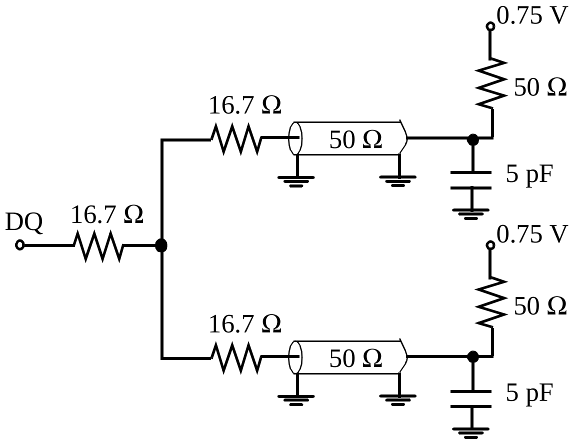


•AC Test Conditions (V_{DDQ} = 1.5V)

(V_{DD} = 1.8V ± 0.1V, V_{DDQ} = 1.5V ± 0.1V, T_A = 0 to 85°C)

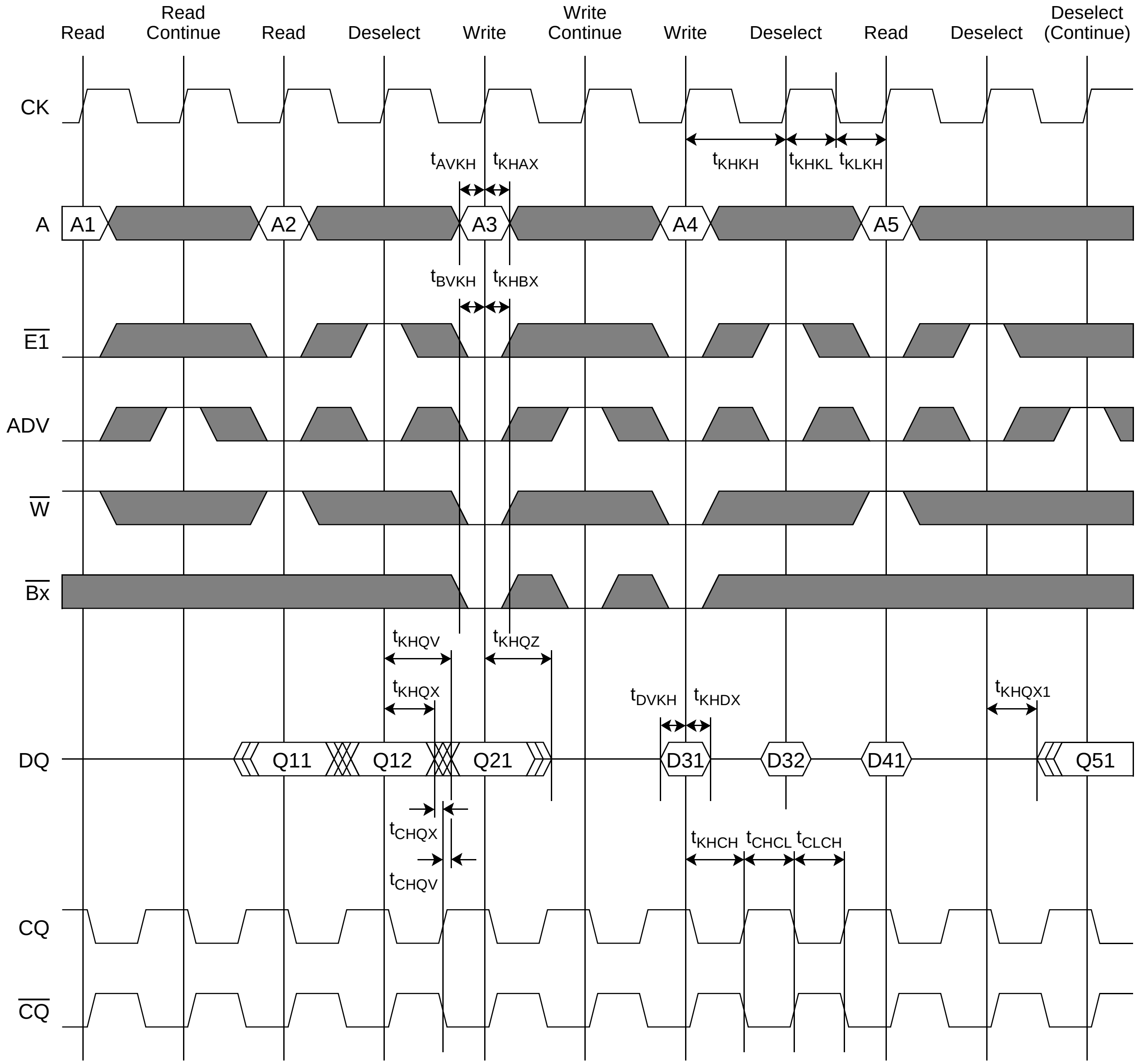
Parameter	Symbol	Conditions	Units	Notes
Input High Level	V_{IH}	1.25	V	
Input Low Level	V_{IL}	0.25	V	
Input Rise & Fall Time		2.0	V/ns	
Input Reference Level		0.75	V	
Clock Input High Voltage	V_{KIH}	1.25	V	
Clock Input Low Voltage	V_{KIL}	0.25	V	
Clock Input Rise & Fall Time		2.0	V/ns	
Clock Input Reference Level		0.75	V	
Output Reference Level		0.75	V	
Output Load Conditions		ZQ = V_{IH}		See Figure 2 below

Figure 2: AC Test Output Load (V_{DDQ} = 1.5V)



One Bank Read-Write-Read Timing Diagram

Figure 3

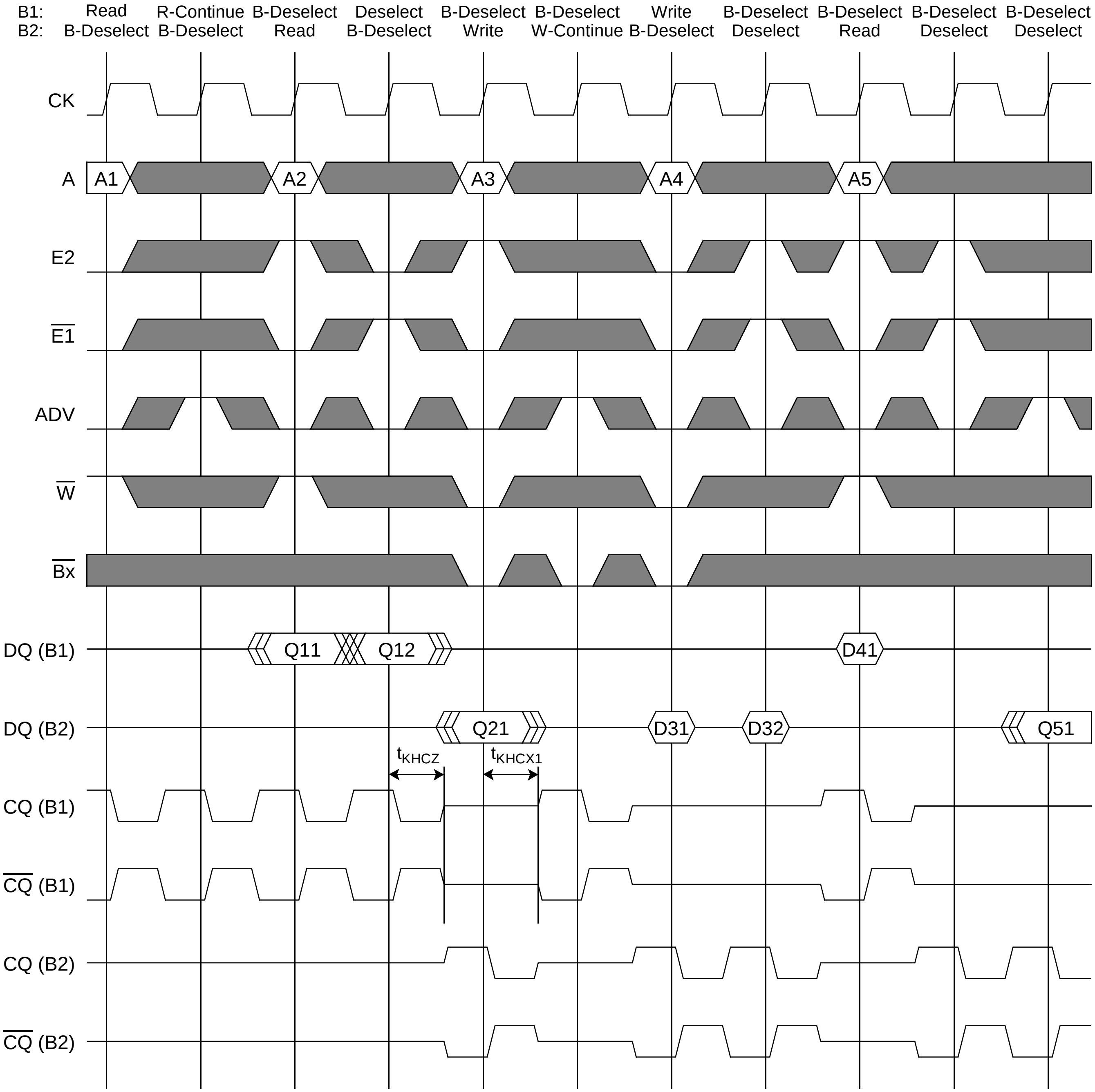


Note: In the diagram above, a Deselect operation is inserted between Read and Write operations to control the data bus transition from output to input. Similarly, a Deselect operation is inserted between Write and Read operations to control the data bus transition from input to output. This depiction is for clarity purposes only. It is NOT a requirement. Depending on the application, these Deselect operations may not be necessary.

Note: E1 = EP1 and E2 = EP2 in this example (not shown).

Two Bank Read-Write-Read Timing Diagram

Figure 4



Note: In the diagram above, a Deselect operation is inserted between Read and Write operations to control the data bus transition from output to input. Similarly, a Deselect operation is inserted between Write and Read operations to control the data bus transition from input to output. This depiction is for clarity purposes only. It is NOT a requirement. Depending on the application, these Deselect operations may not be necessary.

Note: Bank 1 EP1 = “low”, Bank 2 EP1 “high”, and Bank 1 and Bank 2 E2 = EP2 in this example (not shown).

•Test Mode Description

These devices provide a JTAG Test Access Port (TAP) and Boundary Scan interface using a limited set of IEEE std. 1149.1 functions. This test mode is intended to provide a mechanism for testing the interconnect between master (processor, controller, etc.), SRAMs, other components, and the printed circuit board.

In conformance with a subset of IEEE std. 1149.1, these devices contain a TAP Controller and four TAP Registers. The TAP Registers consist of one Instruction Register and three Data Registers (ID, Bypass, and Boundary Scan Registers).

The TAP consists of the following four signals:

TCK:	Test Clock	Induces (clocks) TAP Controller state transitions.
TMS:	Test Mode Select	Inputs commands to the TAP Controller. Sampled on the rising edge of TCK.
TDI:	Test Data In	Inputs data serially to the TAP Registers. Sampled on the rising edge of TCK.
TDO:	Test Data Out	Outputs data serially from the TAP Registers. Driven from the falling edge of TCK.

Disabling the TAP

When JTAG is not used, TCK should be tied “low” to prevent clocking the SRAM. TMS and TDI should either be tied “high” through a pull-up resistor or left unconnected. TDO should be left unconnected.

Note: Operation of the TAP does not disrupt normal SRAM operation except when the EXTEST-A or SAMPLE-Z instruction is selected. Consequently, TCK, TMS, and TDI can be controlled any number of ways without adversely affecting the functionality of the device.

JTAG DC Recommended Operating Conditions

(V_{DD} = 1.8V ± 0.1V, T_A = 0 to 85°C)

Parameter	Symbol	Test Conditions	Min	Max	Units
JTAG Input High Voltage (TCK, TMS, TDI)	V_{TIH}	---	$V_{DD}/2 + 0.3$	$V_{DD} + 0.3$	V
JTAG Input Low Voltage (TCK, TMS, TDI)	V_{TIL}	---	-0.3	$V_{DD}/2 - 0.3$	V
JTAG Output High Voltage (TDO)	V_{TOH}	I_{TOH} = -100uA	$V_{DD} - 0.1$	---	V
JTAG Output Low Voltage (TDO)	V_{TOL}	I_{TOL} = 100uA	---	0.1	V
JTAG Output High Voltage (TDO)	V_{TOH}	I_{TOH} = -8mA	$V_{DD} - 0.4$	---	V
JTAG Output Low Voltage (TDO)	V_{TOL}	I_{TOL} = 8mA	---	0.4	V
JTAG Input Leakage Current	I_{TLI}	$V_{TIN} = V_{SS}$ to V_{DD}	-20	10	uA
JTAG Output Leakage Current	I_{TLO}	$V_{TOUT} = V_{SS}$ to V_{DD}	-10	10	uA

JTAG AC Test Conditions

(V_{DD} = 1.8V ± 0.1V, T_A = 0 to 85°C)

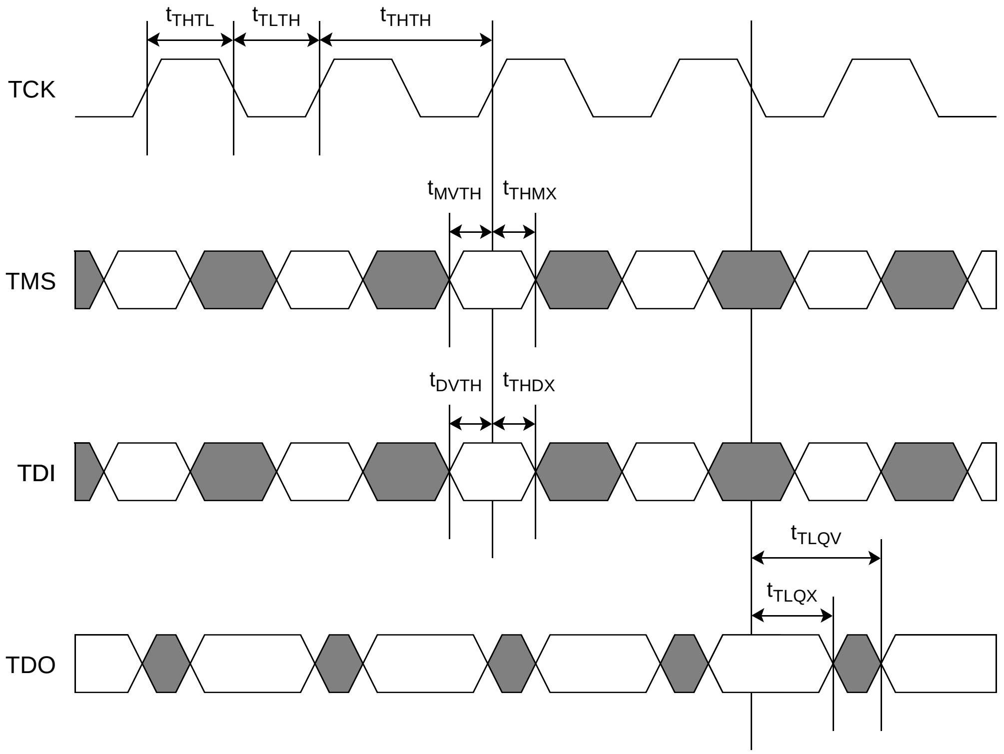
Parameter	Symbol	Conditions	Units	Notes
JTAG Input High Level	V_{TIH}	1.8	V	
JTAG Input Low Level	V_{TIL}	0.0	V	
JTAG Input Rise & Fall Time		1.0	V/ns	
JTAG Input Reference Level		0.9	V	
JTAG Output Reference Level		0.9	V	
JTAG Output Load Condition				See Fig. 1 (page 15)

JTAG AC Electrical Characteristics

Parameter	Symbol	Min	Max	Units
TCK Cycle Time	t_{THTH}	50		ns
TCK High Pulse Width	t_{THTL}	20		ns
TCK Low Pulse Width	t_{TLTH}	20		ns
TMS Setup Time	t_{MVTH}	5		ns
TMS Hold Time	t_{THMX}	5		ns
TDI Setup Time	t_{DVTH}	5		ns
TDI Hold Time	t_{THDX}	5		ns
Capture Setup Time (Address, Control, Data, Clock)	t_{CS}	5		ns
Capture Hold Time (Address, Control, Data, Clock)	t_{CH}	5		ns
TCK Low to TDO Valid	t_{TLQV}		10	ns
TCK Low to TDO Hold	t_{TLQX}	0		ns

JTAG Timing Diagram

Figure 5



TAP Controller

The TAP Controller is a 16-state state machine that controls access to the various TAP Registers and executes the operations associated with each TAP Instruction (see Figure 7 below). State transitions are controlled by TMS and occur on the rising edge of TCK.

The TAP Controller enters the “Test-Logic Reset” state in one of two ways:

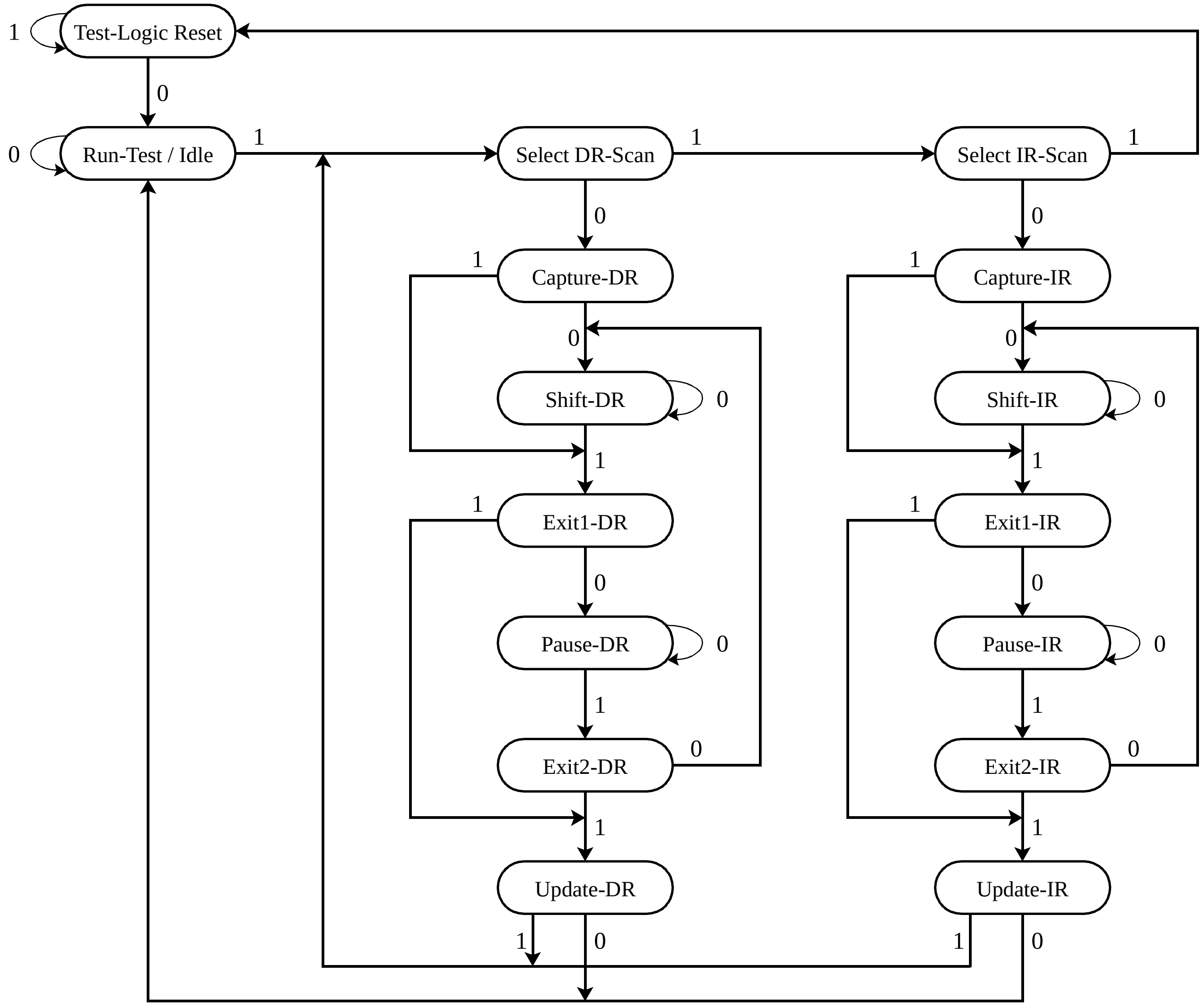
1. At power up.
2. When a logic “1” is applied to TMS for at least 5 consecutive rising edges of TCK.

The TDI input receiver is sampled only when the TAP Controller is in either the “Shift-IR” state or the “Shift-DR” state.

The TDO output driver is active only when the TAP Controller is in either the “Shift-IR” state or the “Shift-DR” state.

TAP Controller State Diagram

Figure 6



TAP Registers

TAP Registers are serial shift registers that capture serial input data (from TDI) on the rising edge of TCK, and drive serial output data (to TDO) on the subsequent falling edge of TCK. They are divided into two groups: “Instruction Registers” (IR), which are manipulated via the “IR” states in the TAP Controller, and “Data Registers” (DR), which are manipulated via the “DR” states in the TAP Controller.

Instruction Register (IR - 3 bits)

The Instruction Register stores the various TAP Instructions supported by these devices. It is loaded with the IDCODE instruction at power-up, and when the TAP Controller is in the “Test-Logic Reset” and “Capture-IR” states. It is inserted between TDI and TDO when the TAP Controller is in the “Shift-IR” state, at which time it can be loaded with a new instruction. However, newly loaded instructions are not executed until the TAP Controller has reached the “Update-IR” state.

The Instruction Register is 3 bits wide, and is encoded as follows:

Code (2:0)	Instruction	Description
000	EXTEST-A	Loads the individual logic states of all signals composing the SRAM’s I/O ring into the Boundary Scan Register when the TAP Controller is in the “Capture-DR” state, and inserts the B-Scan Register between TDI and TDO when the TAP Controller is in the “Shift-DR” state. Also enables the SRAM’s data and clock output drivers, and moves the contents of the B-Scan Register associated with the data and clock output signals to the input side of the SRAM’s output register. The SRAM’s input clock can then be used to transfer the B-Scan Register contents directly to the data and clock output pins (the input clock controls the SRAM’s output register). Note that newly captured and/or shifted B-Scan Register contents do not appear at the input side of the SRAM’s output register until the TAP Controller has reached the “Update-DR” state. See the Boundary Scan Register description for more information.
001	IDCODE	Loads a predefined device- and manufacturer-specific identification code into the ID Register when the TAP Controller is in the “Capture-DR” state, and inserts the ID Register between TDI and TDO when the TAP Controller is in the “Shift-DR” state. See the ID Register description for more information.
010	SAMPLE-Z	Loads the individual logic states of all signals composing the SRAM’s I/O ring into the Boundary Scan Register when the TAP Controller is in the “Capture-DR” state, and inserts the B-Scan Register between TDI and TDO when the TAP Controller is in the “Shift-DR” state. Also disables the SRAM’s data and clock output drivers. See the Boundary Scan Register description for more information.
011	PRIVATE	Do not use. Reserved for manufacturer use only.
100	SAMPLE	Loads the individual logic states of all signals composing the SRAM’s I/O ring into the Boundary Scan Register when the TAP Controller is in the “Capture-DR” state, and inserts the Boundary Scan Register between TDI and TDO when the TAP Controller is in the “Shift-DR” state. See the Boundary Scan Register description for more information.
101	PRIVATE	Do not use. Reserved for manufacturer use only.
110	PRIVATE	Do not use. Reserved for manufacturer use only.
111	BYPASS	Loads a logic “0” into the Bypass Register when the TAP Controller is in the “Capture-DR” state, and inserts the Bypass Register between TDI and TDO when the TAP Controller is in the “Shift-DR” state. See the Bypass Register description for more information.

Bit 0 is the LSB of the Instruction Register, and Bit 2 is the MSB. When the Instruction Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

Bypass Register (DR - 1 bit)

The Bypass Register is one bit wide, and provides the minimum length serial path between TDI and TDO. It is loaded with a logic "0" when the BYPASS instruction has been loaded in the Instruction Register and the TAP Controller is in the "Capture-DR" state. It is inserted between TDI and TDO when the BYPASS instruction has been loaded into the Instruction Register and the TAP Controller is in the "Shift-DR" state.

ID Register (DR - 32 bits)

The ID Register is loaded with a predetermined device- and manufacturer-specific identification code when the IDCODE instruction has been loaded into the Instruction Register and the TAP Controller is in the "Capture-DR" state. It is inserted between TDI and TDO when the IDCODE instruction has been loaded into the Instruction Register and the TAP Controller is in the "Shift-DR" state.

The ID Register is 32 bits wide, and is encoded as follows:

Device	Revision Number (31:28)	Part Number (27:12)	Sony ID (11:1)	Start Bit (0)
256Kb x 72	xxxx	0000 0000 0101 1000	0000 1110 001	1
512Kb x 36	xxxx	0000 0000 0101 1110	0000 1110 001	1
1Mb x 18	xxxx	0000 0000 0110 0100	0000 1110 001	1

Bit 0 is the LSB of the ID Register, and Bit 31 is the MSB. When the ID Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

Boundary Scan Register (DR - 123 bits for x72, 84 bits for x36, 65 bits for x18)

The Boundary Scan Register is equal in length to the number of active signal connections to the SRAM (excluding the TAP pins) plus a number of place holder locations reserved for functional and/or density upgrades. It is loaded with the individual logic states of all signals composing the SRAM's I/O ring when the EXTEST-A, SAMPLE, or SAMPLE-Z instruction has been loaded into the Instruction Register and the TAP Controller is in the "Capture-DR" state. It is inserted between TDI and TDO when the EXTEST-A, SAMPLE, or SAMPLE-Z instruction has been loaded into the Instruction Register and the TAP Controller is in the "Shift-DR" state.

The Boundary Scan Register contains the following bits:

256Kb x 72		512Kb x 36		1Mb x 18	
DQx	72	DQx	36	DQx	18
A, A1, A0	18	A, A1, A0	19	A, A1, A0	20
CK	1	CK	1	CK	1
CQ1, CQ2, $\overline{\text{CQ1}}$, $\overline{\text{CQ2}}$	4	CQ1, CQ2, $\overline{\text{CQ1}}$, $\overline{\text{CQ2}}$	4	CQ1, CQ2, $\overline{\text{CQ1}}$, $\overline{\text{CQ2}}$	4
$\overline{\text{E1}}$, ADV, $\overline{\text{W}}$, $\overline{\text{Bx}}$	11	$\overline{\text{E1}}$, ADV, $\overline{\text{W}}$, $\overline{\text{Bx}}$	7	$\overline{\text{E1}}$, ADV, $\overline{\text{W}}$, $\overline{\text{Bx}}$	5
E2, E3, EP2, EP3	4	E2, E3, EP2, EP3	4	E2, E3, EP2, EP3	4
ZQ	1	ZQ	1	ZQ	1
Place Holder	12	Place Holder	12	Place Holder	12

Boundary Scan Register Bit Order Assignments

The tables below depict the order in which the bits are arranged in the Boundary Scan Register. Bit 1 is the LSB and bit 123 (for x72) or bit 84 (for x36) or bit 65 (for x18) is the MSB. When the Boundary Scan Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

256Kb x 72											
Bit	Signal	Pad	Bit	Signal	Pad	Bit	Signal	Pad	Bit	Signal	Pad
1	NC (1)	5C	36	DQf	11G	71	DQg	1A	106	DQd	2V
2	NC (1)	5U	37	DQf	10F	72	DQg	1B	107	DQd	1V
3	NC (1)	7U	38	DQf	11F	73	DQg	2B	108	DQd	1W
4	MCL (1)	6D	39	DQf	10E	74	DQg	1C	109	DQd	2W
5	MCL (1)	6K	40	DQb	11E	75	DQg	2C	110	MCH	6J
6	MCL (1)	6P	41	DQb	10D	76	DQg	1D	111	A	3V
7	MCL (1)	6T	42	DQb	11D	77	DQg	2D	112	A	4V
8	MCH (2)	6N	43	DQb	10C	78	DQg	1E	113	A	4U
9	MCL	6M	44	DQb	11C	79	DQc	2E	114	A	5V
10	MCH	6L	45	DQb	10B	80	DQc	1F	115	A	6U
11	DQe	10W	46	DQb	11B	81	DQc	2F	116	A	5W
12	DQe	11W	47	DQb	11A	82	DQc	1G	117	A0	6W
13	DQe	11V	48	DQb	10A	83	DQc	2G	118	A1	6V
14	DQe	10V	49	$\overline{\text{Bf}}$	9B	84	DQc	1H	119	A	7V
15	DQe	11U	50	$\overline{\text{Ba}}$	9C	85	DQc	2H	120	A	8V
16	DQe	10U	51	$\overline{\text{Bb}}$	8B	86	DQc	1J	121	A	7W
17	DQe	11T	52	$\overline{\text{Be}}$	8C	87	DQc	2J	122	A	8U
18	DQe	10T	53	EP3	6H	88	CQ2	1K	123	A	9V
19	DQe	11R	54	EP2	6G	89	CK	3K			
20	DQa	10R	55	A	9A	90	NC (1)	4K			
21	DQa	11P	56	E3	8A	91	$\overline{\text{CQ2}}$	2K			
22	DQa	10P	57	A	7B	92	DQh	2L			
22	DQa	11N	58	A	7A	93	DQh	1L			
24	DQa	10N	59	$\overline{\text{W}}$	6B	94	DQh	2M			
25	DQa	11M	60	ADV	6A	95	DQh	1M			
26	DQa	10M	61	$\overline{\text{E1}}$	6C	96	DQh	2N			
27	DQa	11L	62	A	5A	97	DQh	1N			
28	DQa	10L	63	E2	4A	98	DQh	2P			
29	CQ1	11K	64	A	3A	99	DQh	1P			
30	$\overline{\text{CQ1}}$	10K	65	ZQ	6F	100	DQh	2R			
31	DQf	10J	66	$\overline{\text{Bd}}$	4C	101	DQd	1R			
32	DQf	11J	67	$\overline{\text{Bg}}$	4B	102	DQd	2T			
33	DQf	10H	68	$\overline{\text{Bh}}$	3C	103	DQd	1T			
34	DQf	11H	69	$\overline{\text{Bc}}$	3B	104	DQd	2U			
35	DQf	10G	70	DQg	2A	105	DQd	1U			

Note 1: NC and MCL pins at pad locations 5C, 5U, 7U, 6D, 6K, 6P, 6T, and 4K are connected to V_{SS} internally, regardless of pin connection externally.

Note 2: MCH pin at pad location 6N is connected to V_{DD} internally, regardless of pin connection externally.

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512Kb x 36								
Bit	Signal	Pad	Bit	Signal	Pad	Bit	Signal	Pad
1	NC (1)	5C	36	E3	8A	71	MCH	6J
2	NC (1)	5U	37	A	7B	72	A	3V
3	NC (1)	7U	38	A	7A	73	A	4V
4	MCL (1)	6D	39	$\overline{W}$	6B	74	A	4U
5	MCL (1)	6K	40	ADV	6A	75	A	5V
6	MCL (1)	6P	41	$\overline{E1}$	6C	76	A	6U
7	MCL (1)	6T	42	A	5A	77	A	5W
8	MCH (2)	6N	43	A	5B	78	A0	6W
9	MCL	6M	44	E2	4A	79	A1	6V
10	MCH	6L	45	A	3A	80	A	7V
11	DQa	10R	46	ZQ	6F	81	A	8V
12	DQa	11P	47	$\overline{Bd}$	4C	82	A	7W
13	DQa	10P	48	$\overline{Bc}$	3B	83	A	8U
14	DQa	11N	49	DQc	2E	84	A	9V
15	DQa	10N	50	DQc	1F			
16	DQa	11M	51	DQc	2F			
17	DQa	10M	52	DQc	1G			
18	DQa	11L	53	DQc	2G			
19	DQa	10L	54	DQc	1H			
20	CQ1	11K	55	DQc	2H			
21	$\overline{CQ1}$	10K	56	DQc	1J			
22	DQb	11E	57	DQc	2J			
22	DQb	10D	58	CQ2	1K			
24	DQb	11D	59	CK	3K			
25	DQb	10C	60	NC (1)	4K			
26	DQb	11C	61	$\overline{CQ2}$	2K			
27	DQb	10B	62	DQd	1R			
28	DQb	11B	63	DQd	2T			
29	DQb	11A	64	DQd	1T			
30	DQb	10A	65	DQd	2U			
31	$\overline{Ba}$	9C	66	DQd	1U			
32	$\overline{Bb}$	8B	67	DQd	2V			
33	EP3	6H	68	DQd	1V			
34	EP2	6G	69	DQd	1W			
35	A	9A	70	DQd	2W			

Note 1: NC and MCL pins at pad locations 5C, 5U, 7U, 6D, 6K, 6P, 6T, and 4K are connected to V_{SS} internally, regardless of pin connection externally.

Note 2: MCH pin at pad location 6N is connected to V_{DD} internally, regardless of pin connection externally.

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1Mb x 18					
Bit	Signal	Pad	Bit	Signal	Pad
1	NC (1)	5C	36	A	3A
2	NC (1)	5U	37	ZQ	6F
3	NC (1)	7U	38	$\overline{\mathrm{Bb}}$	3B
4	MCL (1)	6D	39	DQb	2E
5	MCL (1)	6K	40	DQb	1F
6	MCL (1)	6P	41	DQb	2F
7	MCL (1)	6T	42	DQb	1G
8	MCH (2)	6N	43	DQb	2G
9	MCL	6M	44	DQb	1H
10	MCH	6L	45	DQb	2H
11	DQa	10R	46	DQb	1J
12	DQa	11P	47	DQb	2J
13	DQa	10P	48	CQ2	1K
14	DQa	11N	49	CK	3K
15	DQa	10N	50	NC (1)	4K
16	DQa	11M	51	$\overline{\mathrm{CQ2}}$	2K
17	DQa	10M	52	MCH	6J
18	DQa	11L	53	A	3V
19	DQa	10L	54	A	4V
20	CQ1	11K	55	A	4U
21	$\overline{\mathrm{CQ1}}$	10K	56	A	5V
22	$\overline{\mathrm{Ba}}$	9C	57	A	6U
22	EP3	6H	58	A	5W
24	EP2	6G	59	A0	6W
25	A	9A	60	A1	6V
26	E3	8a	61	A	7V
27	A	7C	62	A	8V
28	A	7B	63	A	7W
29	A	7A	64	A	8U
30	$\overline{\mathrm{W}}$	6B	65	A	9V
31	ADV	6A			
32	$\overline{\mathrm{E1}}$	6C			
33	A	5A			
34	A	5B			
35	E2	4A			

Note 1: NC and MCL pins at pad locations 5C, 5U, 7U, 6D, 6K, 6P, 6T, and 4K are connected to V_{SS} internally, regardless of pin connection externally.

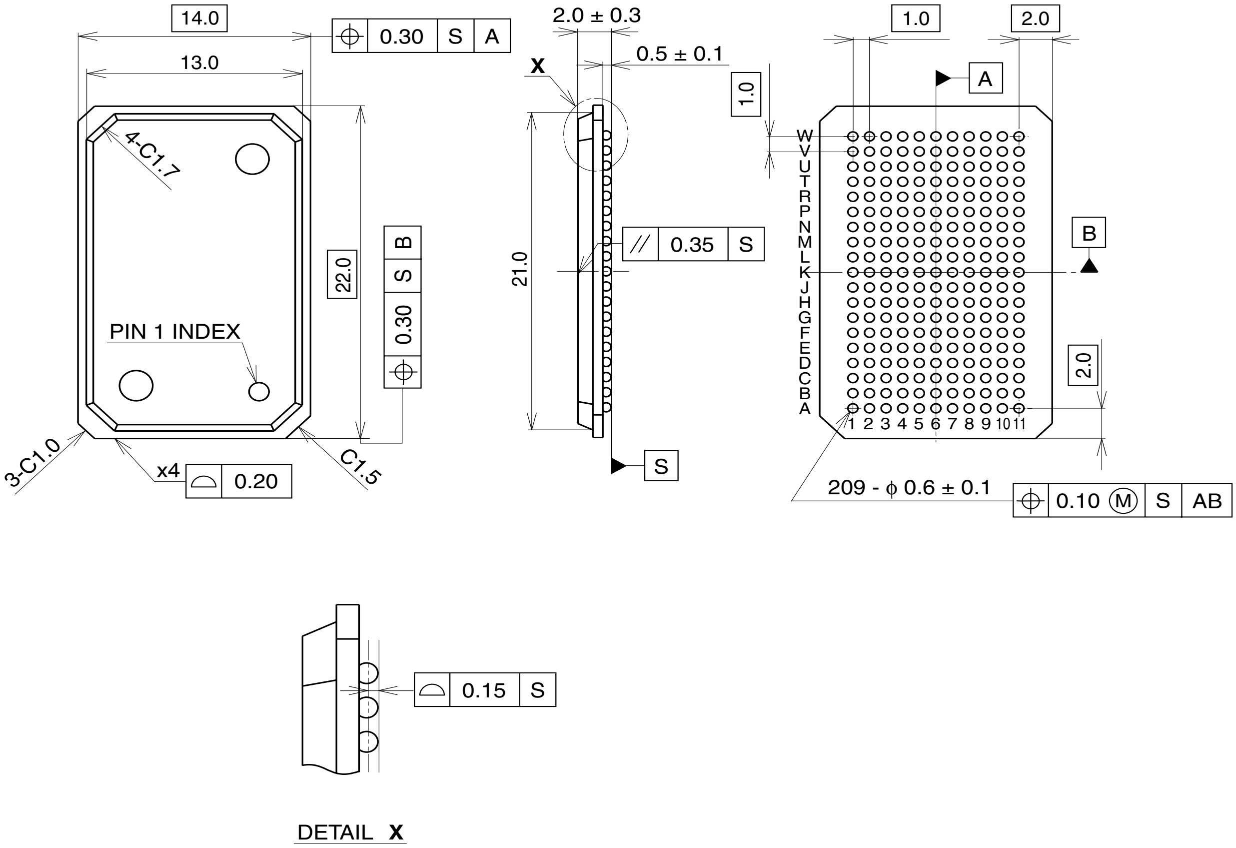
Note 2: MCH pin at pad location 6N is connected to V_{DD} internally, regardless of pin connection externally.

•Ordering Information

Part Number	V_{DD}	I/O Type	Configuration	Speed (Cycle Time / Data Access Time)
CXK79M72C165GB-33	1.8V	LVCMOS	256Kb x 72	3.3ns / 1.8ns
CXK79M72C165GB-4	1.8V	LVCMOS	256Kb x 72	4.0ns / 2.1ns
CXK79M72C165GB-5	1.8V	LVCMOS	256Kb x 72	5.0ns / 2.3ns
CXK79M36C165GB-33	1.8V	LVCMOS	512Kb x 36	3.3ns / 1.8ns
CXK79M36C165GB-4	1.8V	LVCMOS	512Kb x 36	4.0ns / 2.1ns
CXK79M36C165GB-5	1.8V	LVCMOS	512Kb x 36	5.0ns / 2.3ns
CXK79M18C165GB-33	1.8V	LVCMOS	1Mb x 18	3.3ns / 1.8ns
CXK79M18C165GB-4	1.8V	LVCMOS	1Mb x 18	4.0ns / 2.1ns
CXK79M18C165GB-5	1.8V	LVCMOS	1Mb x 18	5.0ns / 2.3ns

•(11x19) 209 Pin BGA Package Dimensions

209PIN BGA (PLASTIC)



PRELIMINARY

SONY CODE	BGA-209P-01
JEITA CODE	P-BGA209-14X22-1.0
JEDEC CODE	——

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	COPPER-CLAD LAMINATE
TERMINAL MATERIAL	SOLDER
PACKAGE MASS	1.1g

•Revision History

Rev. #	Rev. Date	Description of Modifications
rev 0.0	06/23/00	Initial Version.
rev 0.1	02/23/01	1. Added Sony Part Numbers for each device. 2. Removed Asynchronous Output Enable ($\overline{G}$) support. Pin 6D now defined as "MCL". 3. Modified DC Recommended Operating Conditions section (p. 10). $V_{MIH-1.8}$ (min) 1.2V to 1.3V $V_{MIH-1.5}$ (min) 1.2V to 1.1V $V_{MIL-1.8}$ (max) 0.3V to 0.5V $V_{MIL-1.5}$ (max) 0.3V to 0.4V 3. Modified DC Electrical Characteristics section (p. 11). Added I_{DD-4} Average Power Supply Operating Current specifications. Added I_{DD2} Power Supply Deselect Operating Current specification. 4. Modified AC Electrical Characteristics section (p. 12). Removed "-5" bin. Added "-44" bin. All Bins Removed t_{KLCL} specifications -33 t_{AVKH}, t_{BVKH}, t_{DVKH} 0.4ns to 0.7ns t_{KHQV}, t_{KHQZ} 1.85ns to 1.8ns t_{KHCH}, t_{KHCZ} 1.65ns to 1.7ns t_{CHQV} 0.2ns to 0.4ns t_{CHQX} -0.2ns to -0.4ns t_{CHCL} $t_{KHKL} \pm 0.1$ to $t_{KHKL} \pm 0.2$ t_{CLCH} $t_{KLKH} \pm 0.1$ to $t_{KLKH} \pm 0.2$ -4 t_{AVKH}, t_{BVKH}, t_{DVKH} 0.5ns to 0.8ns t_{KHQV}, t_{KHQZ} 2.25ns to 2.1ns t_{CHQV} 0.2ns to 0.5ns t_{CHQX} -0.2ns to -0.5ns t_{CHCL} $t_{KHKL} \pm 0.1$ to $t_{KHKL} \pm 0.25$ t_{CLCH} $t_{KLKH} \pm 0.1$ to $t_{KLKH} \pm 0.25$ 5. Updated the size and content of the Boundary Scan Registers (p. 21).
rev 0.2	07/06/01	1. Modified DC Electrical Characteristics section (p. 11). Added I_{DD-33} and I_{DD-44} Average Power Supply Operating Current specifications. 2. Added Slow Down pin ($\overline{SD}$) and associated AC Electrical Characteristics section (p. 12). 3. Added 209 Pin BGA Package Dimensions (p. 26).
rev 0.3	02/22/02	1. Added BGA Package Thermal Characteristics (p. 10). 2. Removed Slow Down pin ($\overline{SD}$) and associated AC Electrical Characteristics section (p. 13). 3. Modified AC Electrical Characteristics section (p. 13). Removed "-44" bin. Added "-5" bin. -4 t_{CHCL} $t_{KHKL} \pm 0.25$ to $t_{KHKL} \pm 0.2$ t_{CLCH} $t_{KLKH} \pm 0.25$ to $t_{KLKH} \pm 0.2$ 4. Added JTAG ID Codes (p. 23). 5. Added JTAG Boundary Scan Register Bit Order Assignments (pp. 24-26).
rev 1.0	07/19/02	1. Modified Pin Assignment section (p. 2-4). Byte Write Enable Control Inputs $\overline{BWx}$ to $\overline{Bx}$ Pin 1K CQ to CQ2 Pin 2K $\overline{CQ}$ to $\overline{CQ2}$ Pin 10K $\overline{CQ}$ to $\overline{CQ1}$ Pin 11K CQ to CQ1 Pin 6J M4 to MCH Pin 6L M2 to MCH Pin 6M M3 to MCL

Rev. #	Rev. Date	Description of Modifications
		2. Modified I/O Capacitance section (p. 10).
		C_{KIN} 3.5pF to 4.0pF
		3. Modified DC Recommended Operating Conditions section (p. 11).
		Combined -1.8 and -1.5 line items into one for V_{DDQ}, V_{IH}, V_{IL}, V_{MIH}, and V_{MIL}.
		V_{IH} (min) 1.0V to $V_{DDQ}/2 + 0.3V$
		V_{IL} (max) 0.6V to $V_{DDQ}/2 - 0.3V$
		V_{MIH} (min) 1.1V to $V_{DDQ}/2 + 0.4V$
		V_{MIL} (max) 0.5V to $V_{DDQ}/2 - 0.4V$
		Removed notes 1 and 2.
		4. Modified DC Electrical Characteristics section (p. 12).
		Added MCH and MCL Input Leakage Current specifications.
		Reduced x72 Average Power Supply Operating Currents by 100mA.
		Reduced x36 Average Power Supply Operating Currents by 50mA.
		Reduced x18 Average Power Supply Operating Currents by 20mA.
		5. Modified AC Electrical Characteristics section (p. 13).
		-33 t_{KHCH} (max), t_{KHCZ} 1.7ns to 1.8ns
		-4 t_{KHCH} (max), t_{KHCZ} 2.0ns to 2.1ns
		-5 t_{KHCH} (max), t_{KHCZ} 2.2ns to 2.3ns
		6. Modified JTAG DC Recommended Operating Conditions section (p. 19).
		V_{TIH} (min) 1.2V to $V_{DD}/2 + 0.3V$
		V_{TIL} (max) 0.6V to $V_{DD}/2 - 0.3V$
		I_{TLI} (min) -10uA to -20uA
		7. Modified JTAG AC Electrical Characteristics section (p. 20).
		t_{THTH} 20ns to 50ns
		t_{THTL}, t_{TLTH} 8ns to 20ns
		Added t_{CS} Capture Setup and t_{CH} Capture Hold specifications.
		8. Modified TAP Registers section (p. 22).
		Instruction Register Codes 011, 110 Bypass to Private
		9. Modified Boundary Scan Register Bit Order Assignments section (p. 24-25).
		x72 Bit 47 10A to 11A
		x72 Bit 48 11A to 10A
		x36 Bit 29 10A to 11A
		x36 Bit 30 11A to 10A