STANDARD MICROSYSTEMS CORPORATION

COM82586
PRELIMINARY

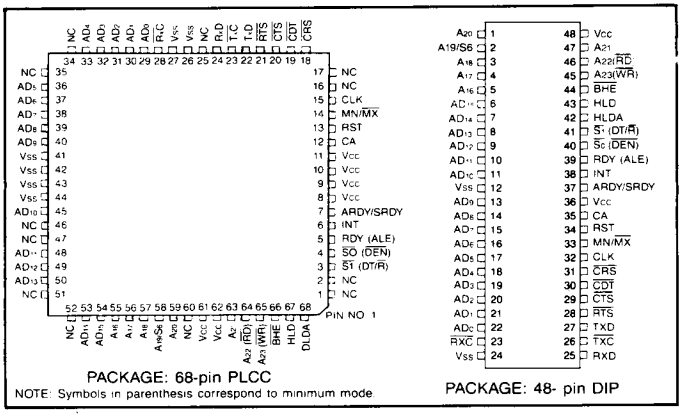
Ethernet™ Local Area Network Coprocessor

SECTION III

FEATURES

- ☐ Performs Complete CSMA/CD Medium Access Control Functions Independently of CPU
  - —High Level Command Interface
- ☐ Supports Established LAN Standards
  - —IEEE 802.3/Ethernet™ (10BASE5)
  - —IEEE 802.3/Cheapernet (10BASE2)
  - —IBM PC Network
  - —IEEE 802.3/StarLAN (1BASE5)
  - —Proprietary CSMA/CD Networks up to 10 Mbps
- ☐ On-Chip Memory Management
  - —Automatic Buffer Chaining
  - —Buffer Reclaim After Receipt of Bad Frames
  - —Save Bad Frames, Optionally
- ☐ Interfaces to 8-bit and 16-bit Microprocessors
- ☐ Supports Minimum Component Systems
  - —Shared Bus Configuration
  - —Interface to IAPX 186 and 188 Microprocessors without Glue
- ☐ Supports High Performance Systems
  - —Bus Master, with On-Chip DMA
  - —5 MBytes/Sec Bus Bandwidth
  - —Compatible with Dual Port Memory
  - —Back to Back Frame Reception at 10 Mbps
- ☐ 48 Pin DIP and 68 Pin PLCC

PIN CONFIGURATION



PACKAGE: 68-pin PLCC

NOTE: Symbols in parenthesis correspond to minimum mode.

PACKAGE: 48- pin DIP

- ☐ Network Management
  - —CRC Error Tally
  - —Alignment Error Tally
  - —Location of Cable Faults
- ☐ Self-Test Diagnostics
  - —Internal Loopback
  - —External Loopback
  - —Internal Register Dump
  - —Backoff Timer Check
- ☐ Single +5 volt supply
- ☐ Direct replacement for Intel's 82586

GENERAL DESCRIPTION

The COM82586 is an intelligent, high performance Local Area Network coprocessor, implementing the CSMA/CD access method (Carrier Sense Multiple Access with Collision Detection). It performs all time-crystal functions independently of the host processor, which maximizes performance and network efficiency.

The COM82586 performs the full set of IEEE 802.3 CSMA/CD media access control and channel interface functions including: framing, preamble generation and stripping, source address generation, destination address checking, CRC generation and checking, short frame detection. Any data rate up to 10 Mb/s can be used.

The COM82586 features a powerful host system interface. It automatically manages memory structures with command chaining and bidirectional data chaining. An on-chip DMA controller manages 4 channels transparently to the user. Buffers containing errored or collided frames can be automatically recovered. The 82586 can be configured for 8-bit or 16-bit data path, with maximum burst transfer rate of 2 or 4 Mbyte/sec. respectively. Memory address space is 16 Mbyte maximum.

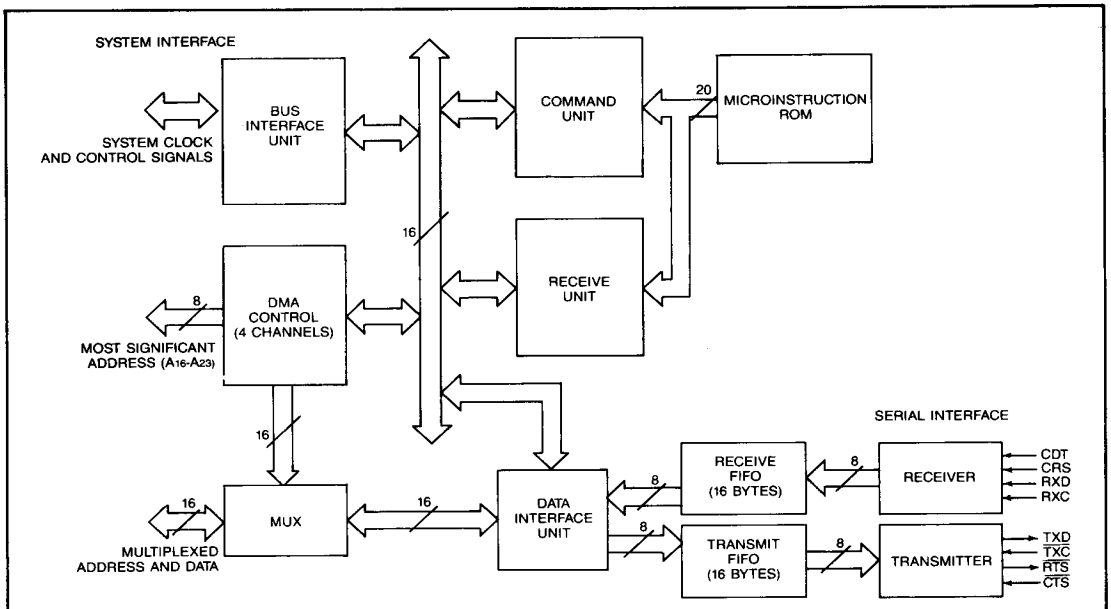
The COM82586 provides two independent 16 byte FIFOs, one for receiving and one for transmitting. The threshold for block transfer to/from memory is programmable, enabling the user to optimize bus overhead for a given worst case bus latency.

The COM82586 provides a rich set of diagnostic and network management functions including: internal and external loopbacks, exception condition tallies, channel activity indicators, optional capture of all frames regardless of destination address, optional capture of errored or collided frames, and time domain reflectometry for locating faults in the cable.

The COM82586 can be used in either baseband or broadband networks. It can be configured for maximum network efficiency (minimum contention overhead) for any length network operating at any data rate up to 10 Mb/s. The controller supports address field lengths of 1, 2, 3, 4, 5, or 6 bytes. It can be configured for either the IEEE 802.3/Ethernet™ or HDLC method of frame delineation. Both 16-bit and 32-bit CRC are supported.

The COM82586 is available in a 48 pin DIP or 68 pin PLCC package.

Ethernet™ is a trademark of the Xerox Corporation.



FUNCTIONAL BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

48 PIN DIP PIN NO.	68 PIN PLCC PIN NO.	NAME	SYMBOL	FUNCTION
48, 36	8, 9, 10, 11, 61, 62	Power Supply	V_{CC}, V_{CC}	+5V Power Supply.
12, 24	26, 27, 41, 42, 43, 44	Ground	V_{SS}, V_{SS}	System Ground.
34	13	Reset	RST	RST is an active HIGH internally synchronized signal, causing the 82586 to terminate present activity immediately. The signal must be HIGH for at least four clock cycles. The 82586 will execute RST within ten system clock cycles starting from RST HIGH. When RST returns LOW, the 82586 waits for the first CA to begin the initialization sequence.
27	22	Transmitted Serial Data	TxD	Output signal. This signal is HIGH when not transmitting.
26	23	Transmit Data Clock	$\overline{TxC}$	This signal provides timing information to the internal serial logic, depending upon the mode of data transfer. For NRZ mode of operation, data is transferred to the TxD pin on the HIGH to LOW clock transition.
25	24	Received Data	RxD	Received Data Input Signal.
23	28	Received Data Clock	$\overline{RxC}$	This signal provides timing information to the internal shifting logic depending upon the mode of data transfer. For NRZ data, the state of the RxD pin is sampled on the HIGH to LOW clock transition.
28	21	Request To Send	$\overline{RTS}$	When LOW, this signal notifies an external interface that the 82586 has data to transmit. It is forced HIGH after a Reset and while the Transmit Serial Unit is not sending data.
29	20	Clear To Send	$\overline{CTS}$	Active LOW Clear To Send input enables the 82586 transmitter to actually send data. It is normally used as an interface handshake to $\overline{RTS}$. This signal going inactive stops transmission. It is internally synchronized. If $\overline{CTS}$ goes inactive, meeting the setup time to $\overline{TxC}$ negative edge, transmission is stopped and $\overline{RTS}$ goes inactive within, at most, two TxC cycles.

48 PIN DIP PIN NO.	68 PIN PLCC PIN NO.	NAME	SYMBOL	FUNCTION
31	18	Carrier Sense	$\overline{CRS}$	Active LOW Carrier Sense input used to notify the 82586 that there is traffic on the serial link. It is used only if the 82586 is configured for external Carrier Sense. When so configured, external circuitry is required for detecting serial link traffic. It is internally synchronized. To be accepted, the signal must stay active for at least two serial clock cycles.
30	19	Collision Detect	$\overline{CDT}$	Active LOW Collision Detect input is used to notify the 82586 that a collision has occurred. It is used only if the 82586 is configured for external Collision Detect. External circuitry is required for detecting the collision. It is internally synchronized. To be accepted, the signal must stay active for at least two serial clock cycles. During transmission, the 82586 is able to recognize a collision one bit time after preamble transmission has begun.
38	6	Interrupt	INT	Active HIGH interrupt request signal.
32	15	Clock	CLK	The system clock input from the 80186 or another symmetric clock generator.
33	14	Minimum Mode/ Maximum Mode	MN/$\overline{MX}$	When HIGH, MN/$\overline{MX}$ selects $\overline{RD}$, $\overline{WR}$, ALE $\overline{DEN}$, DT/$\overline{R}$ (Minimum Mode). When LOW, MN/$\overline{MX}$ selects A22, A23, READY, $\overline{S0}$, $\overline{S1}$ (Maximum Mode). Note: This pin should be static during 82586 operation.
6-11, 13-22	29-33, 36-40, 45, 48, 49, 50, 53, 54	Address and Data Bus	AD0-AD15	These lines from the time multiplexed memory address (t1) and data (t2, t3, tW, 14) bus. When operating with an 8-bit bus, the high byte will output the address during the entire cycle. AD0-AD15 are floated after a RESET or when the bus is not acquired.
1, 3-5 45-47	55-57, 59, 63-65	Address Bus	A16-A18 A20-A23	These lines constitute 7 out of 8 most significant address bits for memory operation. They switch during t1 and stay valid during the entire memory cycle. The lines are floated after RST or when the bus is not acquired. Address lines A22 and A23 are not available for use in minimum mode.
2	58	Address 19 or Status 6	A19/S6	During t1 this signal it forms line 19 of the memory address. During t2 through t4 it is used as a status indicating that this is a Master peripheral cycle, and is HIGH. Its timing is identical to that of AD0-AD15 during write operation.
43	67	Hold	HLD	HLD is an active HIGH signal used by the 82586 to request local bus mastership at the end of the current CPU bus transfer cycle, or at the end of the current DMA burst transfer cycle. In normal operation, HLD goes inactive before HLDA. The 82586 can be forced off the bus by HLDA going inactive. In this case, HLD goes inactive within four clock cycles in word mode and eight clock cycles in byte mode.
42	68	Hold Acknowledge	HLDA	HLDA is an active HIGH Hold Acknowledge signal indicating that the CPU has received the HLD request and that bus control has been relinquished to the 82586. It is internally synchronized. After HLD is detected as LOW, the processor drives HLDA LOW. Note, CONNECTING V_{CC} TO HLDA IS NOT ALLOWED because it will cause a deadlock. Users wanting to give permanent bus access to the 82586 should connect HLDA with HLD.
35	12	Channel Attention	CA	The CA pin is a Channel Attention input used by the CPU to initiate the 82586 execution of memory resident Command Blocks. The CA signal is synchronized internally. The signal must be HIGH for at least one system clock period. It is latched internally on HIGH to LOW edge and then detected by the 82586.
44	66	Bus High Enable	$\overline{BHE}$	The Bus High Enable signal ($\overline{BHE}$) is used to enable data onto the most significant half of the data bus. Its timing is identical to that of A16-A23. With a 16-bit bus it is LOW and with an 8-bit bus it is HIGH. Note: after RST, the 82586 is configured to 8-bit bus.

48 PIN DIP PIN NO.	68 PIN PLCC PIN NO.	NAME	SYMBOL	FUNCTION
39	5	Ready	RDY	This active HIGH signal is the acknowledgement from the addressed memory that the transfer cycle can be completed. While LOW, it causes wait states to be inserted. This signal must be externally synchronized with the system clock. The Ready signal internal to the 82586 is a logical OR between RDY and SRDY/ARDY.
37	7	Synch/Asynch Ready	ARDY/ SRDY	This active HIGH signal performs the same function as RDY. If it is programmed at configure time to SRDY, it is identical to RDY. If it is programmed to ARDY, the positive edge of the Ready signal is internally synchronized. Note, the negative edge must still meet setup and hold time specifications, when in ARDY mode. The ARDY signal must be active for at least one system clock HIGH period for proper strobing. The Ready signal internal to the 82586 is a logical OR between RDY (in Maximum Mode only) and SRDY/ARDY. Note that following RST, this pin assumes ARDY mode.
40, 41	4, 3	Status 0, 1	$\overline{S0}$, $\overline{S1}$	Maximum mode only. These status pins define the type of DMA transfer during the current memory cycle. They are encoded as follows: $\overline{S1}$ $\overline{S0}$ 0 0 Not Used 0 1 Read Memory 1 0 Write Memory 1 1 Passive Status is active from the middle of t4 to the end of t2. They return to the passive state during t3 or during tW when RDY or ARDY is HIGH. These signals can be used by the 8288 Bus Controller to generate all memory control and timing signals. Any change from the passive state signals the 8288 to start the next t1 to t4 bus cycle. These pins are pulled HIGH and floated after a system RST and when the bus is not acquired.
46	64	Read	$\overline{RD}$	Used in minimum mode only. The read strobe indicates that the 82586 is performing a memory read cycle. $\overline{RD}$ is active LOW during t2, t3 and tW of any read cycle. This signal is pulled HIGH and floated after a RST and when the bus is not acquired.
45	65	Write	$\overline{WR}$	Used in minimum mode only. The write strobe indicates that the 82586 is performing a write memory cycle. $\overline{WR}$ is active LOW during t2, t3 and tW of any write cycle. It is pulled HIGH and floats after RST and when the bus is not acquired.
39	5	Address Latch Enable	ALE	Used in minimum mode only. Address Latch Enable is provided by the 82586 to latch the address into the 8282/8283 address latch. It is a HIGH pulse, during t1 ('clock low') of any bus cycle. Not that ALE is never floated.
40	4	Data Enable	$\overline{DEN}$	Used in minimum mode only. Data ENable is provided as output enable for the 8286/8287 transceivers in a stand-alone (no 8288) system. $\overline{DEN}$ is active LOW during each memory access. For a read cycle, it is active from the middle of t2 until the beginning of t4. For a write cycle, it is active from the beginning of t2 until the middle of t4. It is pulled HIGH and floats after a system RST or when the bus is not acquired.
41	3	Data I/O Control	DT/$\overline{R}$	Used in minimum mode only. DT/$\overline{R}$ is used in non-8288 systems using an 8286/8287 data bus transceiver. It controls the direction of data flow through the Transceiver. Logically, DT/$\overline{R}$ is equivalent to $\overline{S1}$. It becomes valid in the t4 preceding a bus cycle and remains valid until the final t4 of the cycle. This signal is pulled HIGH and floated after a RST or when the bus is not acquired.

NOTE: For an updated data sheet please fill out the reply card in the back of this catalog or call SMC at (516) 273-3100.