Universal Semiconductor

USH5801; USH5802

HIGH VOLTAGE OCTAL DRIVER

FEATURES

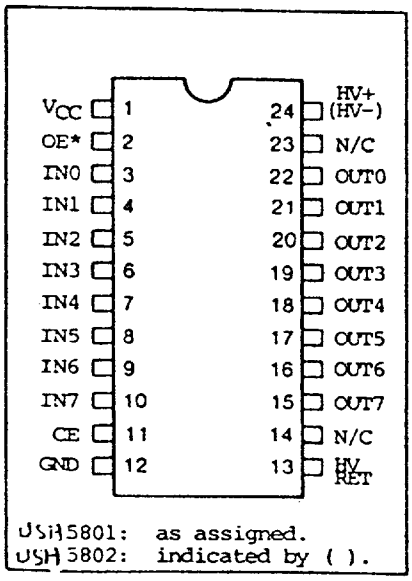
- 450V integrated drivers
- 170mA drive current
- Silicon-gate CMOS logic
- Internal level shifters
- Push-pull drivers
- Parallel input structure
- Microprocessor bus compatible
- TTL/CMOS compatible inputs

DESCRIPTION

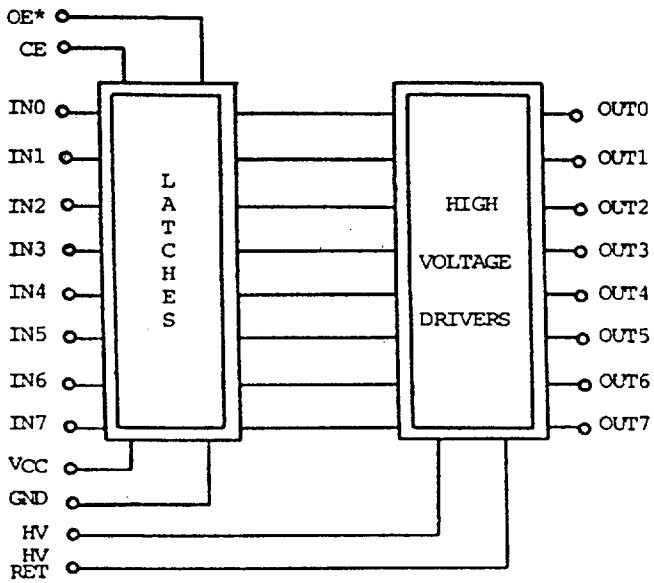
The USH5801 and USH5802 are High Voltage Integrated Circuits (HIVICs) designed for high voltage driver applications. The USH5801 is a +450V device, and the USH5802 is a -450V device. Both devices contain eight independent channels of high voltage push-pull drivers. Each channel has dielectrically isolated high voltage DMOS FET transistors.

The USH5801 and USH5802 incorporate CMOS logic to interface the HV drivers to a microprocessor bus. Both devices are configured as 8-bit parallel-in/parallel-out high voltage drivers and have internal level shifters that provide the interface between the CMOS logic and the high voltage drivers. The integration of high voltage with CMOS logic allows these HIVICs to be used in high voltage driver applications that are microprocessor controlled.

PIN CONFIGURATION



BLOCK DIAGRAM

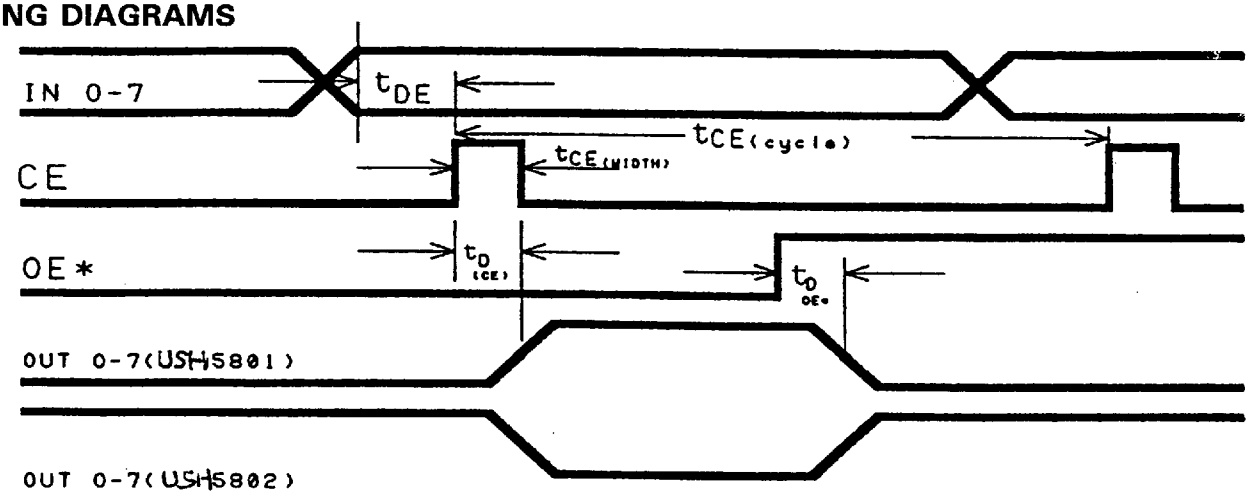


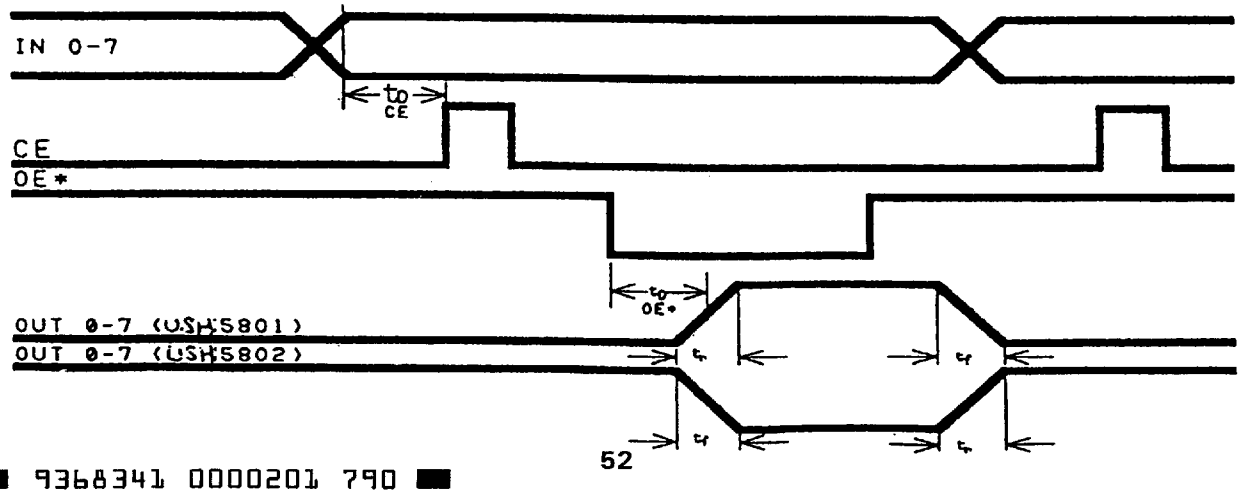
AC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, V_{CC} = 5.0V, HV = + 400V (USH5801), HV = - 400V (USH5802)

PARAMETER	SYMBOL	CONDITION	MIN	MAX	UNITS
Data setup	t_{DE}	Data to CE	10	—	ns
Clock pulse width	t_{CE}(width)	—	50	—	
Clock pulse cycle	t_{CE}(cycle)		200	—	
Delay after clock enable	t_D (CE)	CE to OUT (N)	—	200	
Output rise time	tr	C_L = 10 pf, Rseries = 2K ohms	—	500	
Output fall time	tf			500	
Delay after output enable	t_D	OE* to OUT (N)	—	200	
Clock enable to output enable delay	t_D (OE*)	CE to OE*	20	—	

TIMING DIAGRAMS





ABSOLUTE MAXIMUM RATINGS

LEVEL	PARAMETER	SYMBOL	RATING	UNITS
High Voltage	HV + (USH5801)	BV	+ 450	V
	HV - (USH5802)		- 450	V
	Continuous drain current	I_D	170	mA
CMOS Control	DC supply voltage	V_{CC}	-0.5 to +15	VDC
	DC supply voltage	I_{CC}	±20	mA
	Input voltage	V_{IN}	-0.5 to V_{CC} + 0.5	VDC
	DC input current	I_{IN}	± 10	mA
Packaged Device	Operating temperature	T_{OP}	0 to 70	°C
	Storage temperature	T_{ST}	-55 to 150	
	Power dissipation	P_D	2	W

DC ELECTRICAL CHARACTERISTICS (TA = 25°C, VCC = 5.0V)

PARAMETER	SYMBOL	CONDITION	MIN	MAX	UNITS
High voltage supply (USH5801)	HV +	OE* = 5V	0	400	V
(USH5802	HV-		-400	0	
High voltage output (USH5801)	V_{OUT} (N)	HV + = 400V, VIN = OV, OE* = OV, CE = 5V	—	400	
(USH5802)		HV - = - 400V, VIN = 5V, OE* = OV, CE = 5V	-400	-	
Current output	I_{OUT} (N)	V_{OUT} = + 400V, RSERIES = 2K Ω CSERIES = 100pf	-	170	mA
Logic power supply voltage	V_{CC}		4.5	5.5	V
Logic power supply current	I_{CC}		-	10	mA
Logic voltage in high	V_{IH}		2.4	-	V
Logic voltage in low	V_{IL}		-	0.8	
Drive on-resistance	R_D(ON)	I_{OUT} = 100mA, HV + = 400V, V_{IN} = OV, OE* = OV, CE = 5V	-	80	ohms
Sink on-resistance	R_S(ON)	V_{OUT} = IV, HV + = 400V, V_{IN} = 5V, OE* = OV, CE = 5V	-	100	

DESCRIPTION OF OPERATION

The USH5801 and USH5802 are high voltage integrated circuits (HIVICs) that contain eight independent high voltage drivers and the CMOS logic necessary to control them from a microprocessor bus. These HIVICs are designed to drive 400V into a capacitive load: the USH5801 drives positive 400V, and the USH5802 drives negative 400V.

The outputs (OUTO-7(are controlled by data on lines (INO-7), clock enable (CE) and output enable (OE*). See Tables 1 and 2. An inverted parallel load to INO-7, while CE is high, loads the internal latches. If OE* is low, data in the latches can enable the HV outputs (OUTO-7) during the load process. Alternatively, data can be held in the latches until after the load by keeping OE* high. When OE* is low, the contents of the latches will be transferred to the HV outputs. When OE* is high, the out-puts are disabled and return to ground level (OV).

TABLE 1. PIN DESCRIPTION

PIN	DESCRIPTION
INO-7	Inverted input to control the output of the selected channel.
OUTO-7	Output from high voltage drivers.
VCC	Logic power supply.
GND	Logic power supply ground.
HV + (USH5801)	High voltage power supply for positive driver.
HV - (USH5802)	High voltage power supply for negative driver.
HV RET	High voltage power supply ground for both positive and negative drivers.
CE	Clock enable to allow latches to receive data.
OE*	Output enable to allow data in latches to control the output status.
N/C	No connection.

TABLE 2. INPUT/OUTPUT STATUS

Output Enable (OE*)	Clock Enable (CE)	Input N (INO-7)	Output N TMH5801 (OUTO-7)	Output N TMH5802 (OUTO-7)
L	H	H	OV	HV -
L	H	L	HV +	OV
L	L	X	Qo	Qo
H	X	X	OV	OV

L = logic Low, H = logic high, X = don't care, Qo = previous state

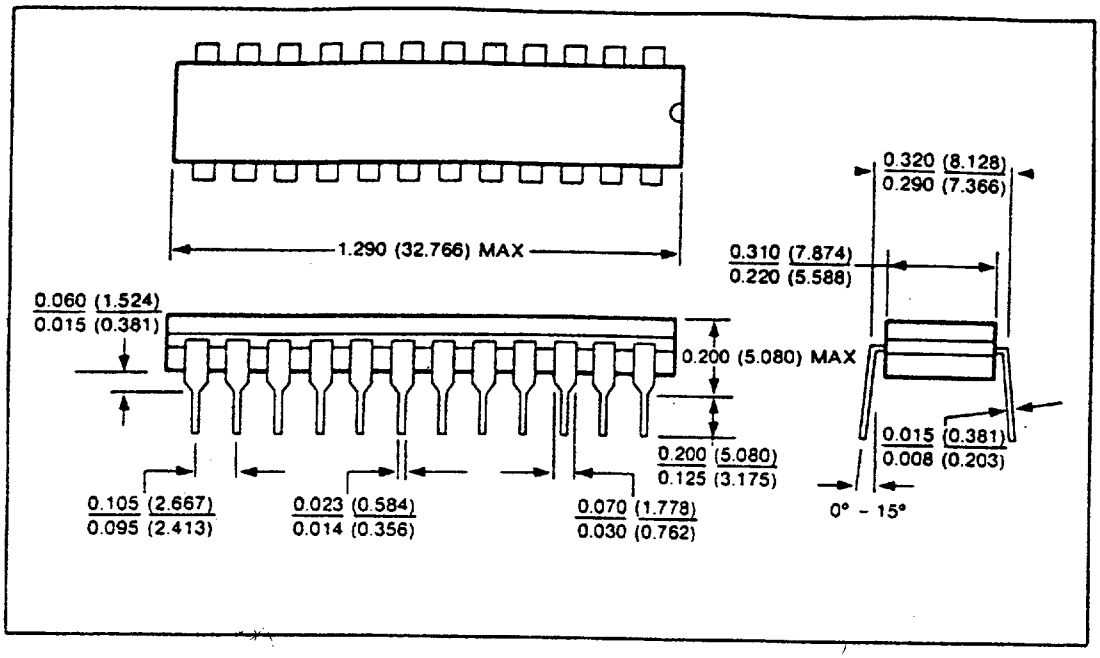
SPECIAL INFORMATION

Specifications are subject to change without notice.

Unless expressly agreed to in writing by an officer of USI, the products supplied by USI are not to be used in life support systems or in any medical application intended for the support of human life.

USI assumes no responsibility for the use of any circuits described and makes no representations that they are free from patent infringement.

PACKAGE INFORMATION



All dimensions in inches and (millimeters)

24 LEAD CERDIP

ORDERING INFORMATION

PRODUCT NO.	PACKAGE	TEMPERATURE RANGE
USH5801-AI-C24	24 pin cerdip	0 to 70°C
USH5802-AI-C24	24 pin cerdip	0 to 70°C