STL42N65M5

N-channel 650 V, 0.070 Ω, 34 A MDmesh™ V Power MOSFET in PowerFLAT™ (8x8) HV

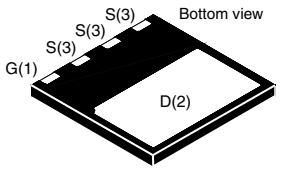
Preliminary data

Features

Type	V_{DSS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STL42N65M5	710 V	< 0.079 Ω	34 A(1)

1. The value is rated according to $R_{thj\text{-}case}$

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



PowerFLAT™(8x8) HV

Application

- Switching applications

Description

MDmesh V is a revolutionary Power MOSFET technology, which combines an innovative proprietary vertical process with the well known company's PowerMESH™ horizontal layout. The resulting product has an extremely low on-resistance, unmatched among silicon-based Power MOSFETs, making it especially suited for applications which require superior power density and outstanding efficiencies.

Figure 1. Internal schematic diagram

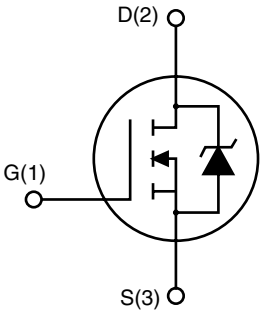


Table 1. Device summary

Order code	Marking	Package	Packaging
STL42N65M5	42N65M5	PowerFLAT™ (8x8) HV	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	650	V
V_{GS}	Gate-source voltage	± 25	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	34	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	22	A
I_{DM} (1),(2)	Drain current (pulsed)	136	A
I_D(3)	Drain current (continuous) at T_C = 25 °C	4	A
I_D(3)	Drain current (continuous) at T_C = 100 °C	2.5	A
I_{DM}(2),(3)	Drain current (pulsed)	16	A
P_{TOT} (3)	Total dissipation at T_C = 25 °C (steady state)	3	W
P_{TOT} (1)	Total dissipation at T_C = 25 °C (steady state)	208	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	11	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	950	mJ
dv/dt (4)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. The value is rated according to $R_{thj\text{-}case}$.
2. Pulse width limited by safe operating area.
3. When mounted on FR-4 board of inch², 2oz Cu.
4. $I_{SD} \leq 34$ A, di/dt $\leq$ 400 A/µs, $V_{Peak} < V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.6	°C/W
$R_{thj\text{-}amb}$(1)	Thermal resistance junction-ambient max	45	°C/W

1. When mounted on FR-4 board of inch², 2oz Cu.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	650			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 16.5 A		0.070	0.079	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	4650 110 5.7	-	pF pF pF
$C_{o(er)}$(1)	Equivalent output capacitance energy related	V_{GS} = 0, V_{DS} = 0 to 80% $V_{(BR)DSS}$	-	400	-	pF
$C_{o(tr)}$(2)	Equivalent output capacitance time related	V_{GS} = 0, V_{DS} = 0 to 80% $V_{(BR)DSS}$	-	285	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	1.4	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 520 V, I_D = 16.5 A, V_{GS} = 10 V (see *Figure 3*)	-	100 26 38	-	nC nC nC

1. $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}
2. $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_r t_c t_f	Turn-off delay time Rise time Cross time Fall time	V_{DD} = 400 V, I_D = 20 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 7*)	-	TBD TBD TBD TBD	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		34 136	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 33 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 33 A, di/dt = 100 A/µs V_{DD} = 100 V (see *Figure 4*)	-	400 7 35		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 33 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150 °C (see *Figure 4*)	-	532 10 38		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

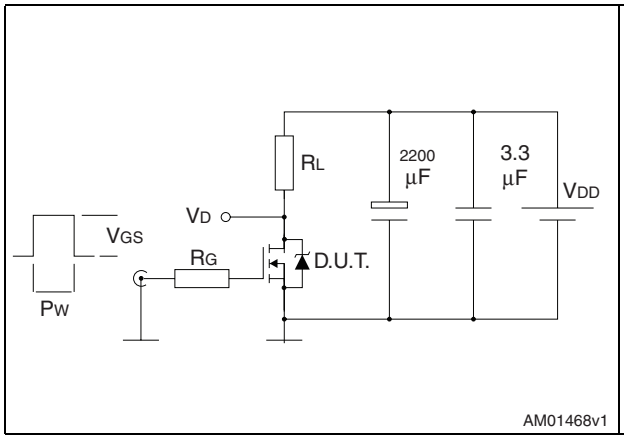


Figure 3. Gate charge test circuit

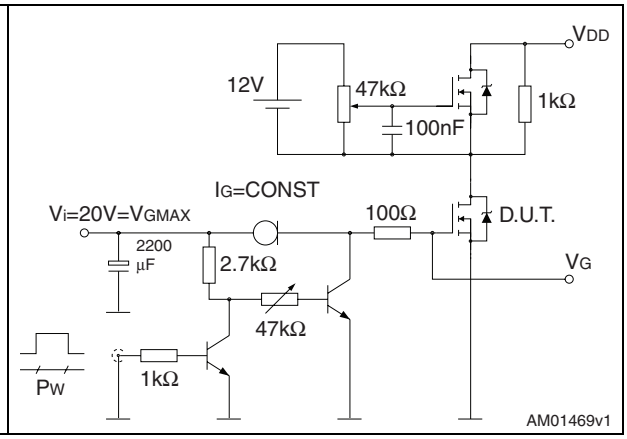


Figure 4. Test circuit for inductive load switching and diode recovery times

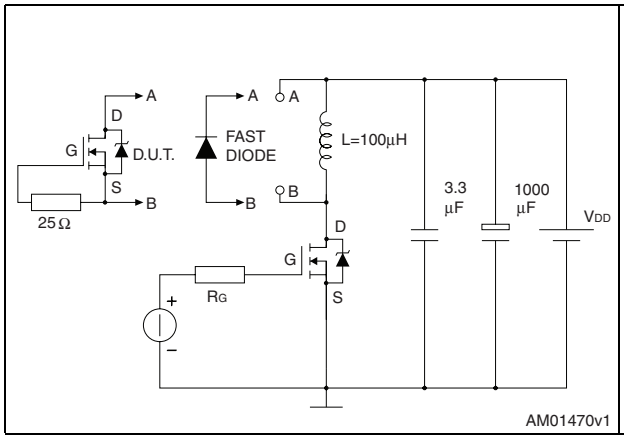


Figure 5. Unclamped inductive load test circuit

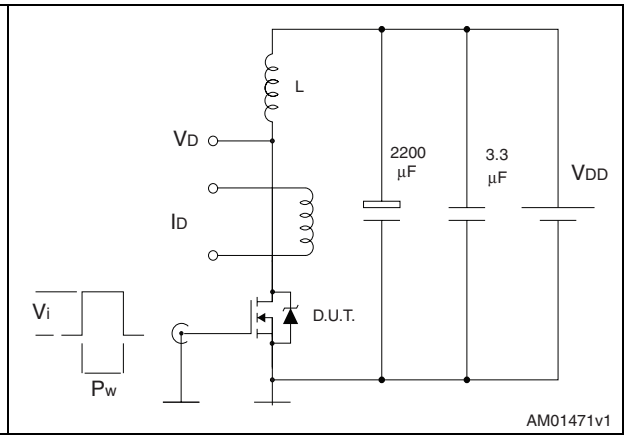


Figure 6. Unclamped inductive waveform

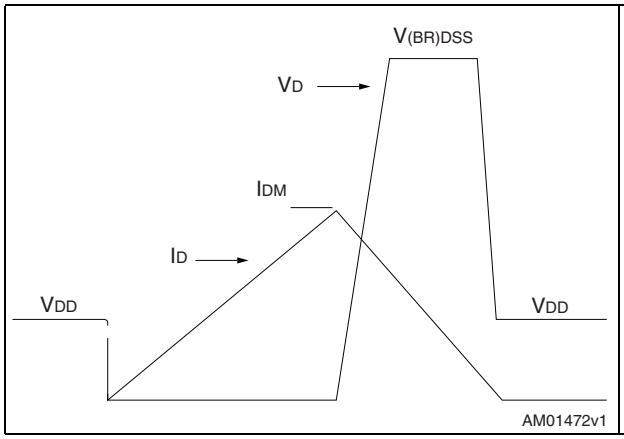
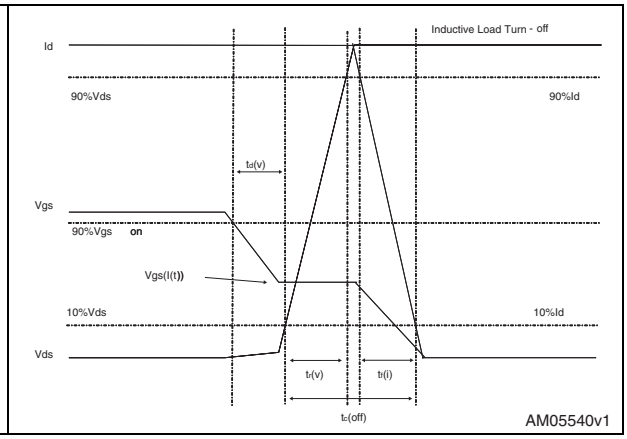


Figure 7. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1		0.02	0.05
b	0.95	1.00	1.05
c		0.10	
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60

Figure 8. PowerFLAT™ 8x8 HV drawing mechanical data

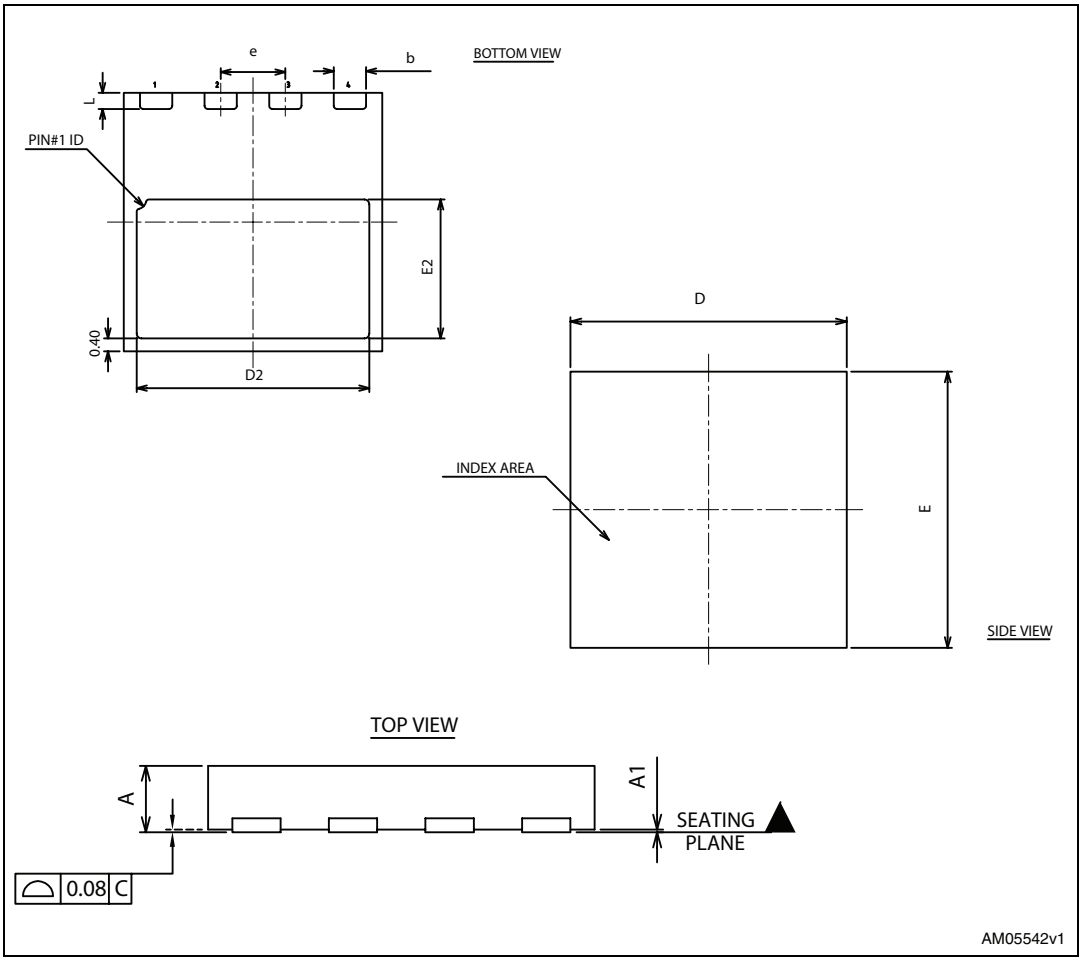
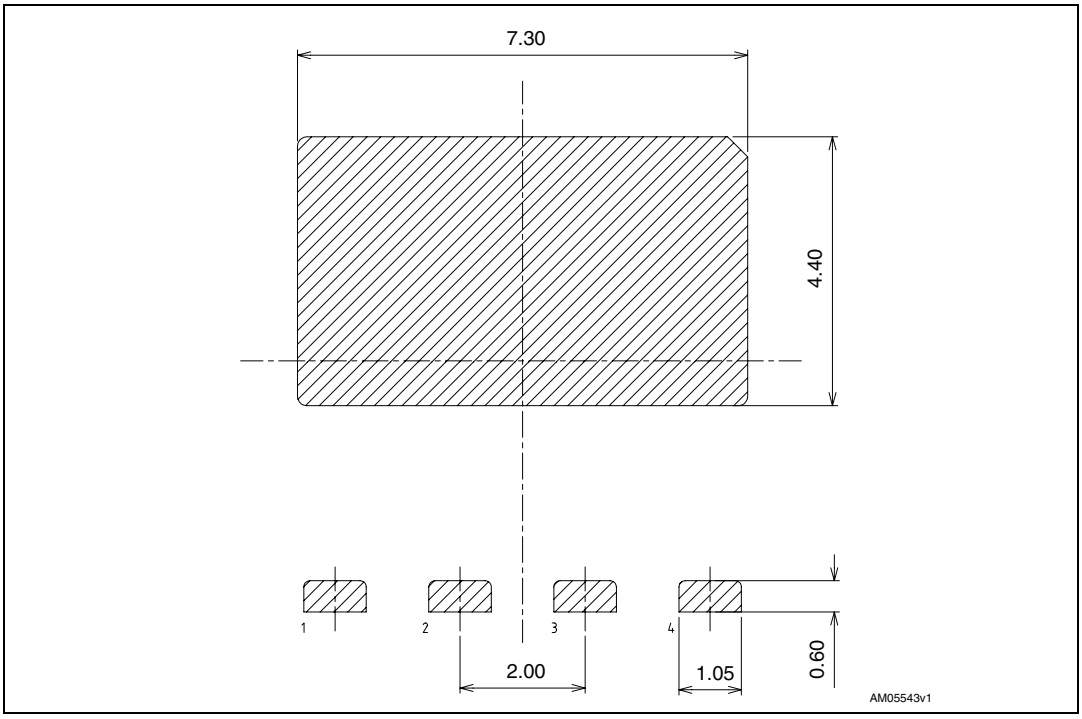


Figure 9. PowerFLAT™ 8x8 HV recommended footprint



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
28-Apr-2010	1	First release

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