



# N-Channel Synchronous MOSFETs With Break-Before-Make

## FEATURES

- 0- to 30-V Operation
- Under-Voltage Lockout
- Shoot Through Resistant
- Fast Switching Times
- SO-16 Package
- Driver Impedance—1 Ω
- 30-V MOSFETs
- High Side: 0.017 Ω @  $V_{DD} = 4.5\text{ V}$
- Low Side: 0.0082 Ω @  $V_{DD} = 4.5\text{ V}$
- Switching Frequency: 250 kHz to 1 MHz

## APPLICATIONS

- Power Supplies
  - Computer Auxillary-Notebook, Tablet, Desktop, Server
  - Point-Of-Load
  - Multiphase

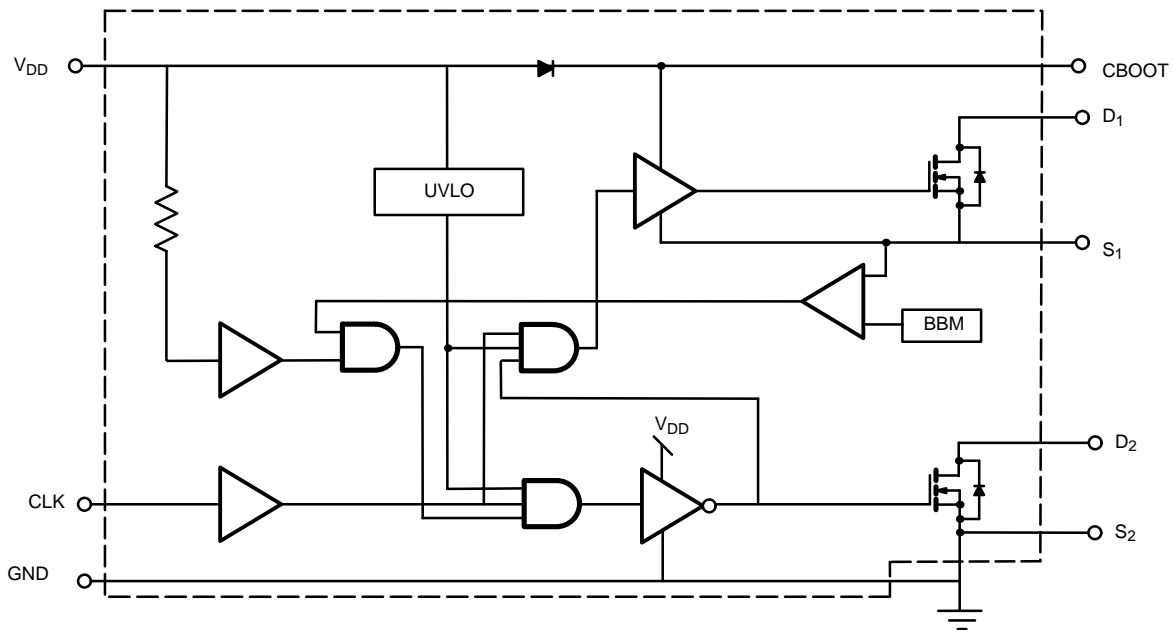
## DESCRIPTION

The Si4768CY n-channel synchronous MOSFET with break-before-make (BBM) is a high speed driver designed to operate in high frequency dc-dc switch-mode power supplies. Its purpose is to simplify the use of n-channel MOSFETs in high frequency buck regulators. This device is designed to be

used with any single output PWM IC or ASIC to produce a highly efficient, low cost, synchronous rectifier converter.

The LITTLE FOOT *Plus*™ Drivers Si4768DY is packaged in Vishay-Siliconix's high-performance SO-16 package.

## FUNCTIONAL BLOCK DIAGRAM



Order Number: Si4768CY (without tape and reel)  
Si4768CY-T1 (with tape and reel)

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Steady State	Unit
Logic Supply		$V_{DD}$	7	V
Logic Inputs		$V_{IN}$	-0.7 to $V_{DD} + 0.3$	
Drain Voltage		$V_{D1}$	30	
Bootstrap Voltage		$V_{BOOT}$	$V_{S1} + 7$	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$T_A = 25^\circ\text{C}$	$I_{D1}$	5.3	A
	$T_A = 70^\circ\text{C}$		4.25	
	$T_A = 25^\circ\text{C}$	$I_{D2}$	11	
	$T_A = 70^\circ\text{C}$		8.85	
Maximum Power Dissipation <sup>a</sup>		$P_D$	1.2	W
Operating Junction and Storage Temperature Range		Driver	-65 to 125	°C
		MOSFETs	-65 to 150	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS				
Parameter		Symbol	Steady State	Unit
Drain Voltage		$V_{D1}$	0 to 30	V
Logic Supply		$V_{DD}$	4.5 to 5.5	
Input Logic High Voltage		$V_{IH}$	$0.6 \times V_{DD}$ to $V_{DD}$	
Input Logic Low Voltage		$V_{IL}$	-0.3 to $0.3 \times V_{DD}$	
Bootstrap Capacitor		$C_{BOOT}$	100 n to 1 $\mu$	F
Ambient Temperature		$T_A$	-40 to 85	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
High-Side Junction-to-Ambient <sup>a</sup>	Steady State	$R_{thJA1}$	85	105	°C/W
Low-Side Junction-to-Ambient <sup>a</sup>		$R_{thJA2}$	68	85	
High-Side Junction-to-Foot (Drain) <sup>b</sup>		$R_{thJF1}$	26	33	
Low-Side Junction-to-Foot (Drain) <sup>b</sup>		$R_{thJF2}$	16	20	

## Notes

- Surface mounted on 1" x 1" FR4 board, 0.062" thick, 2-oz copper double sided.
- Junction-to-foot thermal impedance represents the effective thermal impedance of all heat carrying leads in parallel and is intended for use in conjunction with the thermal impedance of the PC board pads to ambient ( $R_{thJA} = R_{thJF} + R_{thPCB-A}$ ). It can also be used to estimate chip temperature if power dissipation and the lead temperature of a heat carrying (drain) lead is known.

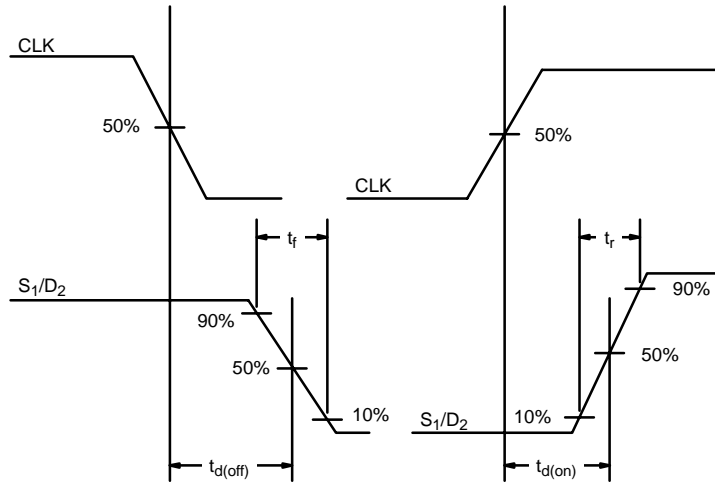


SPECIFICATIONS						
Parameter	Symbol	Test Conditions Unless Specified $T_A = 25^\circ\text{C}$ $4.5\text{ V} < V_{DD} < 5.5\text{ V}, 4.5\text{ V} < V_{D1} < 30\text{ V}$	Limits			Unit
			Min	Typ <sup>a</sup>	Max	
<b>Power Supplies</b>						
Logic Voltage	$V_{DD}$		4.5		5.5	V
Logic Current (Static)	$I_{DD(EN)}$	$V_{DD} = 4.5\text{ V}, V_{CLK}, SYNC = 4.5\text{ V}$		1	3	mA
	$I_{DD(DIS)}$	$V_{DD} = 4.5\text{ V}, V_{CLK}, SYNC = 0\text{ V}$		1	3	
Logic Current (Dynamic)	$I_{DD1(DYN)}$	$V_{DD} = 5\text{ V}, f_{clk} = 250\text{ kHz}$ (See Apps Board)		21	40	
	$I_{DD2(DYN)}$	$V_{DD} = 5\text{ V}, f_{clk} = 1\text{ MHz}$ (See Apps Board)		72	150	
<b>Logic Input</b>						
Logic Input Voltage—High ( $V_{CLK}$ )	$V_{HIGH}$	$V_{DD} = 4.5\text{ V}$	2.7	2.3		V
Logic Input Voltage—Low ( $V_{CLK}$ )	$V_{LOW}$		-0.3	2.25	0.8	
<b>Protection</b>						
Break-Before-Make Reference	$V_{BBM}$	$V_{DD} = 5.5\text{ V}$		2.4		V
Under-Voltage Lockout	$V_{UVLO}$	$V_{DD} = 4.5\text{ V}$	3.5	4	4.25	
Under-Voltage Lockout Hysteresis	$V_H$				0.4	
<b>MOSFETs</b>						
Drain-Source Voltage	$V_{DS}$	$I_D = 250\ \mu\text{A}$	30			V
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)1}$	$V_{DD} = 4.5\text{ V}, I_D = 10\text{ A}$ $T_A = 25^\circ\text{C}$	Q1	13.5	17	m $\Omega$
	$r_{DS(on)2}$		Q2	6.5	8.2	
Diode Forward Voltage <sup>a</sup>	$V_{SD1}$	$I_S = 2\text{ A}, V_{GS} = 0\text{ V}$	Q1	0.7	1.1	V
	$V_{SD2}$		Q2	0.7	1.1	
<b>Dynamic<sup>b</sup></b>						
Driver CLK to S1/D2 Off Delay	$t_{d(off)}$	$f_s = 1\text{ MHz}, I_D = 10\text{ A}$ $V_{IN} = 12\text{ V}, V_{OUT} = 1.6\text{ V}$ (See Single Package Apps Board)		24	50	ns
Driver CLK to S1/D2 Fall Time	$t_f$			4	10	
Driver CLK to S1/D2 On Delay	$t_{d(on)}$			73	150	
Driver CLK to S1/D2 Rise Time	$t_r$			24	50	
Source-Drain Reverse Recovery Time—Q <sub>2</sub>	$t_{rr}$	$I_F 2.7\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		50	80	

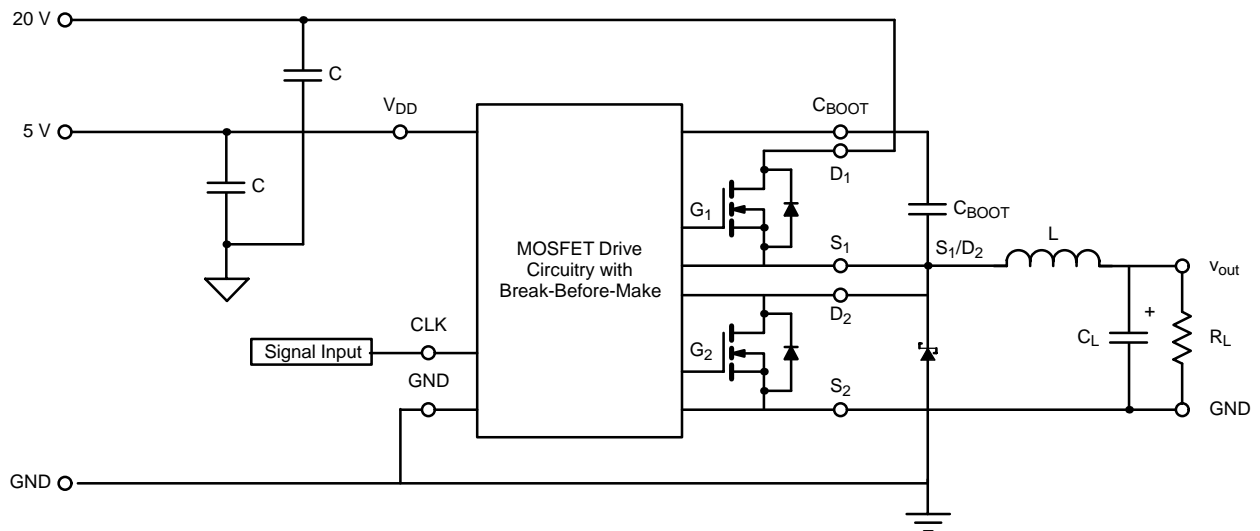
Notes  
a. Pulse test: pulse width  $\leq 300\text{ ms}$ , duty cycle  $\leq 2\%$ .  
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.



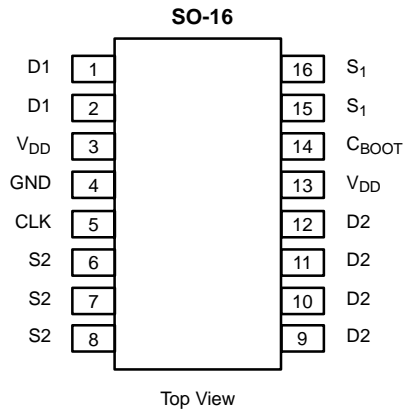
**TIMING DIAGRAMS**



**SWITCHING TEST SET-UP**



**PIN CONFIGURATION**



TRUTH TABLE		
CLK	Q <sub>1</sub>	Q <sub>2</sub>
H	ON	OFF
L	OFF	ON

PIN DESCRIPTION		
Pin	Symbol	Description
1, 2	D <sub>1</sub>	High-Side MOSFET Drain
3, 13	V <sub>DD</sub>	Logic Supply; Decoupling to GND (with a Cap is strongly recommended)
4	GND	Signal Ground
5	CLK	Input Logic Signal
6, 7, 8	S <sub>2</sub>	Low-Side MOSFET Source
9, 10, 11, 12	D <sub>2</sub>	Low-Side MOSFET Drain
14	C <sub>BOOT</sub>	Bootstrap Capacitor for Upper MOSFET
15, 16	S <sub>1</sub>	High-Side MOSFET Source

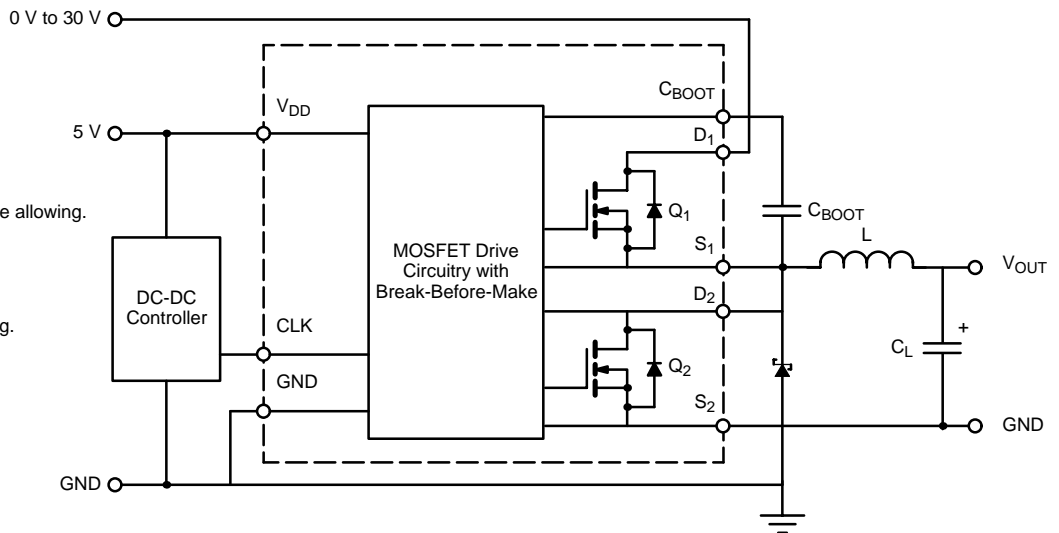
**APPLICATION CIRCUIT**

**Power Up Sequence:**

- 1 Ensure V<sub>DD</sub> is within spec before allowing.
- 2 CLK to be set high.

**Power Down Sequence:**

- 1 Ensure CLK is low before turning.
- 2 Turn V<sub>DD</sub> off.



## DEVICE OPERATION

The Vishay Siliconix MOSFET plus driver product is optimized for dc-dc conversion in all aspects—driver design through MOSFET optimization. The integrated packaged allows the PCB designer to ignore the MOSFET driving current loops and focus on one board layout aspect—output current loop. It also allows for simplicity when adding additional phases to a system.

The MOSFET driver is designed to eliminate any shoot-through currents in the output MOSFET stage by integrating a break-before-make circuit topology. When the low-side MOSFET is to be turned on, there is an internal reference voltage,  $V_{BBM}$ , that the  $S_1$  node needs to be below before the low-side MOSFET is turned on. When the high-side MOSFET is to be turned on, there is an optimized delay time (based on the MOSFET pair used) that will ensure that the low-side is turned off, and minimize the body diode conduction. In addition, the low impedance MOSFET drivers are optimized with the MOSFET gate impedance to help ensure an “off” state gate voltage during any shoot-through conditions when the high-side MOSFET is turned on.

The MOSFETs are designed to meet a specific set of conditions to provide the best performance possible. These requirements are as follows.

1. The size of the MOSFET is selected to provide a good compromise between power dissipation and size.
2. The high-side MOSFET is designed to minimize the  $r_{DS(on)} \cdot Q_g$  figure-of-merit and to have a low  $R_g$  for short switching times.
3. The low-side MOSFET is designed to have the optimum  $r_{DS(on)}$ , low  $R_g$  for short switching times, and low  $Q_{gd}/Q_{gs}$  ratio to eliminate shoot-through conditions.

## Switch Timing

The Si4768CY has a built-in delay time that is optimized for the MOSFET pair. When the CLK signal goes low, the high-side driver will turn off, and the output will start to ramp down,  $t_f$ . After a total delay,  $t_{d(off)}$ , the low-side driver turns on to provide the synchronous rectification.

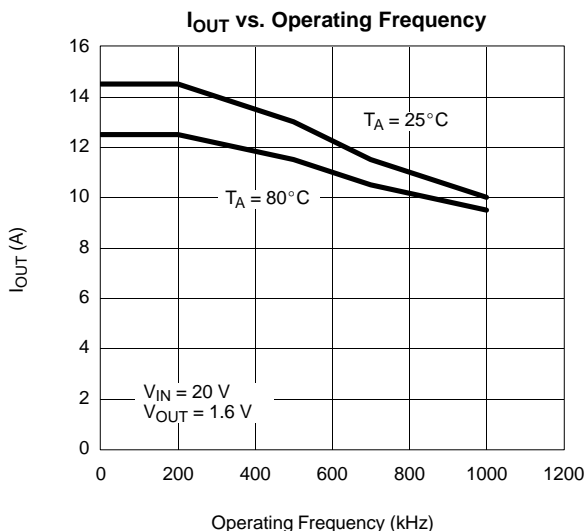
When the CLK goes high, the low-side driver turns off; as the body diode starts to conduct, the high-side MOSFET turns on after a total delay,  $t_{d(on)}$ . The output then ramps up,  $t_r$ .

## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

### Representative Safe Operating Curve

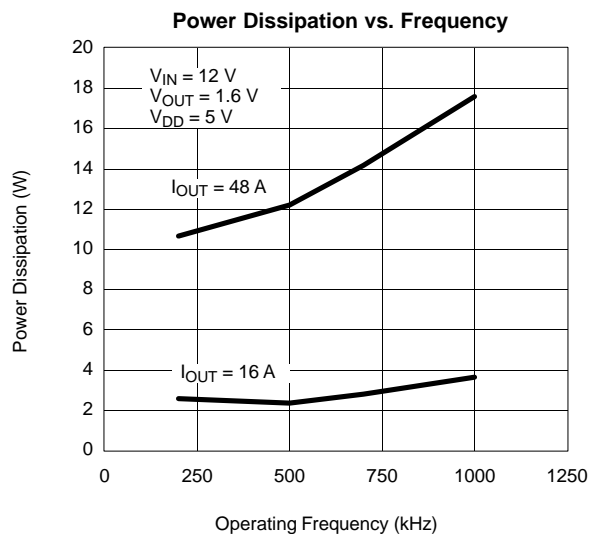
The following guidelines are meant to allow the designer the quickest and simplest method to working with the Vishay Siliconix MOSFET plus driver products.

1. The Si4768CY has a limited maximum output current capability, depending on the frequency, duty cycle and ambient temperature. The following graph shows the limitation

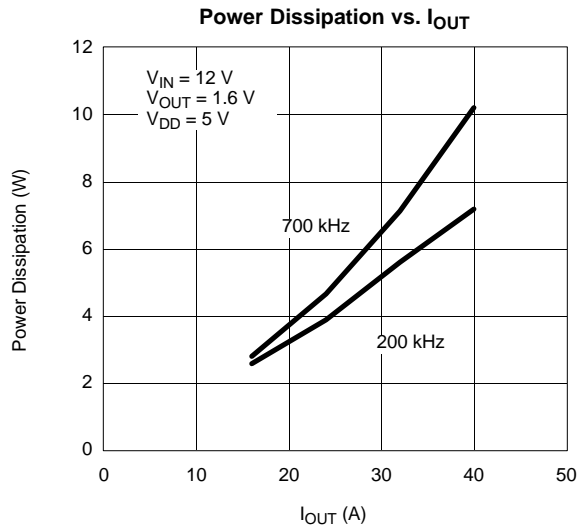


### Typical Performance

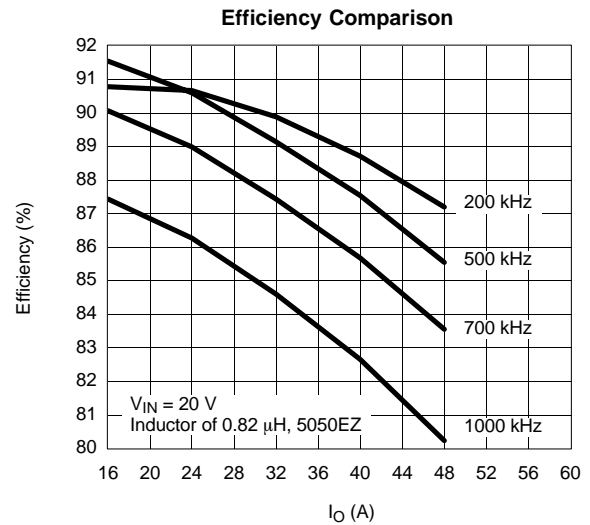
2. The following chart shows experimental results based on a specific set of operating conditions.



**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**



When all of these factors are put together, a set of efficiency curves are developed as shown. This experimental result is based on a spreading copper area on the board of one and a half square inches.



- The dissipation of the heat generated by the MOSFET plus driver product is highly dependent on the board thermal impedance and the  $R_{thJF}$  of the SO-16 package.

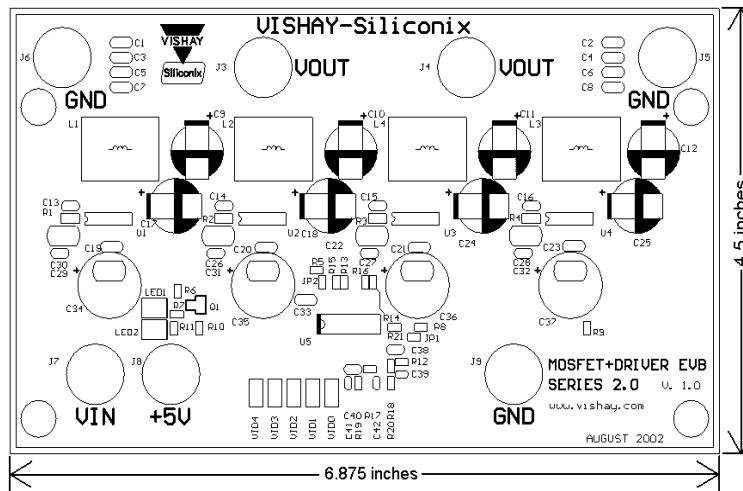
**BOARD DESIGN GUIDELINES**

The performance characteristics shown above was done using a board that follows a suggested layout of the device and surrounding components. The basic design rules are as follows.

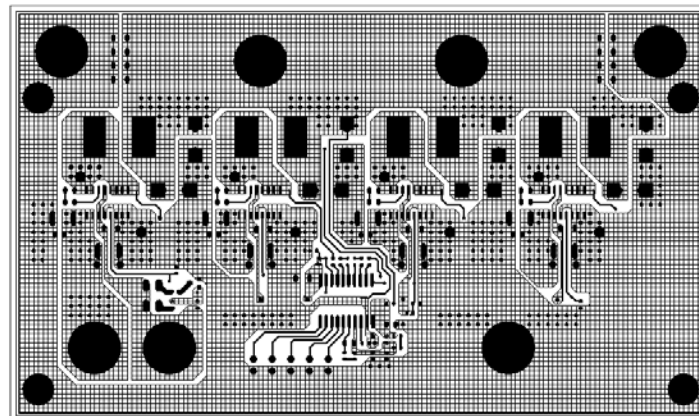
- Minimize the distance of the  $V_{DD}$  capacitor to the  $V_{DD}$  pins and ground.
- Place the output inductor close to the  $S_1$  and  $D_2$  pads. Using a large copper area around these pads help improve the thermal performance. Adding thermal vias to help dissipate the heat also improves performance.
- Use a large copper area for the  $D_1$  and  $S_2$  pads. Again, using thermal vias in this area will help the thermal performance.



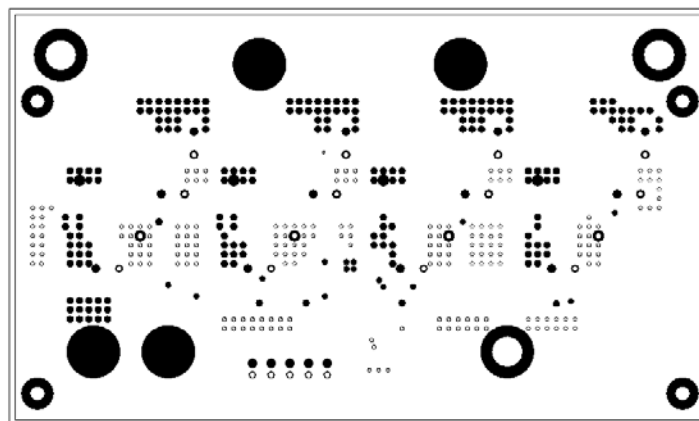
**BOARD LAYOUT**



Top Layer Overlay



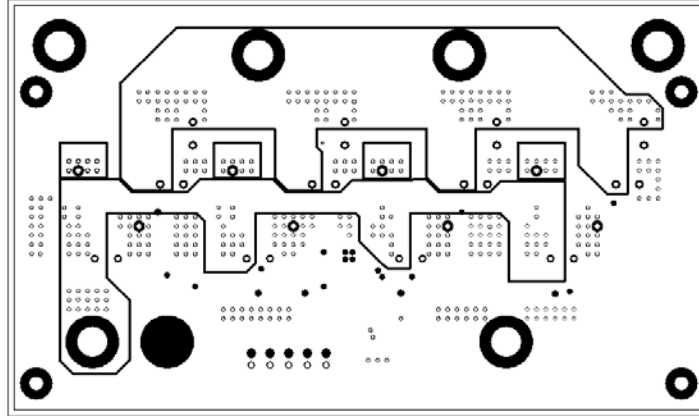
Top Layer



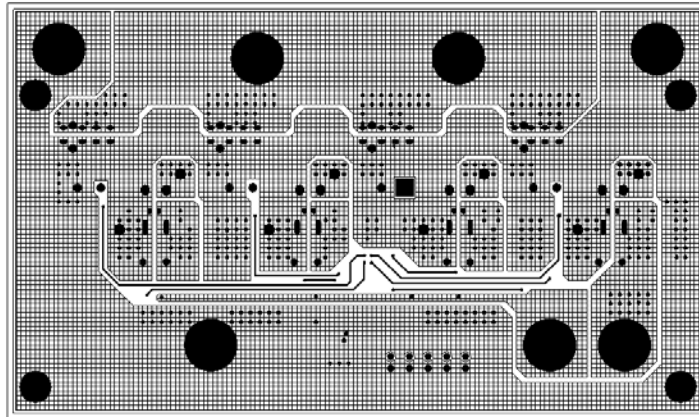
Internal Ground Layer



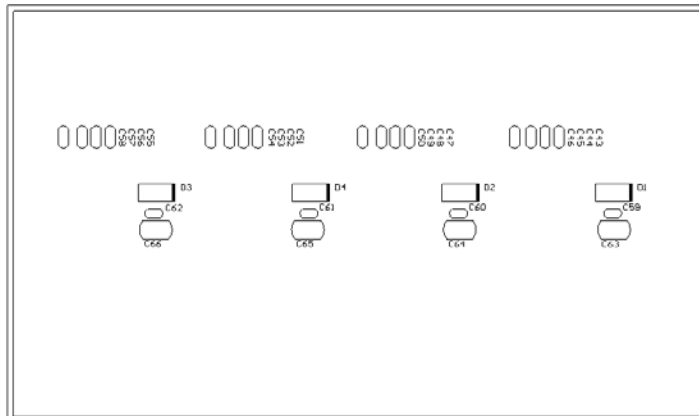
**BOARD LAYOUT**



Internal Power Layer



Bottom Layer



Bottom Layer Overlay