MIC2358YLQ

IEEE 802.3af Octal Power Sourcing Equipment Controller

General Description

The MIC2358YLQYLQ octal network power controller is designed for use in IEEE 802.3af-compliant power-sourcing equipment (PSE). The device provides standardized powered devices (PD) detection, classification, current-limit, and monitoring of both DC and AC maintain power signatures.

The MIC2358YLQYLQ can operate autonomously or be controlled by software through a SMBus-compatible interface. Its five address inputs support 32 unique MIC2358YLQ addresses allowing control and monitoring up to 256 powered Ethernet ports (32 MIC2358YLQ devices) by an external management application.

For each port, the MIC2358YLQ uses external N-Channel power FETs and current sense resistors to deliver and monitor power. State machines have been incorporated into this device for complete configuration, fault reporting, and status on a per-port basis, including port voltage and current.

The MIC2358YLQ also implements Micrel's shared power management and port prioritization which offers more flexible allocation of available power among the ports.

Throughout this document the term 802.3af is synonymous for IEEE Std 802.3-2005.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Features

- Fully compliant with the IEEE 802.3af Power-over-Ethernet standard
- Controls eight independent 48V-powered Ethernet ports
- Powered port attributes:
  - Up to 15.4W delivered per port
  - Input over-voltage protection (OVP)
  - Powered Device detection and classification
  - Active current limit
  - Powered Device AC and DC disconnect supported
- Operates autonomously or by SMBus control
- 5-bit programmable digital addressing allows control of up to 256 Ethernet powered ports
- Hardware fault interrupt output
- Available in a Pb-free 64-pin LQFP package

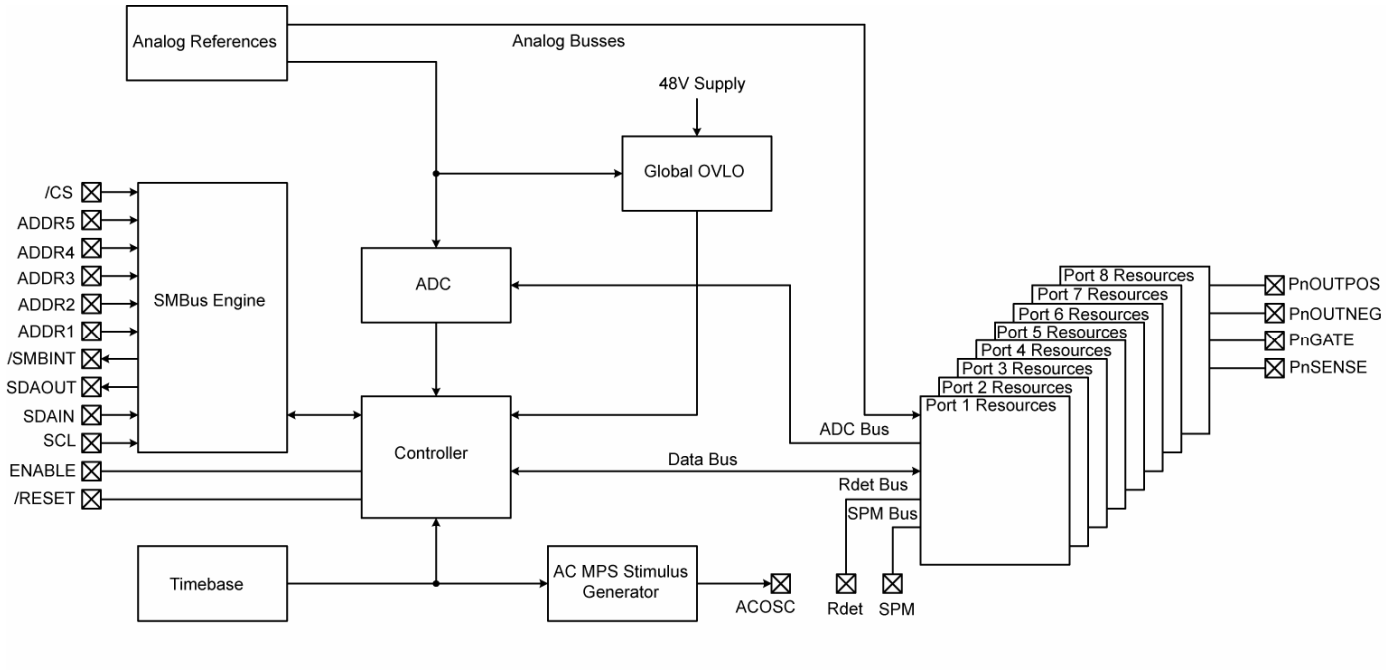
Applications

- IEEE 802.3af Compliant Enterprise Switches/Hubs
- IEEE 802.3af Compliant Endpoint and Midspan Power Sources
- PSE Power Injectors
- IP Phone Systems
- DTE Power Distribution

Ordering Information

Part Number	Temperature Range	Pb-Free Package
MIC2358YLQYLQ	0 °C to +70 °C	64-Pin LQFP

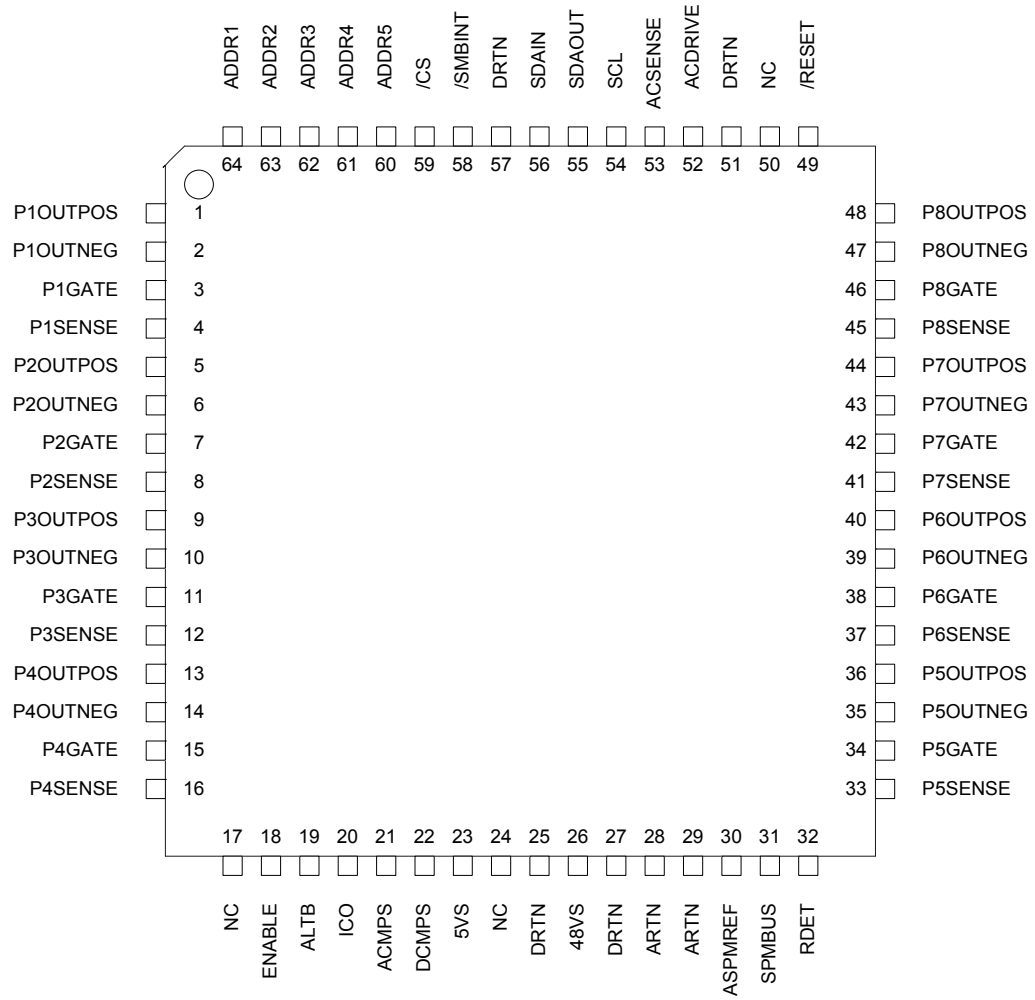
Functional Block Diagram – Global Level



Revision History

Rev.	Date	Reason
1.0	12/08/09	Initial Created
1.1	05/03/10	Autonomous enable is low true max current (5V) is 40mA

Pin Configuration



64-Pin LQFP (V)

Pin Description

Pin Number	Pin Name	Pin Function
1	P1OUTPOS	Port 1 Positive 48V Terminal Input.
2	P1OUTNEG	Port 1 Negative 48V Terminal Input.
3	P1GATE	Port 1 Gate Drive Output: Connect this pin to the gate terminal of Port 1's external power FET.
4	P1SENSE	Port 1 Sense Input: Connect this pin the source terminal of Port 1's external power FET.
5	P2OUTPOS	Port 2 Positive 48V Terminal Input.
6	P2OUTNEG	Port 2 Negative 48V Terminal Input.
7	P2GATE	Port 2 Gate Drive Output: Connect this pin to the gate terminal of Port 2's external power FET.
8	P2SENSE	Port 2 Sense Input: Connect this pin the source terminal of Port 2's external power FET.
9	P3OUTPOS	Port 3 Positive 48V Terminal Input.
10	P3OUTNEG	Port 3 Negative 48V Terminal Input.
11	P3GATE	Port 3 Gate Drive Output: Connect this pin to the gate terminal of Port 3's external power FET.
12	P3SENSE	Port 3 Sense Input: Connect this pin the source terminal of Port 3's external power FET.
13	P4OUTPOS	Port 4 Positive 48V Terminal Input.
14	P4OUTNEG	Port 4 Negative 48V Terminal Input.
15	P4GATE	Port 4 Gate Drive Output: Connect this pin to the gate terminal of Port 4's external power FET.
16	P4SENSE	Port 4 Sense Input: Connect this pin the source terminal of Port 4's external power FET.
17	NC	No connection.
18	ENABLE_L	Autonomous mode select pin Input. When high, all ports are disabled on power up and can only be enabled via SMBus interaction. When low, all ports are enabled on power up and device operation will proceed without SMBus interaction necessary. Internally pulled up to +5V by a 50kΩ resistor.
19	ALTB	Autonomous mode select pin Input. When high all ports will be configured for Alt B operation, when low all ports will be configured for Alt A operation. Internally pulled up to +5V by a 50kΩ resistor.
20	ICO	Autonomous mode select pin Input. When high, ports will not have power removed if its current exceeds the class-dependent overload current, i.e. overload current will be equal to Class 0 Level. Internally pulled up to +5V by a 50kΩ resistor.
21	ACMPS	Autonomous mode select pin Input. When high, AC Maintain Power Signature feature is enabled. Internally pulled up to +5V by a 50kΩ resistor.
22	DCMPS	Autonomous mode select pin Input. When high, DC Maintain Power Signature feature is enabled. Internally pulled up to +5V by a 50kΩ resistor.
23	5VS	+5V Supply Voltage: Applying a +5V supply relative to 48VRTN powers the MIC2358YLQ's internal digital circuits, state machines, and port control circuits.
24	NC	No connection.
25	DRTN	Digital Ground Return.
26	48VS	48V Power Supply Input: In a negative common application, applying a conditioned +48V supply (+44V ≤ 48VS ≤ +60V) provides the supply voltage to power the MIC2358YLQ and all eight ports. In a positive common application, apply system COM to this pin.
27	DRTN	Digital Ground Return.
28	ARTN	Analog Ground Return.
29	ARTN	Analog Ground Return.

Pin Number	Pin Name	Pin Function
30	SPMREF	Shared Power Management Reference Resistor. Connect an external 250kΩ, 1% resistor from this pin-to-ARTN.
31	SPMBUS	Shared Power Management Buss. A resistor connected from this pin to ARTN sets the total power allocated to all ports in use. For all eight ports, the total maximum allocated power is 123.2W (15.4W x 8 ports). The transfer characteristic for this pin is 2.5V/R_{SPMREF} per Watt. Thus, the resistor value is determined by R_{SPMREF}/P_{TOTAL}.
32	RDET	PD Signature Detection Resistor. Connect a 1kΩ 1% resistor from this pin to ARTN.
33	P5SENSE	Port 5 Sense Input: Connect this pin the source terminal of Port 5's external power FET.
34	P5GATE	Port 5 Gate Drive Output: Connect this pin to the gate terminal of Port 5's external power FET.
35	P5OUTNEG	Port 5 Negative 48V Terminal Input.
36	P5OUTPOS	Port 5 Positive 48V Terminal Input.
37	P6SENSE	Port 6 Sense Input: Connect this pin the source terminal of Port 6's external power FET.
38	P6GATE	Port 6 Gate Drive Output: Connect this pin to the gate terminal of Port 6's external power FET.
39	P6OUTNEG	Port 6 Negative 48V Terminal Input.
40	P6OUTPOS	Port 6 Positive 48V Terminal Input.
41	P7SENSE	Port 7 Sense Input: Connect this pin the source terminal of Port 7's external power FET.
42	P7GATE	Port 7 Gate Drive Output: Connect this pin to the gate terminal of Port 7's external power FET.
43	P7OUTNEG	Port 7 Negative 48V Terminal Input.
44	P7OUTPOS	Port 7 Positive 48V Terminal Input.
45	P8SENSE	Port 8 Sense Input: Connect this pin the source terminal of Port 8's external power FET.
46	P8GATE	Port 8 Gate Drive Output: Connect this pin to the gate terminal of Port 8's external power FET.
47	P8OUTNEG	Port 8 Negative 48V Terminal Input.
48	P8OUTPOS	Port 8 Positive 48V Terminal Input.
49	/RESET	Reset Input: This active LOW asserted digital input is used to reset the MIC2358YLQ to default settings. There is an internal 50kΩ resistor connected from this pin to 5VS.
50	NC	Do not connect.
51	DRTN	Digital Ground. Connect this pin to all other MIC2358YLQ DRTN pins at one point.
52	ACDRIVE	Internal AC Oscillator output. Accessible from this pin is the MIC2358YLQ's internal oscillation specifically required to support AC Disconnect. An 83Hz square wave with 50% is available.
53	ACSENSE	Senses the AC Drive forced on positive port terminals. Connect to V48 through 800Ω and diode even if AC disconnect is not used. Please see reference schematic.
54	SCL	SMBus Serial Clock Input. External pull up resistor required.
55	SDAOUT	SMBus Serial Data Output.
56	SDAIN	SMBus Serial Data Input. External pull up resistor required.
57	DRTN	Digital Ground. Connect this pin to all other MIC2358YLQ DRTN pins at one point.
58	/SMBINT	SMBus Interrupt open-drain output. External pull up resistor required.
59	/CS	Address Chip Select Input. This bit is internally pulled up to +5V by a 50kΩ resistor.
60	ADDR5	SMBus Address Bit 5 (MSB): This address bit is the most significant bit of the MIC2358YLQ's 5-bit address bank. This bit is internally pulled up to +5V by a 50kΩ resistor.
61	ADDR4	SMBus Address Bit 4: This bit is internally pulled up to +5V by a 50kΩ resistor.
62	ADDR3	SMBus Address Bit 3: This bit is internally pulled up to +5V by a 50kΩ resistor.
63	ADDR2	SMBus Address Bit 2: This bit is internally pulled up to +5V by a 50kΩ resistor.

Pin Number	Pin Name	Pin Function
64	ADDR1	SMBus Address Bit 1 (LSB): This address bit is the least significant bit of the MIC2358YLQ's 5-bit address bank. This bit is internally pulled up to +5V by a 50kΩ resistor.

Absolute Maximum Ratings[1]

PxOUTPOS, PxOUTNEG, 48VS .....-0.3V to +100V
PxGATE .....-0.3V to +6V
All other pins.....-0.3V to +6V
Storage Temperature (T_s) .....-65°C to +150°C
ESD Rating[3]
Human Body Model 1000V
Machine Model 100V
Lead Temperature (Soldering, 10 sec)
Lead-free Package (YML)
IR Reflow .....260°C +0°C/-5°C

Operating Ratings[2]

Supply Voltage (V_{IN}) ..... +43V to +60V
Ambient Temperature (T_A) ..... 0°C to +70°C
Junction Thermal Resistance
LQFP64 (θ_{JA}) No Air Flow.....42.34°C/W
LQFP64 (θ_{JC}) No Air Flow.....12.9°C/W

DC Electrical Characteristics[4]

(48VS – ARTN) = 48V; T_A = 25°C, unless otherwise noted. **Bold** values indicate specifications apply over the full operating temperature range of 0°C ≤ T_A ≤ +70°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Power Supplies						
V_{DD1}	5V Supply Voltage		**4.5**		**5.5**	V
I_{DD1}	5V Supply Current			**8**	**40**	mA
V_{CC}	48V Supply Voltage		**44**		**60**	V
I_{CC}	48V Supply Current			**0.05**	**.2**	mA
Detection, see Functional Characteristics Rsense=1Ω						
$V_{DETECT1}$	Detection Voltage Point 1	15kΩ ≤ RSIG ≤ 33kΩ	**2.8**	**3.6**	**9**	V
$V_{DETECT2}$	Detection Voltage Point 2	15kΩ ≤ RSIG ≤ 33kΩ	**3.8**	**7.2**	**10**	V
V_{DETECT}		VDETECT2-VDETECT1	**1**	**3.6**		V
$t_{DETECT1-2}$	Time between test points 1 & 2		**2**			ms
$V_{DETECTOC}$	Open-circuit Detection Voltage	RSIG = 332kΩ, 5%	**2.8**	**11**	**30**	V
$I_{DETECTSC}$	Short-circuit Detection Current Limit	RSIG = 0	**0**	**2.3**	**5**	mA
$R_{SIGvalid}$	Valid Signature Resistance		**19**		**26**	kΩ
$R_{SIGreject}$	Reject Signature Resistance		**R<15**		**R>33**	kΩ
C_{SIGMAX}	Maximum Valid Signature Capacitance		**0**		**.15**	µF
Classification, See Functional Characteristics						
V_{CLASS}	Classification Drive Voltage	0mA < ICLASS < 55mA	**15.5**	**19**	**20.5**	V
I_{CLASS}	Classification current compliance		**55**	**88**	**100**	mA
$I_{CLASSTH}$	Classification Current Threshold	Class 0-1 Class 1-2 Class 2-3 Class 3-4 Class 4 – Overcurrent	**5** **13** **21** **31** **45**		**8** **16** **25** **35** **51**	mA mA mA mA mA

DC Electrical Characteristics[4]

(48VS – ARTN) = 48V; T_A = 25°C, unless otherwise noted. **Bold** values indicate specifications apply over the full operating temperature range of 0°C ≤ T_A ≤ +70°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Global Overvoltage Protection						
V_{GOVP}	Global Overvoltage Protection Threshold Voltage	Input Supply voltage at which all ports are powered off		**59.3**		V
$V_{GOVPHYS}$	OVP Threshold Hysteresis			**1.3**		V
V_{GUVP}	Global Undervoltage Protection Threshold Voltage	Input Supply voltage at which all ports report as undervoltage fault		**43.5**		V
$V_{GUVPHYS}$	UVP Threshold Hysteresis			**0.25**		V
$GATE_n$ Drive						
V_{GATE}	External GATE Drive Voltage	$\Delta V_{GATE} = V_{GATEN}$ – ARTN	**4**	**5**		V
I_{GATEUP}	GATE Pin Charge Current			**50**		µA
I_{GATEDN}	GATE Pin Discharge Current			**2.7**		mA
$I_{GATEOFF}$	GATE Pin FAULT mode Pull-down Current	Vol = 5.0V	**50**	**65**		mA
$Port_n$ Sense Input						
R_{PORT}	Port Sense Input Resistance	Portn = ON; PPn and PNn measured to ARTN	**0.7**	**1**	**1.3**	MΩ
$Port_n$ Current Sense Rsense=1Ω						
V_{SUOC}	Start-up Current Limit Threshold Voltage		**408**	**424**	**442**	mV
V_{SSOC}	Overload Current Detection Threshold Voltage	Class 0 Class 1 Class 2 Class 3	**344** **92** **160** **344**	**373** **102** **174** **373**	**396** **106** **182** **396**	mV mV mV mV
V_{SC}	Short-circuit Current Limit Threshold Voltage		**408**	**424**	**442**	mV
$V_{DCMPSMIN}$	DC MPS Disconnect Threshold Voltage		**5.2**	**8**	**9.8**	mV
I_{SENSE}	SENSE Pin Bias Current			**8**	**50**	µA
Internal AC Disconnect Oscillator						
f_{OSC}	Oscillator Output Frequency		**79**	**86**	**500**	Hz
V_{OSCP-P}	Oscillator Output Voltage	48VS = 48.0V	**3.25**	**4.4**	**10**	V_{PP}
Shared Power Management (SPM)						
V_{SPMREF}	SPM Voltage Reference		**2.45**	**2.5**	**2.55**	V
I_{SPMREF}	SPM Standard Unit Current	RSPM = 250kΩ		**10**		µA

DC Electrical Characteristics[4]

(48VS – ARTN) = 48V; T_A = 25°C, unless otherwise noted. **Bold** values indicate specifications apply over the full operating temperature range of 0°C ≤ T_A ≤ +70°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Digital Logic Interface						
$V_{IL(SMBus)}$		SCL, SDAIN		**1.35**		V
$V_{IH(SMBus)}$		SCL, SDAIN		**1.58**		V
$I_{IH(SMBus)}$		SCL, SDAIN		**0.1**	**5**	µA
$V_{OL(SMBbus)}$	(SDAOUT,/SMBINT)	I_{OL} = 4mA		**0.1**	**0.4**	V
V_{IL}		ADDR[5:1], Autonomous select pins, /RST, /CS		**2.5**		V
V_{IH}		ADDR[5:1], Autonomous select pins, /RST, /CS		**2.5**		V
R_{PULLUP}		Autonomous select pins, /RST, /CS, ADDR[5:1]		**59**		kΩ

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
4. Specification for packaged product only.

AC Electrical Characteristics[4]

(48VS – ARTN) = 48V; T_A = 25°C, unless otherwise noted. **Bold** values indicate specifications apply over the full operating temperature range of 0°C ≤ T_A ≤ +70°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_{DET}	Detection Duration	Time to measure PD signature resistance		**100**	**500**	ms
t_{PDC}	Classification Delay Time	Time to classify the PD.	**10**	**19.5**	**75**	ms
t_{DBO}	Detection Backoff Delay Time	Alternative B configuration ONLY	**2**	**2.1**	**16**	s
t_{ED}	Detection delay after error		**750**	**1000**	**10000**	ms
t_{PORAM}	Power On Delay, Autonomous Mode	– From valid detect to Port On in Autonomous mode	**0**	**39**	**400**	ms
$t_{ILIMMAX}$	Maximum ILIM Duration during Port Initialization	– IEEE 802.3af applications	**30**	**57**	**75**	ms
$t_{ICUTMAX}$	Maximum ICUT Duration during Steady-state Operation	– IEEE 802.3af applications	**50**	**55**	**75**	ms
t_{MPSDLY}	AC / DC MPS disconnect delay time		**300**	**335 /360**	**400**	ms
$t_{DCMPSPW}$	DC MPS Disconnect minimum pulse width	See $V_{DCMPSMIN}$		**50**	**60**	ms
SMBus Interface Timing						
t_{SCL}	SCL (serial clock) period		**2.5**			µs
t2	SDA Setup Time to SCL High		**100**			ns
t3	SDA Hold Time to SCL Low		**300**			ns
t4	SDA Low Setup Time to SCL Low		**100**			ns
t5	SDA High Hold Time to SCL High		**100**			ns
$t_{ARA-INT}$	ARA to /SMBINT Pin HIGH Time		**20**		**300**	ns

Notes:

1. GBNT – Guaranteed by design and characterization, not tested in production.
2. Exceeding the absolute maximum rating may damage the device.
3. The device is not guaranteed to function outside its operating rating.
4. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
5. Specification for packaged product only.

Functional Description

The MIC2358YLQ operations are fully compliant with the IEEE 802.3af-2005 standard. States referenced in this section are per IEEE PSE State Diagram. See DC and AC Electrical Characteristics sections for timers, voltage threshold, and current threshold values.

Autonomous Operation

The autonomous mode allows for applications that have no central host controller, or have limited supervision of the MIC2358YLQ.

With the ENABLE_L pin low during power-up, the MIC2358YLQ will initialize and immediately begin checking ports for valid detection signatures, and if present, perform classification and apply power.

Managed Operation

In Managed mode, the MIC2358YLQ may be configured and monitored by an external host processor. Operations include: PD detection, classification, diagnostics, power budget, power-on, power-off, check status, detect faults, AC/DC disconnect detection, voltage and current measurement per port basis.

With the ENABLE_L pin high during device power-up, the MIC2358YLQ will initialize, but will not begin to perform detection on any port until instructed from an external host controller via SMBus.

Reset

At power-up or anytime the MIC2358YLQ supports both hard and soft reset. Upon reset, all ports immediately shut off and internal registers default to values as shown in Register Description section.

Upon a reset operation, the MIC2358YLQ will be configured based on the strap-in pins: ENABLE, DCMPS, ACMPS, ICO, and ALTB (see Pin Description for configuration details). These register bits may be programmed by the host. Any changes to these pins after reset are ignored.

Power Delivery Control

The primary function of the MIC2358YLQ is to control power delivery to each PSE port. It does this by controlling the gate drive voltage of an external N-Channel power FET while monitoring the current through a sense resistor (RS, PnSENSE) and the output voltage across the positive (PnOUTPOS) and negative (PnOUTNEG) terminal pins, where n is the port number (1-8). At power-up, the isolated 48V input supply is coupled to the port in an inrush-controlled manner. Power will then be delivered to the connected PD based upon its classification sensed at power-up. The gate drive logic is designed to prevent simultaneous power-up of ports.

The sense resistor value was selected to reduce power loss and the voltage. The 1Ω resistor is connected between source and the MIC2358YLQ Sense-ARTN pins.

By measuring this voltage across the sense resistor, the MIC2358YLQ sense terminal pin specifically monitors current flow during port classification, power-up inrush, power-on short, power-on overload, and DC disconnect detect. It also measures PD load current on demand by the host.

PD Detection

The MIC2358YLQ will not deliver power until a valid PD is detected. A valid PD has a 25kΩ discovery signature as specified in the IEEE 802.3af standard. The detection cycle is repeated continuously until a valid PD is detected. The status of PD discovery signature for each port is available to the host.

During PD detection, the MIC2358YLQ uses an internal FET to force probe voltages VDETECT1 and VDETECT2 across the port's power terminals (PnOUTPOS, PnOUTNEG). The resulting currents to the port are determined by measuring the voltage across an external 1kΩ resistor that must be connected to the RDET pin. A two-point V-I slope measurement is used as specified by the IEEE 802.3af standard to verify that a valid signature resistance is connected to the port.

The IEEE802.3af standard requires mid-span PSE (Alternative B) to support backoff timing. This causes the port to wait a time period specified by tDBO before attempting another detection cycle after every failed PD detection. With the ALTB pin high during reset or enabled by the host, the MIC2358YLQ ports are initialized as Alternative B.

PD Classification

PD Classification enables each PD to request the power level from the PSE. Per IEEE802.3af standard, classification is preceded by successful detection cycle and is optional. PD Classifications status for each port is available to the host upon completion of the PD Classification process.

During classification, the MIC2358YLQ turns on the external FET and forces probe voltage VCLASS across the positive and negative terminals of the port. The resulting current is measured across RS. The measured current determines the class of the PD as shown in Table 1.

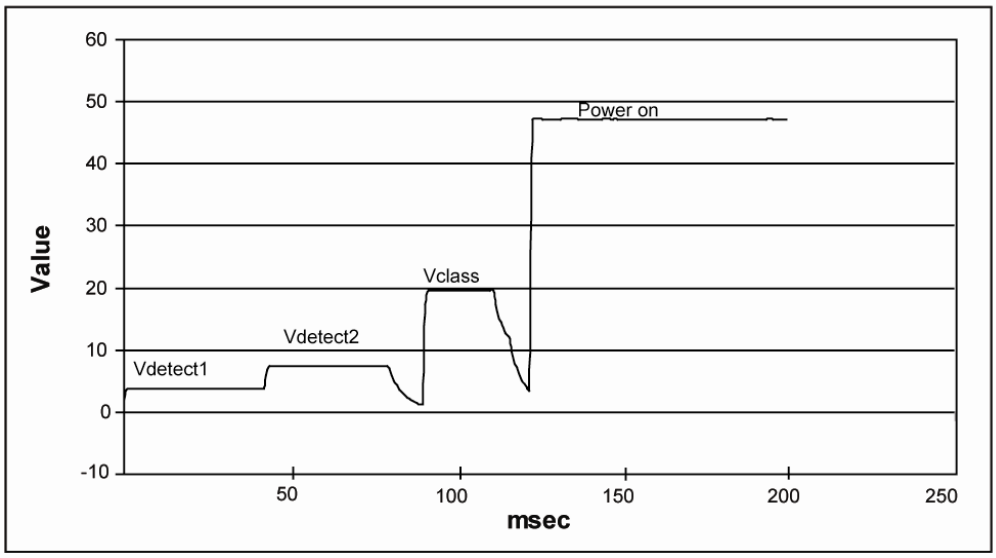
Successful PD Classification does not necessarily guarantee that the PSE will be able to deliver power to the PD at a particular port. The MIC2358YLQ enables the power budget to be managed by the host (Managed Mode) or the unique Shared Power Management (Autonomous Mode). The MIC2358YLQ allows the host

to predefine a maximum class to determine the power level to be supplied to a detected PD. A PD classification exceeding its maximum class will go to the POWER_DENIED state.

With the ICO pin high during reset, classifications of all ports are forced to class 0. This provides system flexibility for Class 1 or Class 2 PD devices such as a security camera that violate its class current often due to many motor start-up occasions.

IEEE 802.3af	Classification Current at PSE	Maximum PD Power	Maximum PSE Output Power Per Port	Class Description
0	0mA to 5mA	12.95W	15.4W	PD Does Not Implement Classification, Unknown Power
1	8mA to 13mA	3.84W	4W	Low Power PD
2	16mA to 21mA	6.49W	7W	Medium Power PD
3	25mA to 31mA	12.95W	15.4W	High or Full Power PD
4	35mA to 45mA	12.95W	15.4W	Reserved, Power as Class 0

Table 1. IEEE 802.3af Powered Device Classes



Detection Timing

Powered State

Assuming sufficient power budget is available, after a successful PD detection and optional classification cycle. The MIC2358YLQ enters POWER_UP state and begins applying 48V power to the port in an inrush-controlled manner. If the sense terminal exceeds VSUOC, an internal current-limiting circuit regulates the gate drive voltage, limiting the current to Iinrush = VSUOC / RS. If the current-limit condition persists, when the startup timer, tILIMMAX, times out, the port shuts off and fault condition is reported as short event

After a fault free power-up, the MIC2358YLQ enters POWER_ON state and maintains 48V power to the port in a steady-state manner. During steady-state power delivery, the MIC2358YLQ constantly checks for overload conditions by monitoring ICUT = VSSOC / RS. If the overload condition persists for a time period greater than $t_{ICUTMAX}$, the overload timer times out, the port shuts off and an overload event is reported. During steady-state power delivery, if the sense terminal exceeds VSC, an internal current-limiting circuit regulates the gate drive voltage, limiting the current to Ilim = VSC / RS. If the current-limit condition persists, when the timer, tILIMMAX, times out, the port shuts off and fault condition is reported as short event. Under all circumstances neither Ilim nor Iinrush are allowed to exceed their respective maximum threshold.

In the TEST_MODE state, the MIC2358YLQ checks the selected port for short or overload faults with the same method used during POWER_UP and POWER_ON states.

Disconnect Detection

Disconnect Detection ensures that the MIC2358YLQ PSE shuts off power delivery when a PD is disconnected from a port. The IEEE 802.3af standard specifies two methods for determining that a PD has disconnected from the PSE referred to as DC or AC Maintain Power Signature (MPS).

With the DCMPS pin high during reset or enabled by host, the MIC2358YLQ DC disconnect detection function starts at beginning of POWER_UP state. If the sense terminal falls below VDCMPSMIN for time out period of tMPSDLY, the port shuts off and fault condition is reported as DCMPS absent event.

With the ACMPS pin high during reset or enabled by host, the MIC2358YLQ AC disconnect detection function starts at beginning of POWER_UP state. The MIC2358YLQ produces a low frequency square wave on the ACDRIVE pin. This signal is level-shifted through a single external 47µF capacitor, then injected on to the positive terminal of each port through an external 1.96kΩ AC current sense resistor. The voltage amplitude of the AC probing signal is measured by the ACSENSE pin of the MIC2358YLQ. The AC current into each port is measured by sensing the voltage drop across the external AC sense resistor. By combining the sensed voltage and current, the MIC2358YLQ can then determine if the low-frequency AC impedance on the port is within the limits specified by 802.3af. If the impedance falls outside of the AC maintain power signature limits for longer than tMPSDLY, the port shuts off and fault condition is reported as an ACMPS absent event.

If both DC and AC disconnect are enabled on a port, then per section 33.2.10.1 of the 802.3af standard, both the DC and AC maintain power signatures must be present on a port to keep it powered. If either the DC or the AC maintains power signature does not exist for longer than tMPSDLY, then the port will be shut off.

A port with neither, DC or AC disconnect enabled will not power off automatically when the PD is removed.

Shared Power Management

In Managed Mode, an external host management applications manages the available power budget, and maintains which ports are powered up and at what classification. For systems where no host management application is present or where it is not desired to burden, the controller with power budget management tasks, the MIC2358YLQ performs Shared Power Management to manage the power budget in Autonomous mode.

The power budget is established by selecting the appropriate values of a pair of resistors. A 250kΩ resistor is placed between the SPMREF pin and ground. The MIC2358YLQ will apply 2.5V to this resistor to establish a per-watt-of-power reference current (nominally 10µA per Watt). Another resistor is placed from the SPMBUS pin-to-ground, with a value that establishes the size of the system power budget. The value of the resistor is determined by dividing 2.5V by the reference current (10µA), then dividing by the total power budget in Watts.

For example, if the total power budget is 100W, then the SPMBUS resistor should be 2.5kΩ. Then, when the MIC2358YLQ powers up a port, it will also source a current out of the SPMBUS pin that is proportional to the maximum power for that port's classification. As more ports power up, these currents all sum together, and the voltage at SPMBUS will increase accordingly. Once the voltage on SPMBUS has reached 2.5V, the total power budget has been allocated, and the MIC2358YLQ will not allow additional ports to power up until an already powered port is powered off.

The power budget may be managed across multiple MIC2358YLQ devices by tying together the SPMBUS pins of each device to a single budget-establishing resistor.

To disable Shared Power Management tie the SPMBUS pin-to-ground or disable SPM by the host.

Port Prioritization

The MIC2358YLQ offers Port Priority to enable additional flexibility in managing the power budget.

In Managed Mode, the host software can assign each port one of four levels of priority: critical, high, medium, or low. During an emergency power supply disruption event such as brown out, the host has the flexibility to globally declare a minimum priority level for a port to be powered following detection of a PD and/or declare a minimum priority level for a port to remain powered. Each individual port's assigned priority level is compared with global priority declaration and if determined of a lower priority level will then go to the POWER_DENIED state.

If multiple ports are assigned the same priority level (higher than the minimum priority referred to above), and the power supply is inadequate to power all of the ports, then none of the ports will be powered normally. Thus it is important to manage the priority levels for the most important levels.

The Port Prioritization power management scheme is complementary to Shared Power Management.

Supply Voltage Overvoltage and Undervoltage Protection

The MIC2358YLQ monitors the input power supply for overvoltage and undervoltage conditions. If the supply voltage reaches VGOVP, all ports immediately shut off and overvoltage fault status is reported to host by the Global Status Register (0x45) bit 1, which may be read by the host.

If the supply voltage drops off to VGUVP, undervoltage fault status is reported to host by the Global Status Register (0x45) bit 2, which may be read by the host.

Digital Logic Power

The MIC2358YLQ must be supplied with 5V (VDD). VDD supplies power for most of device internal analog and all internal logic circuitry including SMBus interface. All logic inputs and outputs reference to DRTN. DRTN and ARTN are completely isolated internally to the MIC2358YLQ.

Non-Compliant IEEE 802.3af Features

For enhanced system flexibility, the MIC2358YLQ supports non-compliant IEEE 802.3af or legacy PDs detection resistance value. This would enable the MIC2358YLQ to support pre-802.3af standard PD Detection schemes. The host can program acceptable lower threshold as low as 400Ω (dec 1x400) by the Global_Detect_Min_Register (0x48) and higher threshold as high as 102kΩ (dec 255x400) by the Global_Detect_Max_Register (0x49). This programming affects all ports and cannot be done per port basis.

SMBus Serial Interface

The MIC2358YLQ communicates with a host (master) using the standard 2-wire interface as described in the SMBus Specification Version 2.0.

The SMBus is an extension of the I2C bus, and the MIC2358YLQ is also compatible with the I2C bus standard. The I2C interface allows easy application of opto-coupler circuitry to maintain system isolation when a ground based micro-controller host is required. The MIC2358YLQ features separate input and output data pins (SDAIN and SDAOUT) for use with opto-couplers. For applications where opto-isolation is not required, SDAIN and SDAOUT are tied together.

The SMBus standard requires seven-bit device addressing. The MIC2358YLQ top two most significant address bits are hardwired to 10 with the next five bits specified by strapping five pins on the device.

The MIC2358YLQ uses standard Write_Byte and Read_Byte, for communication with its host. The Write_Byte operation (see Figure 1) involves sending the device's slave address (with the R/W bit low to signal a write operation), followed by the address of the register to be operated upon and the data byte. The Read_Byte operation (see Figure 2) is a composite write and read operation: the host first sends the device's slave address followed by the register address, as in a write operation. A new start bit must then be sent to the MIC2358YLQ, followed by a repeat of the slave address with the R/W bit (LSB) set to the high (read) state. The data to be read from the part may then be clocked out.

The MIC2358YLQ expects to be interrogated using the Alert Response Address once it has asserted its interrupt output, /SMBINT. Following an interrupt, a successful response to the A.R.A. *or* a read operation on EVENT register will cause /SMBINT to be de-asserted. EVENT will also be cleared by the read operation. Reading EVENT following an interrupt is an acceptable substitute for using the A.R.A., if the

host system does not implement the A.R.A protocol. Illustrates A.R.A responding to MIC2358YLQ interrupts.

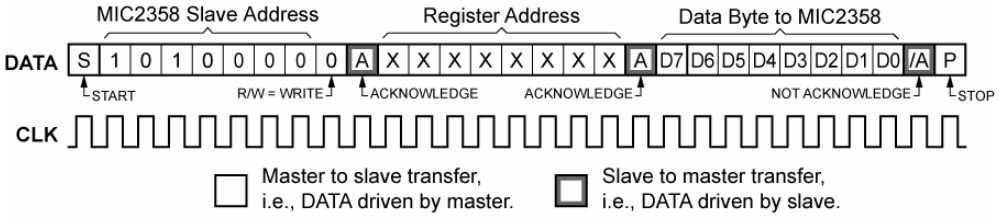


Figure 1. Write Byte Protocol

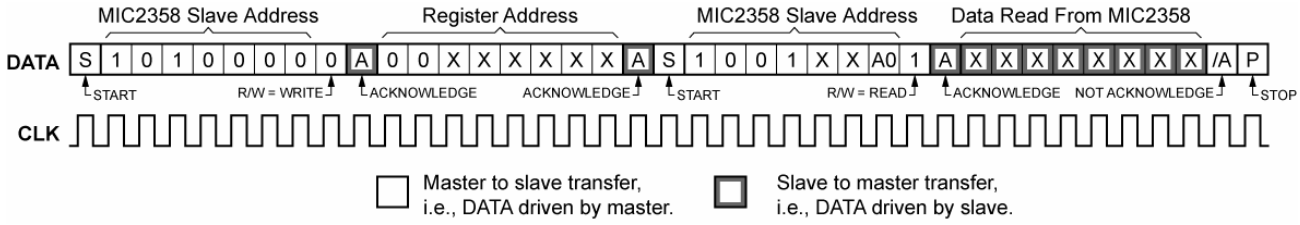


Figure 2. Read Byte Protocol

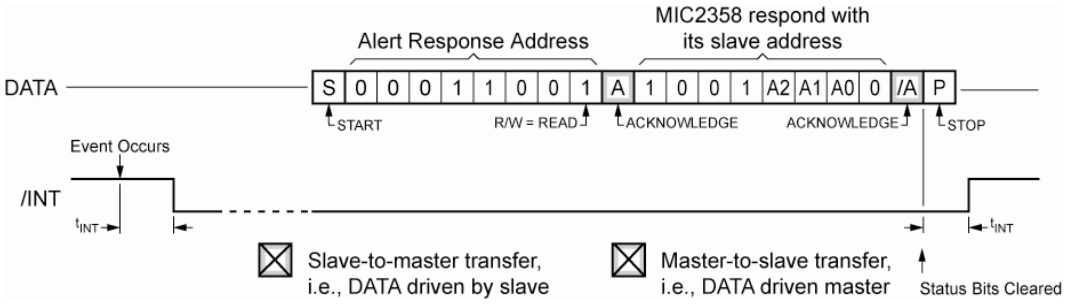


Figure 3. Alert Response Address Protocol

Typical Application

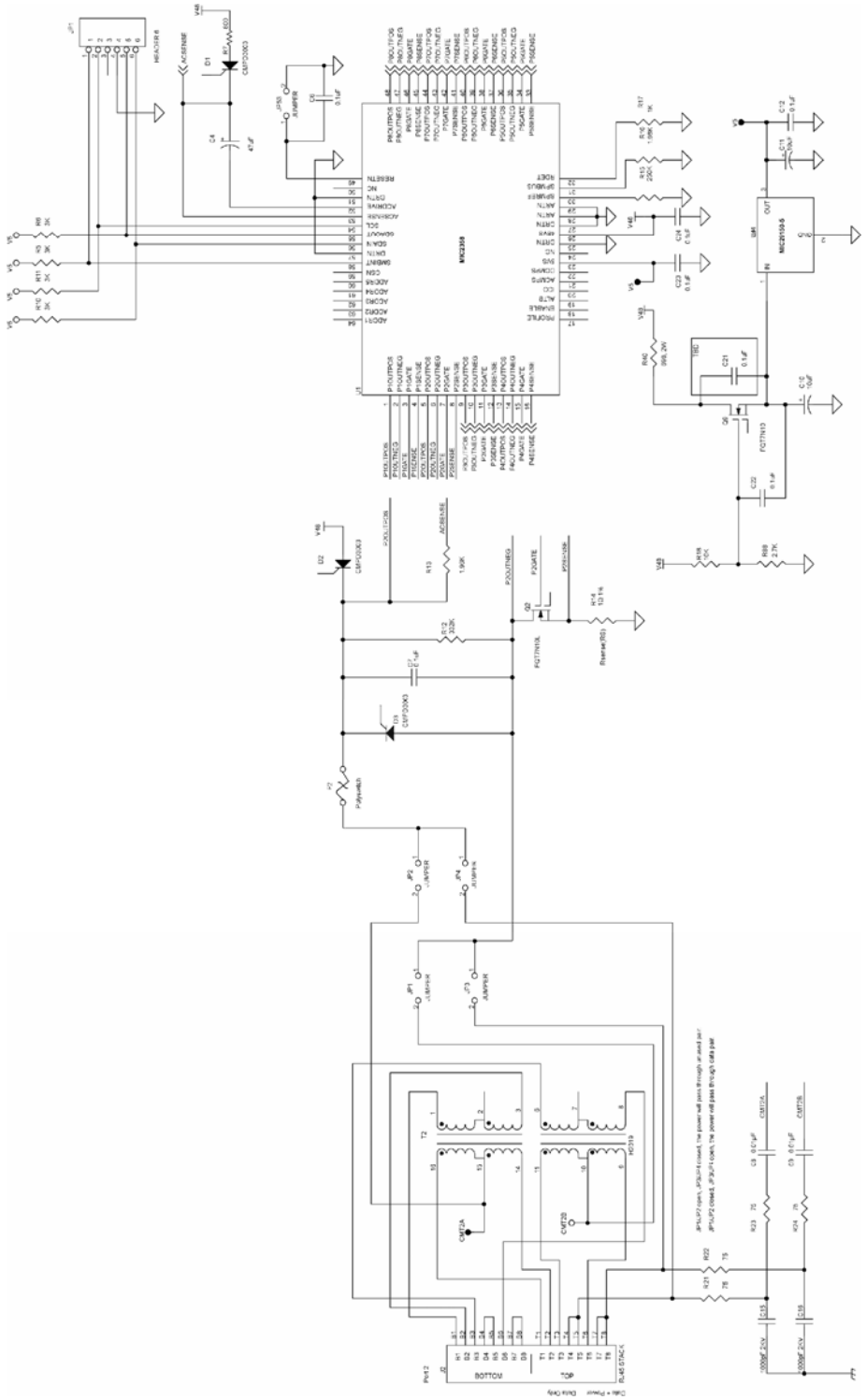


Figure 4. Midspan Configuration for 1 port of 8 ports

Register Definitions

Purpose

The MIC2358YLQ uses write registers to configure the operation of the device and read registers to supply information about the operation of the device. These registers are accessed through the SMBus interface.

Register Map

The SMBus can address 128 individual registers, as shown in Table 1. Each port has eight assigned registers: four that have read/write access, three that are read only, and one that is read only and is cleared after being read. There are 11 global registers: six read/write and five read only. The remaining registers are reserved for factory testing purposes. These test registers may be read without harm, but should not be written. The test register definitions are not included in this document.

Table 2 shows the internal structure of the registers assigned to each port. Table 3 shows the internal structure of the global registers.

Global registers affect all ports. Port registers affect individual ports only.

The remainder of this document explains in detail the use of each register, and if appropriate the meaning and use of individual bits within a register.

Conventions

Throughout this document, SMBus registers are referenced using BOLD_UPPERCASE. Individual bits within a register are referenced using *italic_lowercase*. States from the state machine diagram are shown in Figure 33-6 of the IEEE std 802.3af are written using REGULAR_UPPERCASE.

	-0	-1	-2	-3	-4	-5	-6	-7
0x0-	Port 1 Control	Port 1 Option	Reserved	Reserved	Port 1 Voltage	Port 1 Current	Port 1 Status	Port 1 Event
0x1-	Port 3 Control	Port 3 Option	Reserved	Reserved	Port 3 Voltage	Port 3 Current	Port 3 Status	Port 3 Event
0x2-	Port 5 Control	Port 5 Option	Reserved	Reserved	Port 5 Voltage	Port 5 Current	Port 5 Status	Port 5 Event
0x3-	Port 7 Control	Port 7 Option	Reserved	Reserved	Port 7 Voltage	Port 7 Current	Port 7 Status	Port 7 Event
0x4-	Global Config	Global Power Set-Up	Global Event Mask	SMBus Status	Global SRQ	Global Status	Global Current Port	reserved
0x5-	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
0x6-	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
0x7-	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Read & Write Read Only Read Only, Clear on Read

	-8	-9	-A	-B	-C	-D	-E	-F
0x0-	Port 2 Control	Port 2 Option	Reserved	Reserved	Port 2 Voltage	Port 2 Current	Port 2 Status	Port 2 Event
0x1-	Port 4 Control	Port 4 Option	Reserved	Reserved	Port 4 Voltage	Port 4 Current	Port 4 Status	Port 4 Event
0x2-	Port 6 Control	Port 6 Option	Reserved	Reserved	Port 6 Voltage	Port 6 Current	Port 6 Status	Port 6 Event
0x3-	Port 8 Control	Port 8 Option	Reserved	Reserved	Port 8 Voltage	Port 8 Current	Port 8 Status	Port 8 Event
0x4-	Global Detect Min	Global Detect Max	reserved	reserved	reserved	reserved	Global ID	Global REV
0x5-	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
0x6-	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
0x7-	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Table 2. SMBus Register Map

	Port Control (-0, -8)	Port Option (-1, -9)	Port Reserved (-2, -A)	Test (-3, -B)	Port Voltage (-4, -C)	Port Current (-5, -D)	Port Status (-6, -E)	Port Event (-7, -F)
Bit 7		classify_and_deny						
Bit 6		max_class						power_denied
Bit 5							pse_status	valid_signature
Bit 4	dc_mps							Invalid_signature
Bit 3	ac_mps	monitor						short_circuit
Bit 2	classify	event_hold						overload
Bit 1	force_power	priority					pd_class	dc_mps_absent
Bit 0	Disable							ac_mps_absent

Read & Write | Read Only | Read Only, Clear on Read

Table 3. Port Registers

	Global Config (0x40)	Global Power Set-Up (0x41)	Global Event Mask (0x42)	Global SMBus Status (0x43)	Global SQR (0x44)	Global Status (0x45)	Global Current Port (0x46)	Global Detect Min (0x48)	Global Detect Max (0x49)	Global ID (0x4E)	Global Rev (0x4F)
Bit 7					port_8						
Bit 6		max_ class	power_ denied		port_7						
Bit 5			valid_ signature		port_6						
Bit 4	Ignore_ faults		Invalid_ signature		port_5						
Bit 3	enable_ spm	min_ priority_ new_ power	short_ circuit		port_4						
Bit 2	Ignore_ class_ overload		overload		port_3		current_ port				
Bit 1	Alternative _b	min_ priority_ maintain_ power	dc_mps_ absent		port_2		current_ port				
Bit 0	restore_ default_ setup		ac_mps_ absent	enable_ SMBINT	port_1	smp_ fault	current_ port				

Read and Write | **Read Only**

Table 4. Global Registers

Port Control Register

SMBus Address: 0x00, 0x08, 0x10, 0x18, 0x20, 0x28, 0x30, 0x38

Read and Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	dc_mps	ac_mps	classify	force_power	disable

Name	Default	Description
dc_mps	Note 1	Enables DC maintain power signature detection.
ac_mps	Note 2	Enables AC maintain power signature detection.
classify	1	Enables classification.
force_power	0	Puts the port into the TEST_MODE state.
disable	Note 3	Puts the port into the DISABLE state.

Notes:

1. Initial state determined by DCMPS input pin
2. Initial state determined by ACMPS input pin
3. Initial state determined by ENABLE input pin. If cleared, puts the port into the IDLE state.

Port Option Register

SMBus Address: 0x01, 0x09, 0x11, 0x19, 0x21, 0x29, 0x31, 0x39

Read and Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
classify_ and_deny	max_class			monitor	event_hold	priority	

Name	Default	Description
classify_and_deny	0 (Note 1)	The port will be detected and classified, but power will be denied (i.e,. put into POWER_DENIED state).
max_class	0	Maximum class allowed for new power to be supplied to a detected PD.
monitor	0	Enables readback of the port voltage and current.
event_hold	0	Prevents the port from starting a new detection cycle when an unmasked event is stored in the event register.
priority	Low	Port priority level for power management. Possible settings are shown below. This setting is used in conjunction with the *minimum_priority_new-power* and *minimum_priority_maintain_power* settings in the global POWER_SETUP register.

Port Priority Levels

Name	Value
critical	11
high	10
medium	01
low	00

Note:

1. Bit classify must be enabled in Control register

Port Voltage Register

SMBus Address: 0x04, 0x0C, 0x14, 0x1C, 0x24, 0x2C, 0x34, 0x3C

Read Only

The Voltage register holds the 8-bit value of the measured port voltage. The LSB is equivalent to 0.25V. The register is only valid if the monitor bit of the port option register is set; otherwise it reads as 0x00.

Port Current Register

SMBus Address: 0x05, 0x0D, 0x15, 0x1D, 0x25, 0x2D, 0x35, 0x3D

Read Only

The Current register holds the 8-bit value of the measured port current. The LSB is equivalent to 2mA. The register is only valid if the monitor bit of the port OPTION register is set; otherwise it reads as 0x00.

Port Status Register

SMBus Address: 0x06, 0x0E, 0x16, 0x1E, 0x26, 0x2E, 0x36, 0x3E

Read Only

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	pse_status				pd_class		

Name	Description
pse_status	Indicates the port PSE Status bits from the Table 33-16 of *IEEE Std 802.3af*. Possible values are shown below
pd_class	Indicates the class of a detected PD. Possible values are shown below. (Note 1)

PSE Status

Status	Value
Disabled	000
Searching	001
Delivering Power	010
Test mode	011
Test error	100
Implementation specific fault	101
Reserved	110
Reserved	111

PD Class

Class	Value
Class 0	000
Class 1	001
Class 2	010
Class 3	011
Class 4	100

Note:

1. Per *IEEE Std 802.3af*, PD class defaults to 0 if classification is disabled.

Port Event Register

SMBus Address: 0x07, 0x0F, 0x17, 0x1F, 0x27, 0x2F, 0x37, 0x3F

Read Only, Clear on Read

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	power_ denied	valid_ signature	invalid_ signature	short_circuit	overload	dc_mps_absent	ac_mps_absent

Name	Description
power_denied	Set when the port was not powered, or power was removed, and the state machine enters the power_denied state.
valid_signature	Set when a valid signature is detected.
Invalid_signature	Set when an invalid signature is detected.
short_circuit	Set when a short circuit condition occurs.
overload	Set when an overload condition occurs.
dc_mps_absent	Set when the DC maintain power signature drops out.
ac_mps_absent	Set when the AC maintain power signature drops out.

Notes:

1. Port EVENT register bits correspond to PSE Status register bit[12..7] from Table 33-16 of *IEEE Std 802.3af-2005*. MPS Absent bit is reported separately as *dc_mps_absent and ac_mps_absent.*
2. Port EVENT register is associated with other behaviors of the MIC2358YLQ. The first behavior is the assertion of the /SMBINT pin (pin 58). If the port has an event occur that is not masked by the global EVENT_MASK register, then the /SMBINT pin will be asserted, letting the host know that an event has occurred.
3. The second behavior is the event holding. If the event hold bit in the port OPTION register is clear and an unmasked event occurs on this port, then the MIC2358YLQ will attempt another at detection on this port. If the event_hold bit in the port OPTION register is set and an unmasked event occurs on this port, then the MIC2358YLQ will make no further attempts to do detection on this port until the host has cleared the event_hold bit. This gives the host the opportunity to analyze what caused the event on the port and deal with it accordingly, prior to trying to power up the port again.

Global Configuration Register

SMBus Address: 0x40

Read and Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	_	enable_spm	Ignore_class_ overlaod	alternative_b	restore_default _setup

Name	Default	Description
enable_spm	1	Turns on the shared power management feature.
ignore_class_overload	Note 1	Inhibits shutdown of port power if its current exceeds the class-dependent overload current, i.e. overload current will be equal to Class 0 level. Shutdown will still occur if the current exceeds the short-circuit threshold.
alternative_b	Note 2	Enables Alternative B behavior, which adds a backoff delay following an invalid detection.
restore_default_setup	0	Software Reset. Forces the controller to restart and return all settings to default values. This bit will be cleared once the reset is complete.

Notes:

1. Initial state determined by ICO input pin.
2. Initial state determined by ALTB input pin.

Global Power_Setup Register

SMBus Address: 0x41

Read and Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	max_class			minimum_priority_new_power		minimum_priority_maintain_power	

Name	Default	Description
max_class	Class 0 (Note 1)	Specifies the maximum class that will be powered after detection of a new powered device. Possible values are shown following the port STATUS register description.
minimum_priority_new_power	Low (Note 2)	Sets the minimum priority level for a port to be powered following detection of a powered device. A port with a lower priority will go to the POWER_DENIED state. Possible values are shown following the port OPTION register description.
minimum_priority_maintain_ power	Low (Note 3)	Sets the minimum priority level for a port to remain powered. A port with a lower priority will go to the POWER_DENIED state. Possible values are shown following the port OPTION register description.

Notes:

1. The max_class is defined independently in both global POWER_SETUP and port OPTION registers. After a PD has been classified, the detected class is compared to these two values. If the PD is requesting more power than either of the max_class fields, then that port will not be powered. Upon power-up or, reset, global max_class and all port max_class default to Class 0.

   Examples: The host sets global max_class to Class 2, and Port 5 max_class to Class 1. A PD is plugged into port 1 and classifies as Class 0. This is more power than allowed by global max_class, so power will be denied to port 1. Another PD is plugged into port 2 and classifies as Class 2. This is equal to global max_class and less than port 2's max_class (which defaulted to Class 0), so port 2 is powered up. A Class 2 PD is plugged into port 5. This is equal to global max_class, but greater than port 5's max_class, so power is denied. Then a Class 1 PD is plugged into port 5. This is less than global max_class and equal to port 5's max_class, so the port is powered.
2. When a valid PD is detected on a port, that port's priority level is compared to the minimum_priority_new_power field in the global POWER_SETUP register. If the port's priority is equal to or greater than the minimum_priority_new_power, then the port will be powered up. Otherwise, the port will go to the POWER_DENIED state of the state diagram.
3. When the value of the minimum_priority_maintain_power field in the global POWER_SETUP register is changed, the MIC2358YLQ will check this against the priority level of all ports that are currently powered. If a port's priority level is equal to or greater than the minimum_priority_maintain_power, then that port will continue being powered up. If a port's priority level is less than the minimum_priority_maintain_power, then power will be removed from that port and it will go to the POWER_DENIED state of the state diagram.

Global Event_Mask Register

SMBus Address: 0x42

Read and Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	power _denied	valid_ signature	invalid_ signature	short_circuit	overload	dc_mps_ absebt	ac_mps_absent

Name	Default	Description
power_denied	1	Masks all ports from responding to a power denied event.
valid_signature	1	Masks all ports from responding to a valid signature event.
invalid_signature	1	Masks all ports from responding to an invalid signature event.
short_circuit	1	Masks all ports from responding to a short circuit event.
overload	1	Masks all ports from responding to an overload event.
dc_mps_absent	1	Masks all ports from responding to a DC MPS dropout event.
ac_mps_absent	1	Masks all ports from responding to an AC MPS dropout event.

Note:

1. This port is associated with every port EVENT register. If any port has an event occur that is not masked by the global EVENT_MASK register, then the /SMBINT pin will be asserted.

Global SMBus_Status Register

SMBus Address: 0x43

Read and Write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	–	–	–	enable_SMBINT

Name	Default	Description
enable_smbint	1	Cleared once the device has won SMBus INT Response Address arbitration. Must be set with SMBus commands to restore the /SMBINT functionality.

Global SRQ Register

SMBus Address: 0x44

Read Only

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
port_8	port_7	port_6	port_5	port_4	port_3	port_2	port_1

Name	Description
port_8	Set when an unmasked event is set in the PORT_EVENT register for Port 8.
port_7	Set when an unmasked event is set in the PORT_EVENT register for Port 7.
port_6	Set when an unmasked event is set in the PORT_EVENT register for Port 6.
port_5	Set when an unmasked event is set in the PORT_EVENT register for Port 5.
port_4	Set when an unmasked event is set in the PORT_EVENT register for Port 4.
port_3	Set when an unmasked event is set in the PORT_EVENT register for Port 3.
port_2	Set when an unmasked event is set in the PORT_EVENT register for Port 2.
port_1	Set when an unmasked event is set in the PORT_EVENT register for Port 1.

Note:

1. Global SRQ register provides the host a quick starting point to determine which port is reporting occurrence of an event, if any. During service of /SMBINT or polling, the host can read the global SRQ register first to determine which port had the event, then read that port's EVENT register to determine which specific event occurred.

Global Status Register

SMBus Address: 0x45

Read Only

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	–	UVP	OVP	spm_fault

Name	Description
spm_fault	Set when the port has requested more power than is available as indicated by the shared power management controller. The port state machine will transition to the POWER_DENIED state.
OVP	Set when the power supply exceeds Global Overvoltage Protection Threshold Voltage V_{GOVP}.
UVP	Set when the power supply drops off below Global Undervoltage Protection Threshold Voltage V_{GUVP}.

Global Current_Port Register

SMBus Address: 0x46

Read Only

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	–	current_port		

Name	Description
current_port	Indicates which port is currently being managed by the chip. Possible values are shown below.

Ports

Status	Value
Port 1	000
Port 2	001
Port 3	010
Port 4	011
Port 5	100
Port 6	101
Port 7	110
Port 8	111

Note:

1. The MIC2358YLQ implements a single ADC to service all ports during detection, classification, measurement of port output voltage and current. The *current_port* indicates which particular port is being serviced. This register allows the host with capability to monitor internal ports activity timing.

Global Detect_Min Register

SMBus Address: 0x48

Read and Write

This register is used to program the lower limit of acceptable resistor values for detecting a powered device. The weighting is 400Ω and the default value is 40 dec (0x28 hex). The default value of 40 means the lower limit is 40 x 400 = 16000Ω. Setting this register to a different value could cause operation that does not comply with IEEE Std 802.3af-2003.

Global Detect_Max Register

SMBus Address: 0x49

Read and Write

This register is used to program the upper limit of acceptable resistor values for detecting a powered device. The weighting is 400Ω and the default value is 68 dec (0x44). The default value of 68 means the upper limit is 68 x 400 = 27200Ω. Setting this register to a different value could cause operation that does not comply with IEEE Std 802.3af-2003.

Global ID Register

SMBus Address: 0x4E

Read Only

Reading this register returns the part ID number as 0x58.

Global REV Register

SMBus Address: 0x4F

Read Only

Reading this register returns the part revision number as 00.

Programming Guide

There are several ways of turning on a port in a system where the host manages the power budget. The following example outlines one such method.

The ENABLE_L pin is high, so that the host can gain control of the MIC2358YLQ before any attempt is made to power ports. The host sets the classifies and deny and event_hold bits in every port OPTION register, and sets the classify bit in every port CONTROL register. The host then unmasks the valid_signature event in the global EVENT_MASK register. The host then clears all the disable bits in the port CONTROL registers, allowing the ports to begin operation. The host then waits for an event, either by monitoring the global SRQ register, or by waiting for the /SMBINT to be asserted. Once an event occurs, the host can read the global SRQ register to figure out which port the event occurred on, then read that port's EVENT register to make sure it was a valid_signature event that occurred on that port (the host may have chosen to unmask other events besides valid_signature). The host then reads the port's STATUS register to find out what level of classification the PD presented to the PSE. The host can then decide if it has enough power available to power up this port at that classification level. If the host decides to not to power up the port, then nothing further needs to be done.

If the host does decide to power the port, then it must clear the classify_and_deny bit in the port's OPTION register. The next time this port is serviced, it will repeat detection and classification, and power up the port. The host can monitor the port's STATUS register to see that the port gets powered up, then set the classify_and_deny bit in the port's OPTION register so that everything is ready to go for the next time a PD is plugged into this port.

Selection of Isolation Transformer

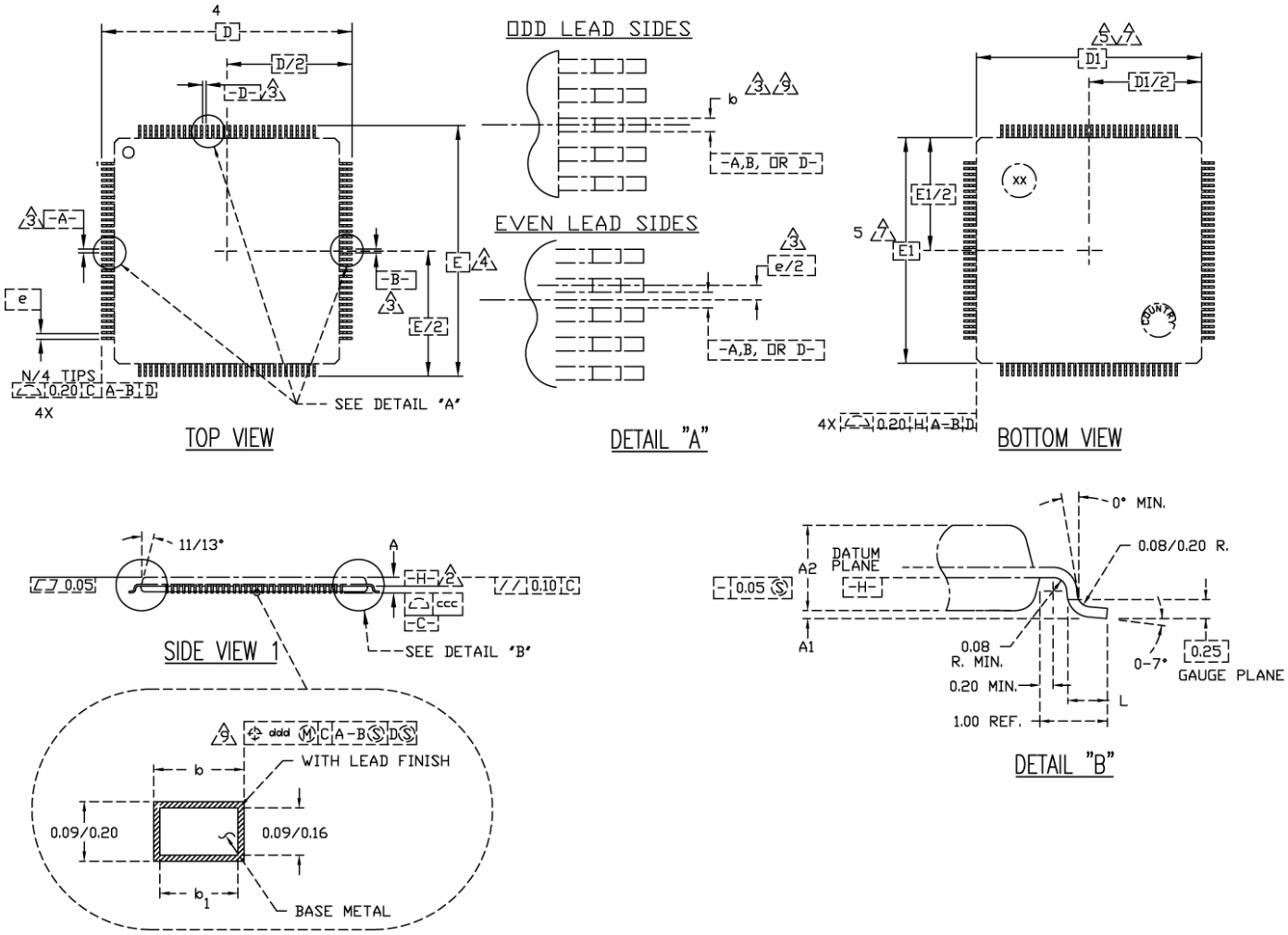
One simple 1:1 isolation transformer is needed at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements. The following table gives recommended transformer characteristics.

Characteristics Name	Value	Test Condition
Turns Ratio	1 CT : 1 CT	
Open-Circuit Inductance (min.)	350µH	100mV, 100kHz, 8mA
Leakage Inductance (max.)	0.4µH	1MHz (min.)
Inter-Winding Capacitance (max.)	12pF	
D.C. Resistance (max.)	0.9Ω	
Insertion Loss (max.)	1.0dB	0MHz to 65MHz
HIPOT (min.)	1500Vrms	

The following transformer vendors provide compatible PoE magnetic parts for Micrel's device:

Vendor	Part	Auto MDIX	Number of Ports
Pulse	H2019, H1197	Yes	1
Pulse	H2017	Yes	4
TDK	TAL-6T127LF(-T)	Yes	1

Package Information



64-Pin (10x10x1.4) LQFP (V)

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