CS-279

Floppy Disk Logic Circuit and Stepper Motor Driver

Description

Block Diagram

Q/S

The CS-279 is a floppy disk logic circuit with on chip bipolar stepper motor drivers and clamp diodes. It provides all the logic functions needed for a standard disk drive. The CS-279 is compatible with the CS-570, CS-3471/CS-3470A or other Read/Write circuits. The CS-279 incorporates Schmitt Trigger inputs for clean operation. The CS-279 also has high current open collector outputs capable of connecting directly back to the host computer or interface.

The three comparators on the circuit can be connected to photo sensors or switches to detect INDEX PULSES, TRACK-00 and WRITE PROTECTION. An on chip pull-down resistor provides a current path for the sensors so no additional components are necessary.

The Stepper Logic is capable of full or half stepping. An on chip, externally programmable one shot determines the

> ONE SHOT

> > RESE

RC₄

 RC_3

RC₂

INDEX

READ IN

WRTPRT

NWRTG1

NDS

STEP

TK00

RC₁

time delay for the ghost pulse. This can easily be defeated by grounding the one shot pin. The direction input allows the circuit to step the motor in or out. Two high current bridge outputs are provided and can be directly connected to the bipolar stepper motor. On chip diodes provide the protection needed for the IC. This bipolar stepper motor driver is capable of driving up to 275mA per phase. A power saving circuit is provided and may be used to reduce the power consumption when the motor has finished stepping. Three grounds have been used on the chip to eliminate cross-talk between the stepper driver and the rest of the circuit.

The CS-279 also has the necessary logic to inhibit the stepper circuit during the write mode. The write enable output only goes low when all the requirements of writing are met.

NPS

Gnd

NINDEX

NRDDAT

NWRPRT

NWF

Vcc

ACTLED

NTRK00

HGnd

 V_{DD}

LGnd

PH3 PH1

PH4

£

Features

Stepper Logic, Full or Half Stepping

On Chip Bipolar Stepper Motor Driver, Up to 275mA

On Chip Clamp Diodes

Power Saving Circuitry

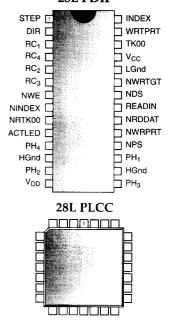
Direct Connection of Sensors: Such as INDEX, TRACK-00 and WRITE PROTECT

High Current Outputs for Direct Connection to the Host Controller

LED Output Driver, Active During Drive Select

Package Options

28L PDIP



CSC GHERRY &

Cherry Semiconductor Corporation 2000 South County Trail East Greenwich, Rhode Island 02818 Tel: (401)885-3600 Fax (401)885-5786 Telex WUI 6817157

Absolute Maximum Ratings

Logic Supply Voltage	7.0V
Analog Supply Voltage	
Input Voltage	0.3 to V_{CC} + 0.3V
Storage Temperature	40 to +150°C
Operating Temperature	0 to 70°C
Power Dissipation (Continuous, T _A = 50°C)	

Electrical Characteristics: $V_{CC} = 5.0V$;	$V_{SS} = 12.0V, T_A =$	= 25°C unless otherwise specified
		-

PARAMETER	TEST CONDITIONS			- MAX **	
■ DC Characteristics					
Logic Supply		4.5		5.5	V
Stepper Supply		4.0		13.2	V
Logic Current				150	mΑ
Stepper Supply	No load			75	mA
Rising Edge Schmitt Trip Point		1.4		2.0	V
Falling Edge Schmitt Trip Point		0.5		1.0	V
Schmitt Hysteresis		400		800	mV
High Level Schmitt Input Current	$V_{1N} = 2.7V$			20	μA
Low Level Schmitt Input Current	$V_{IN} = 0.4V$			-400	μA
Rising Comparator Trip Point		1.6		2.2	V
Falling Comparator Trip Poin	t	1.1		1.7	V
Comparator Hysteresis (Note	5)	200		400	mV
Comparator Pulldown (Note	5)	13.0		29.7	kΩ
Read in High Trip Point		2			V
Read in Low Trip Point				0.8	V
Read in High Level Input Current	$V_{IN} = 2.7V$			20	μΑ
Read in Low Level Input Current	$V_{IN} = 0.4V$			-1.6	mΑ
Open Collector Output High Leakage Current	$V_{OH} = 5V$			250	μА
Open Collector Output Voltage	$l_{O} = 40 \text{mA}$			0.4	V
NWE Output High Voltage	$I_{O} = -400 \mu A$	2.7	3.4		V
NWE Output Low Voltage	$I_{O} = 4mA$			0.4	V
Total Phase Output Saturation Voltage	$I_{OUT} = \pm 275 \text{mA}$			3.4	V
Positive Phase Clamp	$I_{OUT} = 275 \text{mA}$			2.0	V
Negative Phase Clamp	$I_{OUT} = -275 \text{mA}$	-2.0			V
■ AC Characteristics					
Power Save Pulse Width (Note 1)	$C4 = 0.1 \mu F$	30	50	125	ms
Index Pulse Width (Note 2)	R3 = 81k $C3 = 0.1 \mu f$	2.8		4.3	ms

Electrical Characteristics: continued					
PARAMETER	TEST CONDITIONS			越 沙雪	
■ AC Characteristics (continue	d)				
Index to Data Pulse Width (Note 3)	$R2 = 1.25k$ to $50k$; $C2 = 0.1\mu F$	50		2000	μs
Step One Shot Pulse Width (Note 4)	$R1 = 75k\Omega, C1 = 0.1\mu F$	2.4	3.0	3.6	ms
Read in Pulse		1			μs
NRDDAT Propogation Delay	V _{OUT} , Low to High V _{OUT} , High to Low			750 100	ns ns
Input Step Pulse Width		1			μs
V _{SS} & V _{CC} Supply Ripply	1Hz < f < 1MHz			100	mV

NOTES:

- 1. Minimum Pulse Width is specified over the operating temperature range.
- 2. Index Pulse Width is specified over the operating temperature range.
- 3. Index to Data Pulse Width shall remain within $\pm 50~\mu s$ of room temperature value over the temperature range of $10^{\circ}C$ to $46^{\circ}C$. Also the following equation is true: $0.320~RC \le PW \le 0.480~RC$.
- 4. Step One Shot Pulse Width shall not vary be more than $\pm 20\%$ over the temperature range of 10 C to 46°C. Grounding the RC₁ pin shall inhibit this function.
- 5. The input current at the positive threshold shall not vary more than 2000 PPM/°C over the normal operating range.

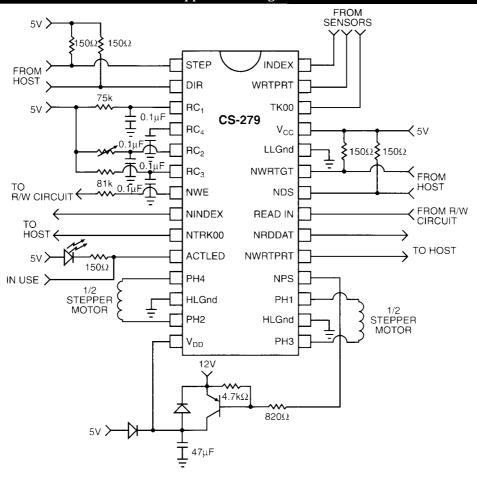
	Packag	ge Pin Description
PACKAGE PIN#	PIN SYMBOL	- FUNCTION
28L PDIP & 28L PLCC		
Input Pins		
26	TK00	TRACK 00 is a comparator input with hysterisis. An internal $22k\Omega$ pull down resistor is provided. A "0" on this input causes NTRK00 output to go low.
27	WRTPRT	WRITE PROTECT is a comparator input with hysteresis. An internal $22k\Omega$ pulldown resistor is provided. A "0" on this input causes NWE to go high and NWRPRT to go low.
23	NWRTGT	NOT WRITE GATE is a Schmitt trigger input. A "0" on this input disables the stepper circuitry and causes a "0" on the NWE output.
22	NDS	NOT DRIVE SELECT is a Schmitt trigger input. A "0" on this input enables the IC.
28	INDEX	INDEX is a comparator input with a $22k\Omega$ pulldown resistor provided. A positive transition on this input fires the RC ₂ oneshot. After RC ₂ times out the RC ₃ oneshot fires during which time the NINDEX goes low.
2	DIR	DIRECTION is a Schmitt trigger input. The polarity of this input determines the direction which the stepper motor moves. This signal is latched in by the step signal.
1	STEP	STEP input is a Schmitt input. The positive going trailing edge clocks the direction flip-flop, steps the stepper motor and triggers the stepper one shot.
21	READIN	READ INPUT input is a TTL input. A "1" on this input causes a low condition on the NRDDAT output.

Package Pin Description: continued

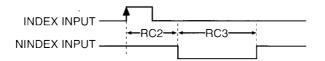
PACKAGE PIN# + #		FUNCTION
28L PDIP & 28L PLCC		
Input Pins (continued)		
3	RC ₁	RC_1 is the stepper one shot. This one shot shall trigger on the trailing edge of the step pulse. If RC_1 is grounded the one shot is inhibited.
5	RC_2	RC_2 is the Index to Data one shot. This one shot shall trigger on the leading edge of the Index pulse.
6	RC_3	RC_3 is the Index pulse width one shot. This one shot shall trigger on the trailing edge of the Index to Data one shot.
4	RC_4	RC_4 is the Power Save one shot. This one shot shall trigger on the trailing edge of the Step pulse.
25	V_{CC}	V_{CC} is the +5V supply voltage to the IC.
14	V_{DD}	V_{DD} is the +12V supply voltage to the stepper motor outputs.
12, 16	HGnd	HIGH GROUND High current output ground.
24	LGnd	LOW GROUND Low current logic ground.
Output Pins		
7	NWE	NOT WRITE ENABLE is a TTL type output. This output turns on when NWRTGT is a "0" and WRTPRT is a "1".
9	NRTK00	NOT TRACK 00 is a 40mA open collector output. This output is turned on when TK00 is a "0".
18	NPS	NOT POWER SAVE is a 40mA open collector output. This output is turned on when the Power Save one shot triggers during the step Pulse.
8	NINDEX	NOT INDEX is a 40mA open collector output. This output turns on when the Index Pulse Width one shot triggers.
10	ACTLED	THE ACTIVITY LED is a 30mA open collector output. This output turns on when the NDS input is low.
19	NWRPRT	NOT WRITE PROTECT is a 40mA open collector output. This output turns on when WRTPRT is low.
20	NRDDAT	NOT READ DATA is a 40mA open collector output. This output turns on when READIN is high.
17	PH_1	PHASE 1 is a 275mA push pull output. This output reflects the \overline{Q} of one of the stepper motor flip-flops.
13	PH_2	PHASE 2 is a 275mA push pull output. This output reflects the Q of one of the stepper motor flip-flops.
15	PH ₃	PHASE 3 is a 275mA push pull output. This output reflects the Q of one of the stepper motor flip-flops.
11	PH₊	PHASE 4 is a 275mA push pull output. This output reflects the \overline{Q} of one of the stepper motor flip-flops.

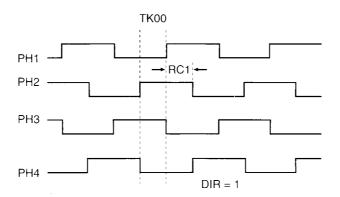






Timing Diagram

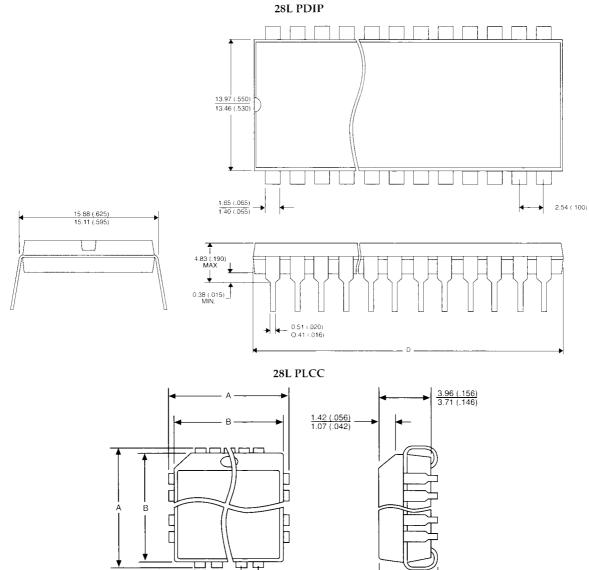




Package Specification

		D			
Lead Count	Met	ric	Eng	lish	
	Max	Min	Max	Min	
28 Lead PDIP	36.96	36.70	1.455	1.445	
28 Lead PLCC (A)	12.57	12.32	.495	.485	
28 Lead PLCC (B)	11.53	11.43	.454	.450	

	PAC	KAGE THERM	AL DATA	
Therma	l Data	28L PDIP	28L PLCC	
$R\Theta_{JC}$	typ	23	18	°C/W
$R\Theta_{JA}$	typ	55	70	°C/W



Ondania molination

Part Number Description CS-279N28 28 Lead PDIP CS279FN28 28 Lead PLCC



Cherry Semiconductor Corporation 2000 South County Trail East Greenwich, Rhode Island 02818 Tel: (401)885-3600 Fax (401)885-5786 Telex WUI 6817157