CIRRUS LOGIC®

CL-CR3410

Product Bulletin

ATAPI (ATA Packet Interface) CD-ROM Decoder

FEATURES

- **General**
  - Fully compatible with the ATAPI Specification SFF-8020, Revision 1.2
  - All ATAPI commands supported
  - ATAPI command and control registers contained in the CL-CR3410 register set
  - Designed for easy and efficient firmware programming
  - Pinout organized for optimum board layout efficiency
  - Low-power, highly efficient 0.6 micron CMOS technology
  - Automatic power-down on interfaces when idle
  - 100-pin PQFP package
- **CD-ROM DSP Interface**
  - Supports Sony-Philips® CD-ROM, CD-I, and CD-DA™ (CD-Digital Audio) formats
  - Supports various compact disc DSP (digital signal processor) controllers
    Supports disc speeds up to 25-MHz MCLK
  - Supports programmable pseudo-sync-mark insertion for CD-ROM sector synchronization
  - Supports automatic target sector header search for CD-ROM
  - Sector header validity check is done by hardware during data transfer
  - Realtime CD-ROM layered ECC error correction with programmable number of sets of P-word and Q-word corrections per sector (up to 64 total)

(cont.)

OVERVIEW

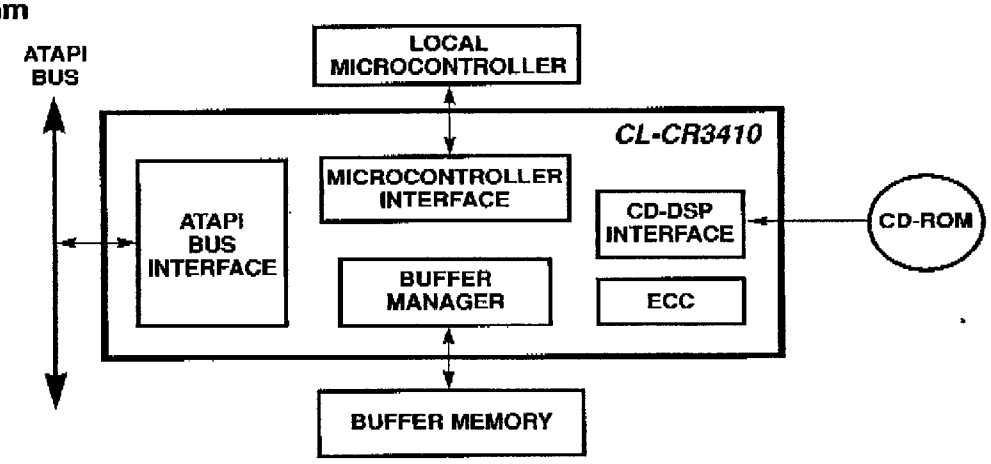
ATAPI (AT Attachment Packet Interface) was developed by the ATA Small Form Factor Committee to provide an inexpensive method for interfacing a CD-ROM drive to an ATA host computer without the need for a separate host adapter. ATAPI is an extension of the standard IDE/ATA interface, which permits a CD-ROM to share the ATA bus of the host computer with existing ATA hard disk drives.

The CL-CR3410 is Cirrus Logic's high-performance ATAPI CD-ROM decoder. It is configured with an external buffer memory (SRAM or DRAM), and a local microcontroller, and system RAM and ROM to create a complete controller.

The ATAPI host interface is designed for full compliance with the ATAPI specification. The ATAPI Command and

(cont.)

Functional Block Diagram



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FEATURES (cont.)

- **CD-ROM Interface** *(cont.)*
  - — Supports realtime subcode error correction in CD-DA™ mode
  - — Supports serial DSP programming interface
- **ATAPI Host Interface**
  - — True realtime hardware/software ATAPI compatibility
  - — Hardware implementation of:
    - ATAPI packet command
    - ATAPI reset command
  - — Automated protocol control on block data transfers for ATAPI read/write commands
  - — Direct interface to ATAPI bus with programmable 12- or 24-mA drivers
  - — Supports any host speed with programmable and automatic wait-state generation
  - — FIFOs synchronize buffer RAM access with the host bus and the DSP data transfer
  - — Provision for daisy-chaining two ATA- or ATAPI-embedded drives
- **High-Performance**
  - — PIO/DMA ATAPI bus transfer rate:
    - PIO modes 3 and 4 and DMA modes 1 and 2
  - — CD-DSP data transfer rate:
    - up to 8x drive speed
  - — Buffer bandwidth:
    - 14 Mbytes per second with DRAM
    - 20 Mbytes per second with SRAM
- **Buffer Manager**
  - — Dual-port circular buffer control with access-priority resolver
  - — Direct addressing of up to 64 Kbytes of SRAM or up to 4 Mbytes of DRAM
  - — Supports 4-bit mode for single 4-bit DRAM chip solution
  - — Optional buffer memory parity for data integrity
  - — Supports variable buffer segmentation
  - — Programmable timing control for SRAM/DRAM
  - — Host overrun control
- **Microcontroller Interface**
  - — Supports high-speed Intel®- and Motorola®-type microcontrollers, such as the 8051 or 68HC11
  - — Supports nonmultiplexed and multiplexed address and data buses
  - — Interrupt- or polled-microcontroller interface
  - — Microcontroller access to six external switch settings on the buffer bus
  - — Three-level power-down capability when idle, automatic power-up when command is received

OVERVIEW (cont.)

Control Block registers are contained in the CL-CR3410 register set, which allow both host and local microcontroller access. The CL-CR3410 supports some ATAPI protocols by hardware without microcontroller intervention. The host interface logic includes integrated 12/24-mA switchable drivers for the ATAPI interface data signals. The CL-CR3410 supports PIO modes 3 and 4 and DMA modes 1 and 2, allowing faster transfer (as defined by the ATA-2 standard).

The buffer manager controls the flow of data between the host and DSP interfaces. These interfaces store and retrieve data to/from the external buffer memory using interleaved access cycles. The actual buffer memory may be implemented with static or dynamic RAM devices. The buffer manager is programmable to provide all the necessary address and control signals for RAM devices of varying access times and memory configurations. Up to 64 Kbytes of SRAM or 4 Mbytes of DRAM can be directly addressed by the CL-CR3410. A 4-bit buffer memory mode is also available, allowing the use of a single ×4 DRAM for low-cost buffer memory implementations.

The CL-CR3410 DSP interface supports various CD-ROM DSPs (digital signal processors) from various manufacturers. The DSP interface includes three types of interface signals: the main data channel signals, subcode channel signals, and serial DSP programming signals. The CL-CR3410 supports realtime layered ECC correction, which is programmable for up to 64 P/Q-word corrections per sector. All ECC correction, including erasure pointer correction, is achieved without microcontroller intervention, reducing firmware overhead and complexity, and minimizing microcontroller performance requirements. Also, subcode R-W correction is supported in the CD-DA™ mode.

ADVANTAGES

Unique Features	*Benefits*
■ Fully compatible with the SFF-8020, Revision 1.2 ATAPI Specification	❒ All ATAPI commands supported
■ CD-to-DSP data transfer rates up to 8× drive speed	❒ Supports CD-ROM speeds above current industry requirements
■ Supports Sony-Philips® CD-ROM, CD-I, and CD-DA™ formats	❒ Can be used in all implementations of CD technology
■ Supports automatic target sector header search for CD-ROM	❒ Automates header search/validity check, which improves performance and reduces firmware requirements
■ Sector header validity check is done by hardware during data transfer	
■ Realtime ECC correction (up to 64 P/Q-word corrections/sector) and Erasure Pointer correction, with no microcontroller intervention	❒ Improves system performance, reduces firmware overhead and microcontroller performance requirements, and improves reliability and correction capability
■ Realtime subcode error correction in CD-DA™ mode	❒ Exceeds advanced ECC requirements of state-of-the-art CD-ROM designs for a variety of media/performance combinations
■ Supports ATA PIO Mode 4 and DMA Mode 2 transfers	❒ Enables transfer rates of the highest performance systems
■ Three-level power-down capability when idle, automatic power-up when command is received	❒ Exceeds low-power requirements of leading-edge CD-ROM drives
■ Automated ATAPI packet and reset commands	❒ Improves system performance, lowers firmware overhead

System Block Diagram