ACT™ 3 Field Programmable Gate Arrays

Preliminary

Features

- Highly Predictable Performance with 100% Automatic Placement and Routing
- 9 ns Clock-to-Output Times
- Up to 150 MHz On-Chip Performance
- Up to 228 User-Programmable I/O Pins
- Four Fast, Low-Skew Clock Networks
- More Than 500 Macro Functions
- Up to 10,000 Gate Array Equivalent Gates (up to 25,000 equivalent PLD Gates)
- Replaces up to 250 TTL Packages
- Replaces up to 100 20-pin PAL® Packages
- Up to 1153 Dedicated Flip-Flops
- I/O Drive to 12 mA
- PQFP, PLCC, and CPGA Packages
- Nonvolatile, User Programmable
- Low-power 0.8 µm CMOS Technology
- Fully Tested Prior to Shipment

Description

The ACT 3 family, based on Actel's proprietary PLICE® antifuse technology and 0.8-micron double-metal, double-poly CMOS process, offers a high-performance programmable solution capable of 150 MHz on-chip performance and 9 nanosecond clock-to-output speeds. The ACT 3 family spans capacities from 1,500 to 10,000 gate array equivalent gates (up to 25,000 PLD gates), and offers very high pin-to-gate ratios, with up to 228 user I/Os for 10,000 gate designs.

Predictable Performance* (Worst-Case Commercial)	
Accumulators (16-bit)	46–47 MHz
Loadable Counters (16-bit)	76–82 MHz
Prescaled Loadable Counters (16-bit)	127–145 MHz
Shift Registers	150–150 MHz

*See page 1-82 for further details.

1

Product Family Profile

Device	A1415A	A1425A	A1440A	A1460A	A14100A
Capacity					
Gate Array Equivalent Gates	1,500	2,500	4,000	6,000	10,000
PLD Equivalent Gates	3,750	6,250	10,000	15,000	25,000
TTL Equivalent Packages (40 gates)	40	60	100	150	250
20-Pin PAL Equivalent Packages (100 gates)	15	25	40	60	100
Logic Modules	200	310	564	848	1,377
S-Module	104	160	288	432	697
C-Module	96	150	276	416	680
Dedicated Flip-Flops[1]	264	360	568	768	1,153
User I/Os (maximum)	80	100	140	168	228
Packages[2]					
CPGA	100-pin	133-pin	175-pin	207-pin	257-pin
PLCC	84-pin	84-pin	—	—	—
PQFP	100-pin	100-pin 160-pin	160-pin	208-pin	TBD
Performance[3] (maximum, worst-case commercial)					
Chip-to-Chip[4]	83 MHz	83 MHz	77 MHz	75 MHz	72 MHz
Accumulators (16-bit)	47 MHz	47 MHz	47 MHz	47 MHz	47 MHz
Loadable Counter (16-bit)	82 MHz	82 MHz	82 MHz	80 MHz	80 MHz
Prescaled Loadable Counters (16-bit)	145 MHz	145 MHz	145 MHz	115 MHz	115 MHz
Shift Registers	150 MHz	150 MHz	150 MHz	120 MHz	120 MHz
I/O, Clock-to-Output	10 ns	10 ns	11 ns	11.6 ns	12 ns
CMOS Process	0.8 µm	0.8 µm	0.8 µm	0.8 µm	0.8 µm

Notes:

1. One flip-flop per S-Module, two flip-flops per I/O-Module.
2. See product plan on page 1-84 for package availability.
3. Based on A1425A-1 device.
4. Clock-to-Output + Setup

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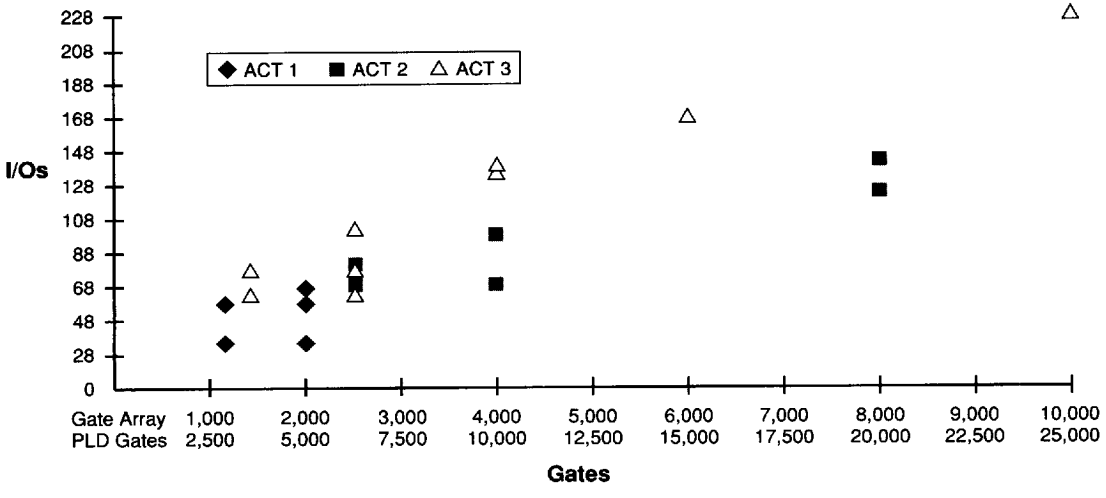
The ACT 3 family represents the third generation of Actel Field Programmable Gate Arrays (FPGAs). The family improves on the proven ACT 2 family two-module architecture, consisting of combinatorial and sequential-combinatorial logic modules. The ACT 3 family offers registered I/O modules delivering 9 ns clock-to-out times. The devices contain four clock distribution networks, including dedicated array and I/O clocks, supporting very fast synchronous and asynchronous designs. In addition, routed clocks can be used to drive high fanout signals like resets or output enables, reducing buffering requirements.

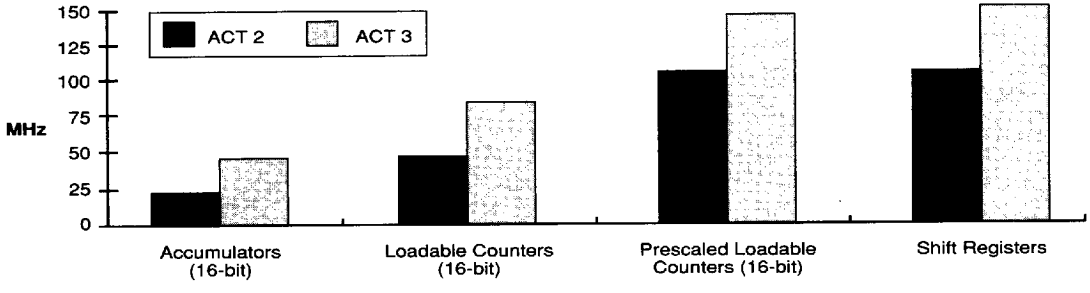
The ACT 3 family is supported by the Designer and Designer Advantage systems, which offers automatic or fixed pin assignment, automatic placement and routing with optional manual placement, timing analysis, user programming, and diagnostic probe capabilities. The system is supported on the following platforms: 386/486™ PC, Sun™ Microsystems, and HP™ workstations. The software provides CAE interfaces to Cadence, Mentor Graphics®, OrCAD™ and Viewlogic® design environments. Additional platforms and CAE interfaces are supported through Actel's Industry Alliance Program, including the CAD/CAM Group, DATA I/O® (ABEL™ FPGA), DAZIX, and MINC.

With the introduction of ACT 3, Actel extends its line of programmable devices. The ACT 1 family offers up to 2,000 gate array equivalent gates (to 6,000 PLD equivalent gates) at industry leading price-to-gate ratios. The ACT 2 family advances this price leadership into higher speed, higher I/O applications requiring 2,500 to 8,000 gate array equivalent gates (to 20,000 PLD equivalent gates). The ACT 3 family offers very high speed with very high I/O-to-gate ratios for designs requiring from less than 1,500 to 10,000 gate array equivalent gates (to 25,000 PLD equivalent gates).

Actel Families: Gates Versus I/Os



Performance: ACT 3 Versus ACT 2 (Standard-Speed Devices)



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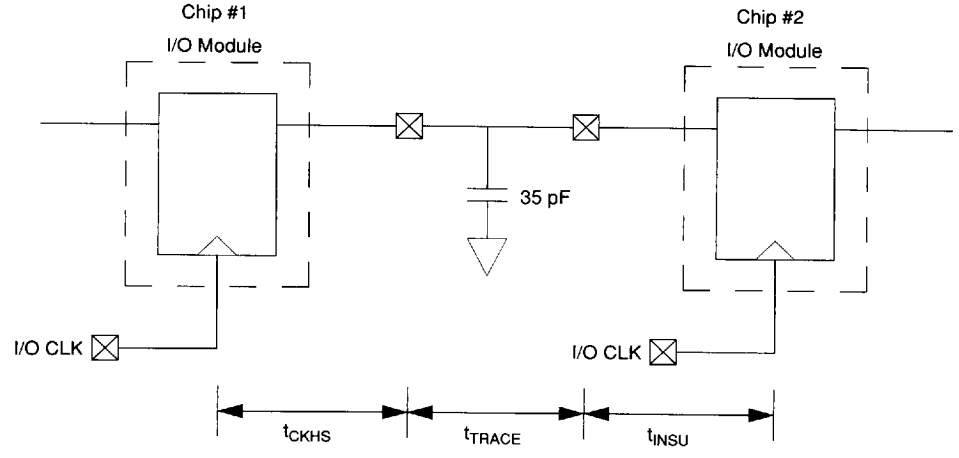
Chip-to-Chip Performance



Chip-to-Chip Performance (Worst-Case Commercial)

	t_{CKHS}	t_{TRACE}	t_{INSU}	Total	MHz
A1425A-1	9.0	1.0	3.0	13.0 ns	77
A1460A-1	10.4	1.0	3.0	14.4 ns	69

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ACT 3 PREP Performance Examples

The ACT 3 family offers very high system performance. Typical application design building blocks have been developed and implemented to estimate and report ACT 3 system performance. These building blocks have been routed in multiple instances, replicated to fill a device in a step and repeat fashion. The average, minimum, and maximum performances were then determined, giving a realistic estimate of achievable performance. ACT 3 performance is very predictable, as observed by the small spread between maximum and minimum performance. The step and repeat methodology is illustrated in Figure 1.

16-bit Shift Registers

The 16-bit Shift Register Example is a parallel loadable shift register with clear, shift enable, serial in, and serial out. It is replicated by connecting parallel data in to parallel data out, and serial data in to serial data out.

16-bit Prescaled Counters

The 16-bit Prescaled Counter Example is a very high-speed loadable counter optimized for counting. The load requires multiple clock cycles (four), but counting and holding occur at the full clock rate. This counter is ideal for address generation and high-speed timing applications. It is replicated by connecting data inputs to data outputs.

16-bit Non-Prescaled Counters

The Non-Prescaled 16-bit Counter Example is the more traditional 16-bit loadable counter, where loading, counting, and hold all occur at the same clock rate. It is replicated by connecting inputs to counter outputs.

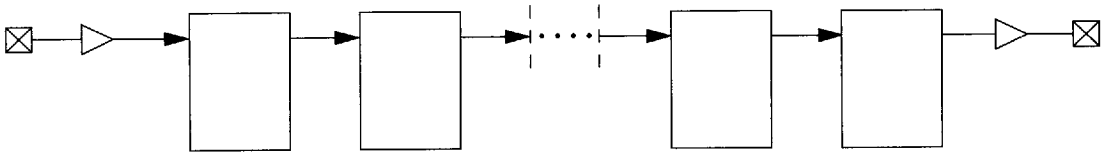
16-bit Accumulators

The 16-bit Accumulator adds a 16-bit number to the previous output value. It is replicated by connecting the data output to the data input.

Performance Results

These designs were completed using Actel's 100% automatic place and route software. No manual placement or routing was used when completing these designs. The performance measurements reflect worst-case commercial conditions.

Table 1 below presents the performance results for each design in minimum, maximum, and average measurements. The table also shows the number of design iterations completed within the device. Notice the tight distribution between minimum and maximum performance, in all cases within 1 ns, and in all cases automatic place and route was used exclusively.



- Step and Repeat Methodology
- Fully Utilized Device
- 100% Automatic Placement and Routing
- No Manual Placement or Routing

Figure 1. Layout of Performance Examples

Table 1. A1425A-1 Performance Results: Worst-Case Commercial Conditions

Design	Iterations	Performance		
		Minimum	Maximum	Average
16-bit Shift Registers	10	150 MHz	150 MHz	150 MHz
16-bit Prescaled Counters	3	127 MHz	145 MHz	134 MHz
16-bit Non-Prescaled Counters	6	76 MHz	82 MHz	80 MHz
16-bit Accumulators	3	46 MHz	47 MHz	47 MHz

Note:
For more information on the PREP Benchmarks, see Section 2 of this data book.

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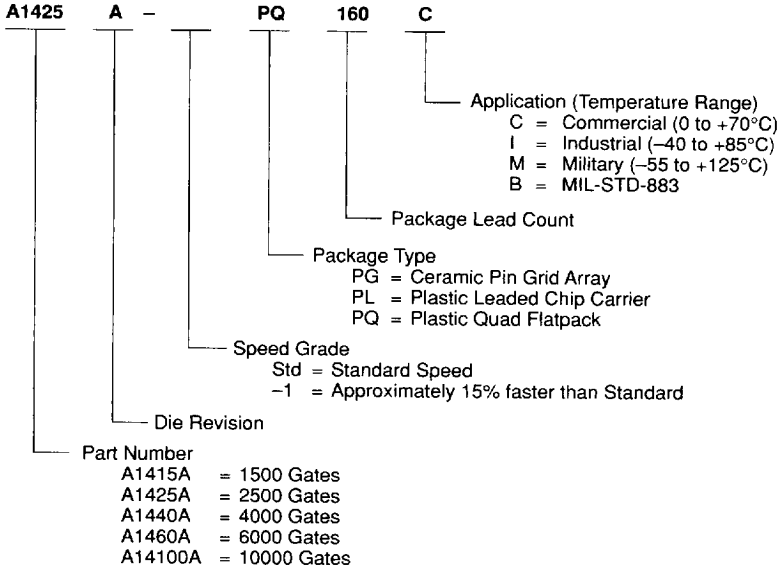
Ordering Information



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Product Plan[1]

	Speed Grade*		Application				
	Std	–1	C	I	M	B	E
A1415A Device							
84-pin Plastic Leaded Chip Carrier (PL)	P	P	P	P	—	—	—
100-pin Plastic Quad Flatpack (PQ)	P	P	P	P	—	—	—
100-pin Ceramic Pin Grid Array (PG)	P	P	P	—	—	—	—
A1425, A1425A Devices							
84-pin Plastic Leaded Chip Carrier (PL)	✔	✔	✔	✔	—	—	—
100-pin Plastic Quad Flatpack (PQ)	✔	✔	✔	✔	—	—	—
133-pin Ceramic Pin Grid Array (PG)	✔	✔	✔	—	P	P	—
160-pin Plastic Quad Flatpack (PQ)	✔	✔	✔	✔	—	—	—
A1440A Device							
160-pin Plastic Quad Flatpack (PQ)	P	P	P	P	—	—	—
175-pin Ceramic Pin Grid Array (PG)	P	P	P	—	—	—	—
A1460A Device							
207-pin Ceramic Pin Grid Array (PG)	✔	P	✔	—	P	P	—
208-pin Plastic Quad Flatpack (PQ)	✔	P	✔	P	—	—	—
A14100A Device							
257-pin Ceramic Pin Grid Array (PG)	P	P	P	—	P	P	—

Applications: C = Commercial, I = Industrial, M = Military, B = MIL-STD-883, E = Extended Flow

Availability: ✔ = Available, P = Planned, — = Not Planned

* Speed Grade: –1 = 15% faster than Standard

Note:

1. Availability as of January 1993. Please consult Actel Representatives for current availability.

Device Resources

			User I/Os								
			PLCC	PQFP			CPGA				
Device Series	Logic Modules	Gates	84-pin	100-pin	160-pin	208-pin	100-pin	133-pin	175-pin	207-pin	257-pin
A1415A	200	1500	70	80	—	—	80	—	—	—	—
A1425A	310	2500	70	80	100	—	—	100	—	—	—
A1440A	564	4000	—	—	130	—	—	—	140	—	—
A1460A	848	6000	—	—	—	167	—	—	—	168	—
A14100A	1377	10000	—	—	—	—	—	—	—	—	228

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Pin Description

CLKA **Clock A (Input)**

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

CLKB **Clock B (Input)**

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK **Diagnostic Clock (Input)**

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND **Ground**

LOW supply voltage.

HCLK **Dedicated (Hard-wired) Array Clock (Input)**

TTL Clock input for sequential modules. This input is directly wired to each S-Module and offers clock speeds independent of the number of S-Modules being driven. This pin can also be used as an I/O.

I/O **Input/Output (Input, Output)**

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW by the ALS software.

IOCLK **Dedicated (Hard-wired) I/O Clock (Input)**

TTL Clock input for I/O modules. This input is directly wired to each I/O module and offers clock speeds independent of the number of I/O modules being driven. This pin can also be used as an I/O.

IOPCL **Dedicated (Hard-wired) I/O Preset/Clear (Input)**

TTL input for I/O preset or clear. This global input is directly wired to the preset and clear inputs of all I/O registers. This pin functions as an I/O when no I/O preset or clear macros are used.

MODE **Mode (Input)**

The MODE pin controls the use of diagnostic pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os.

NC **No Connection**

This pin is not connected to circuitry within the device.

PRA **Probe A (Output)**

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB **Probe B (Output)**

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is accessible when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDI **Serial Data Input (Input)**

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

V_{CC} **5 V Supply Voltage**

HIGH supply voltage.

V_{KS} **Programming Voltage**

Supply voltage used for device programming. This pin must be connected to GND during normal operation.

V_{PP} **Programming Voltage**

Supply voltage used for device programming. This pin must be connected to V_{CC} during normal operation.

V_{SV} **Programming Voltage**

Supply voltage used for device programming. This pin must be connected to V_{CC} during normal operation.

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Architecture

This section of the data sheet is meant to familiarize the user with the architecture of the ACT 3 family of FPGA devices. A generic description of the family will be presented first, followed by a detailed description of the logic blocks, the routing structure, the antifuses, and the special function circuits. The on-chip circuitry required to program the devices is not covered.

Topology

The ACT 3 family architecture is composed of six key elements: Logic modules, I/O modules, I/O Pad Drivers, Routing Tracks, Clock Networks, and Programming and Test Circuits. The basic structure is similar for all devices in the family, differing only in the number of rows, columns, and I/Os. The array itself consists of alternating rows of modules and channels. The logic modules and channels are in the center of the array; the I/O modules are located along the array periphery. A simplified floor plan is depicted in Figure 2.

Logic Modules

ACT 3 logic modules are enhanced versions of the ACT 2 family logic modules. As in the ACT 2 family, there are two types of modules: C-modules and S-modules. The C-module is functionally equivalent to the ACT 2 C-module and implements high fanin combinatorial macros, such as 5-input AND, 5-input OR, and so on. It is available for use as the CM8 hard macro. The S-module is designed to implement high-speed sequential functions within a single module. S-modules consist of a full C-module driving a flip-flop, which allows an additional level of logic to be implemented without additional propagation delay. It is available for use as the DFM8A/B and DLM8A/B hard macros. C-modules and S-modules are arranged in pairs called module-pairs. Module-pairs are arranged in alternating patterns and make up the bulk of the array. This arrangement allows the placement software to support two-module macros of four types (CC, CS, SC, and SS). The C-module implements the following function:

$$Y = !S1 * !S0 * D00 * !S1 * S0 + D01 * S1 * !S0 * D10 + S1 * S0 * D11$$

where: $S0 = A0 * B0$ and $S1 = A1 + B1$

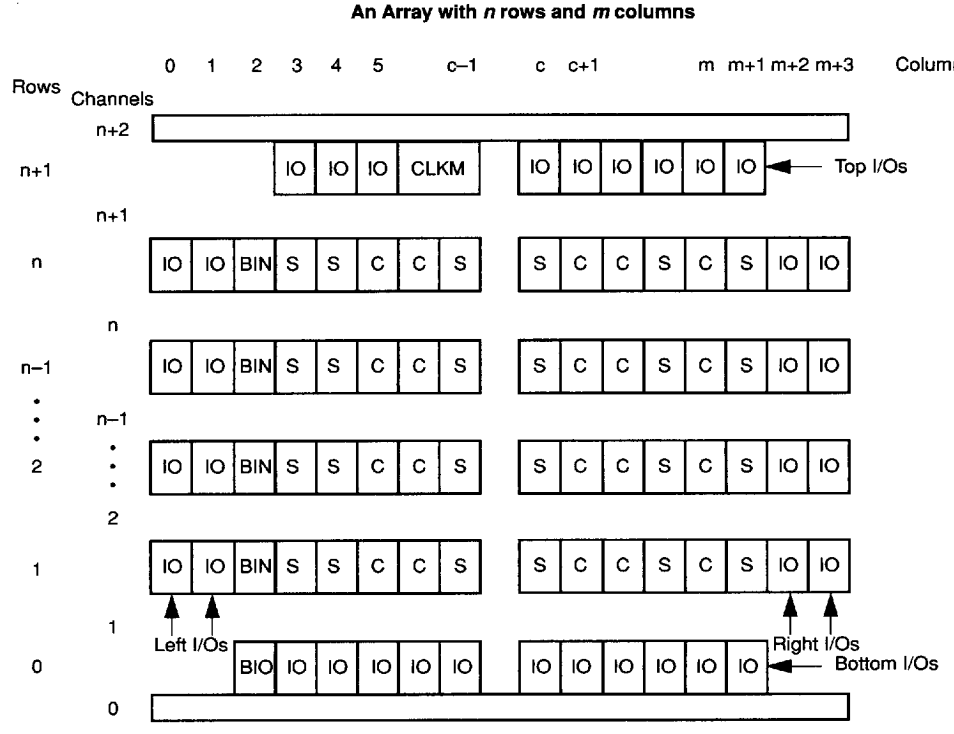

Figure 2. Generalized Floor Plan of ACT 3 Device

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The S-module contains a full implementation of the C-module plus a clearable sequential element that can either implement a latch or flip-flop function. The S-module can therefore implement any function implemented by the C-module. This allows complex combinatorial-sequential functions to be implemented with no delay penalty. The Action Logic System will automatically combine any C-module macro driving an S-module macro into the S-module, thereby freeing up a logic module and eliminating a module delay.

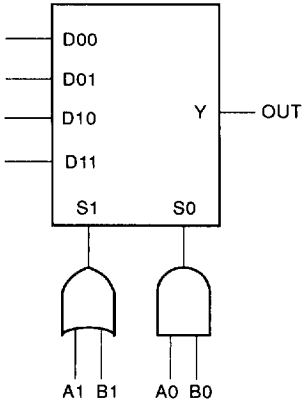

Figure 3. C-Module Diagram

The clear input CLR is accessible from the routing channel. In addition, the clock input may be connected to one of three clock networks: CLK0, CLK1, or HCLK. The C-module and S-module functional descriptions are shown in Figures 3 and 4. The clock selection multiplexor selects the clock input to the S-module.

I/Os

I/O Modules

I/O modules provide an interface between the array and the I/O Pad Drivers. I/O modules are located in the array and access the routing channels in a similar fashion to logic modules. There are two types of I/O modules: side and top/bottom. The I/O module schematic is shown in Figure 5. UO1 and UO2 are inputs from the routing channel, one for the routing channel above and one for the routing channel below the module. The top/bottom I/O modules interact with only one channel and therefore have only one UO input. The signals DataIn and DataOut connect to the I/O pad driver. Each I/O module contains two D-type flip-flops. Each flip-flop is connected to the dedicated I/O clock (IOCLK). Each flip-flop can be bypassed by nonsequential I/Os. In addition, each flip-flop contains a data enable input that can be accessed from the routing channels (ODE and IDE). The asynchronous preset/clear input is driven by the dedicated preset/clear network (IOPCL). Either preset or clear can be selected individually on an I/O module by I/O module basis.

The I/O module output Y is used to bring Pad signals into the array *or* to feed the output register back into the array. This allows the output register to be used in high-speed state machine applications. Side I/O modules have a dedicated output segment for Y extending into the routing channels above and below

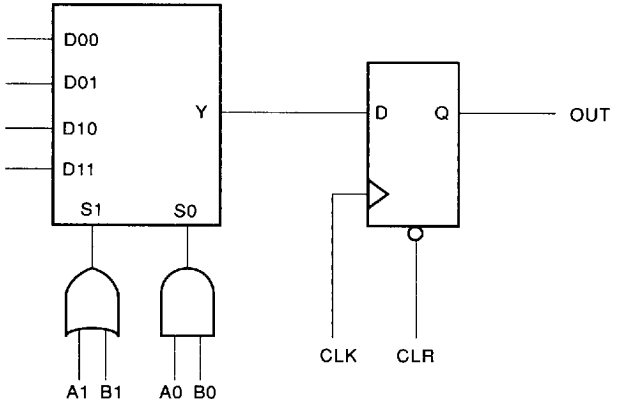

Figure 4. S-Module Diagram

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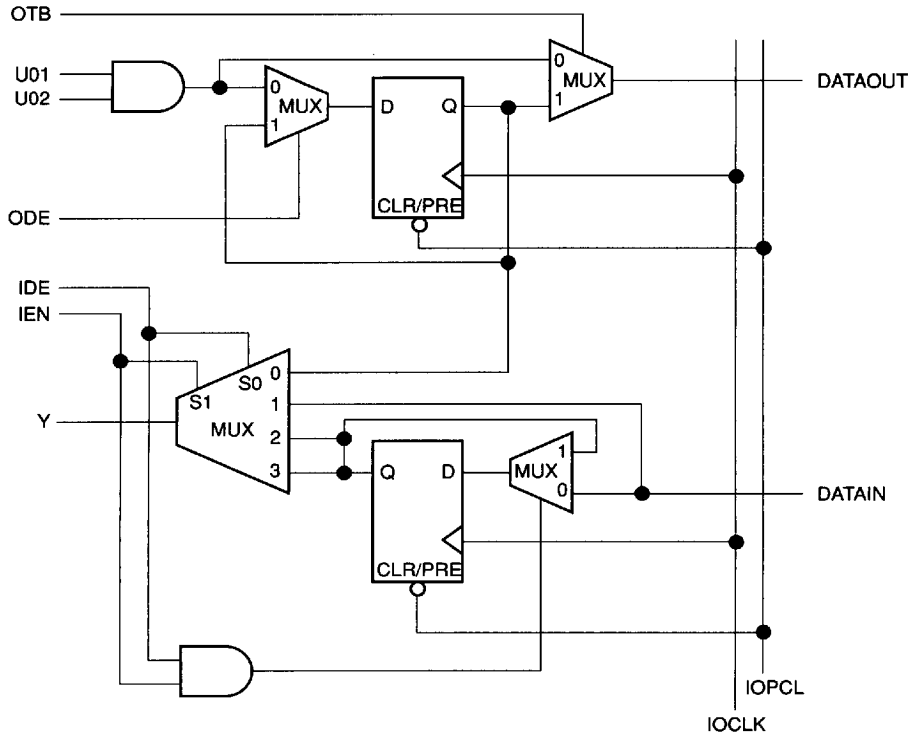

Figure 5. Functional Diagram for I/O Module

(similar to logic modules). Top/Bottom I/O modules have no dedicated output segment. Signals coming into the chip from the top or bottom are routed using F-fuses and LVTs (F-fuses and LVTs are explained in detail in the routing section).

I/O Pad Drivers

All pad drivers are capable of being tristate. Each buffer connects to an associated I/O module with four signals: OE (Output Enable), IE (Input Enable), DataOut, and DataIn. Certain special signals used only during programming and test also connect to the pad drivers: OUTEN (global output enable), INEN (global input enable), and SLEW (individual slew selection). See Figure 6.

Special I/Os

The special I/Os are of two types: temporary and permanent. Temporary special I/Os are used during programming and testing. They function as normal I/Os when the MODE pin is inactive. Permanent special I/Os are user programmed as either normal I/Os or special I/Os. Their function does not change once the device has been programmed. The permanent special I/Os consist of the array clock input buffers (CLKA and CLKB), the hard-wired array clock input buffer (HCLK), the hard-wired I/O clock input buffer (IOCLK), and the hard-wired I/O register preset/clear input buffer (IOPCL). Their function is determined by the I/O macros selected.

Clock Networks

The ACT 3 architecture contains four clock networks: two high-performance dedicated clock networks and two general purpose routed networks. The high-performance networks function up to 150 MHz, while the general purpose routed networks function up to 75 MHz.

Dedicated Clocks

Dedicated clock networks support high performance by providing sub-nanosecond skew and guaranteed performance. Dedicated clock networks contain no programming elements in the path from the I/O Pad Driver to the input of S-modules or I/O modules. There are two dedicated clock networks: one for the array registers (HCLK), and one for the I/O registers (IOCLK). The clock networks are accessed by special I/Os.

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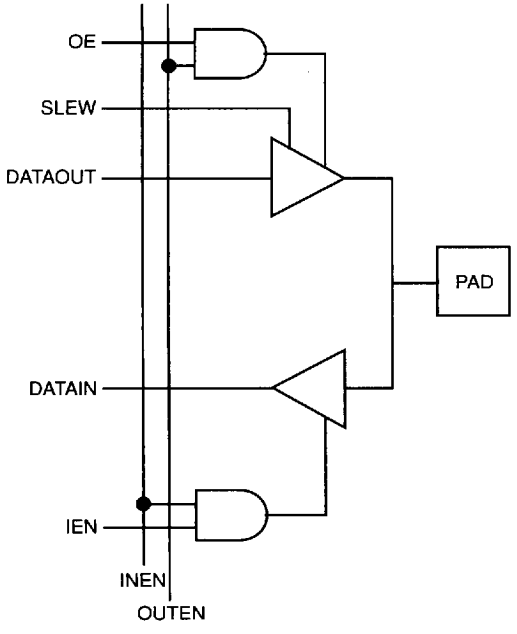

Figure 6. Function Diagram for I/O Pad Driver

Routed Clocks

The routed clock networks are referred to as CLK0 and CLK1. Each network is connected to a clock module (CLKMOD) that selects the source of the clock signal and may be driven as follows (see Figure 7):

- externally from the CLKA pad
- externally from the CLKB pad
- internally from the CLKINA input
- internally from the CLKINB input

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel. The function of the clock module is determined by the selection of clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an internally generated clock signal to a clock network. Since both clock networks are identical, the user does not care whether CLK0 or CLK1 is being used. Routed clocks can also be used to drive high fanout nets like resets, output enables, or data enables. This saves logic modules and results in performance increases in some cases.

Routing Structure

The ACT 3 architecture uses vertical and horizontal routing tracks to connect the various logic and I/O modules. These routing tracks are metal interconnects that may either be of continuous length or broken into segments. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track.

Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module-pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 8. Undedicated horizontal routing tracks are used to route signal nets. Dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.

Vertical Routing

Other tracks run vertically through the modules. Vertical tracks are of three types: input, output, and long. Vertical tracks are also divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module. Each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. LVTs contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 9.

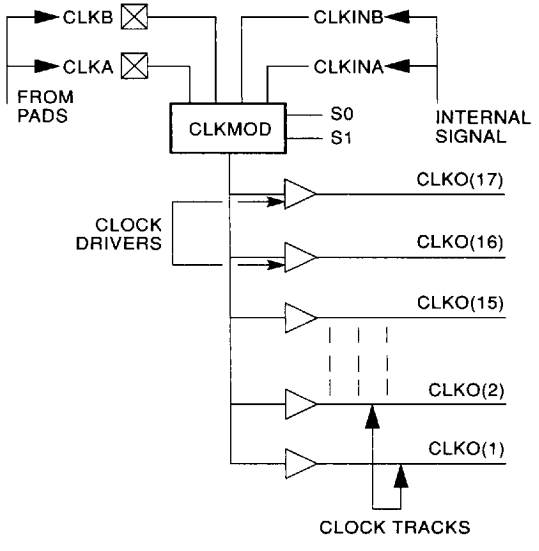

Figure 7. Clock Networks

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Antifuse Connections

An antifuse is a "normally open" structure as opposed to the normally closed fuse structure used in PROMs or PALs. The use of antifuses to implement a programmable logic device results in highly testable structures as well as an efficient programming architecture. The structure is highly testable because there are no preexisting connections; temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed as well as isolate individual circuit structures to be tested. This can be done both before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Four types of antifuse connections are used in the routing structure of the ACT 3 array. (The physical structure of the antifuse is identical in each case; only the usage differs.) Table 2 shows four types of antifuses.

Table 2. Antifuse Types

XF	Horizontal-to-Vertical Connection
HF	Horizontal-to-Horizontal Connection
VF	Vertical-to-Vertical Connection
FF	"Fast" Vertical Connection

Examples of all four types of connections are shown in Figure 8 and Figure 9.

Module Interface

Connections to Logic and I/O modules are made through vertical segments that connect to the module inputs and outputs. These vertical segments lie on vertical tracks that span the entire height of the array.

Module Input Connections

The tracks dedicated to module inputs are segmented by pass transistors in each module row. During normal user operation, the pass transistors are inactive, which isolates the inputs of a module from the inputs of the module directly above or below it. During certain test modes, the pass transistors are active to verify the continuity of the metal tracks. Vertical input segments span only the channel above or the channel below. The logic modules are arranged such that half of the inputs are connected to the channel above and half of the inputs to segments in the channel below as shown in Figure 10.

Module Output Connections

Module outputs have dedicated output segments. Output segments extend vertically two channels above and two channels below, except at the top or bottom of the array. Output segments twist, as shown in Figure 10, so that only four vertical tracks are required.

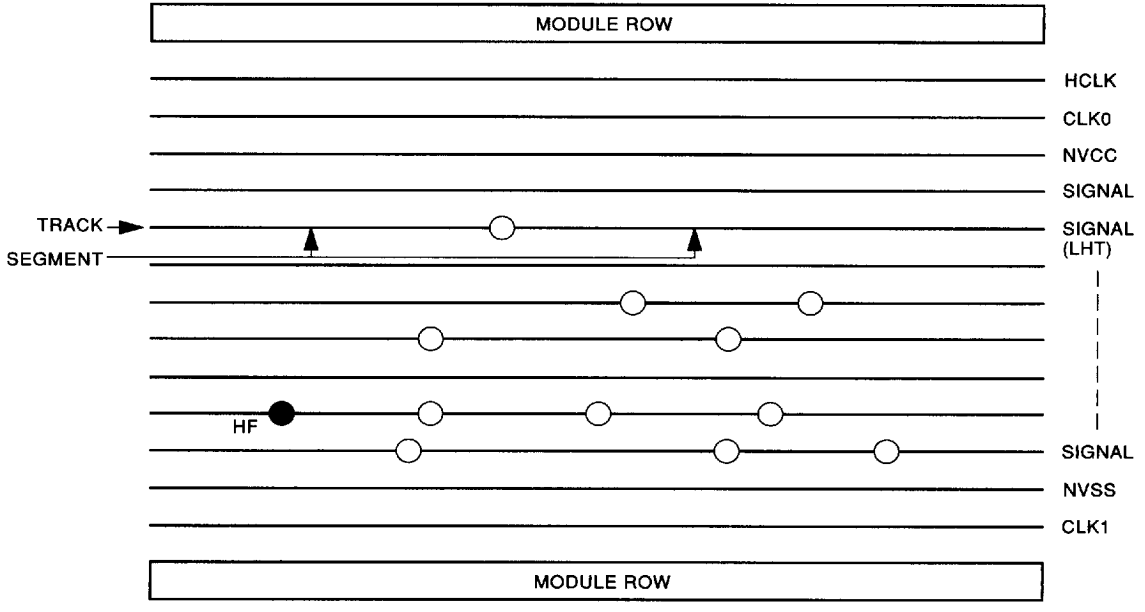

Figure 8. Horizontal Routing Tracks and Segments

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LVT Connections

Outputs may also connect to nondedicated segments called Long Vertical Tracks (LVTs). Each module pair in the array shares four LVTs that span the length of the column. Any module in the column pair can connect to one of the LVTs in the column using an FF connection. The FF connection uses antifuses connected directly to the driver stage of the module output, bypassing the isolation transistor. FF antifuses are programmed at a higher current level than HF, VF, or XF antifuses to produce a lower resistance value.

Antifuse Connections

In general every intersection of a vertical segment and a horizontal segment contains an unprogrammed antifuse (XF-type). One exception is in the case of the clock networks.

Clock Connections

To minimize loading on the clock networks, a subset of inputs has antifuses on the clock tracks. Only a few of the C-module and S-module inputs can be connected to the clock networks. To further reduce loading on the clock network, only a subset of the horizontal routing tracks can connect to the clock inputs of the S-module.

Programming and Test Circuits

The array of logic and I/O modules is surrounded by test and programming circuits controlled by the temporary special I/O pins MODE, SDI, and DCLK. The function of these pins is similar to all ACT family devices. The ACT 3 family also includes support for two Actionprobe® circuits allowing complete observability of any logic or I/O module in the array using the temporary special I/O pins, PRA and PRB.

1

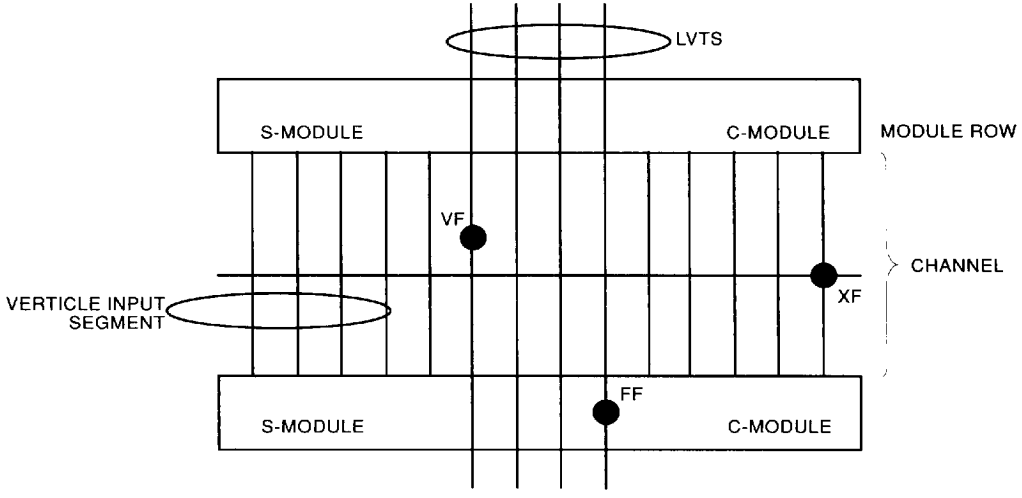

Figure 9. Vertical Routing Tracks and Segments

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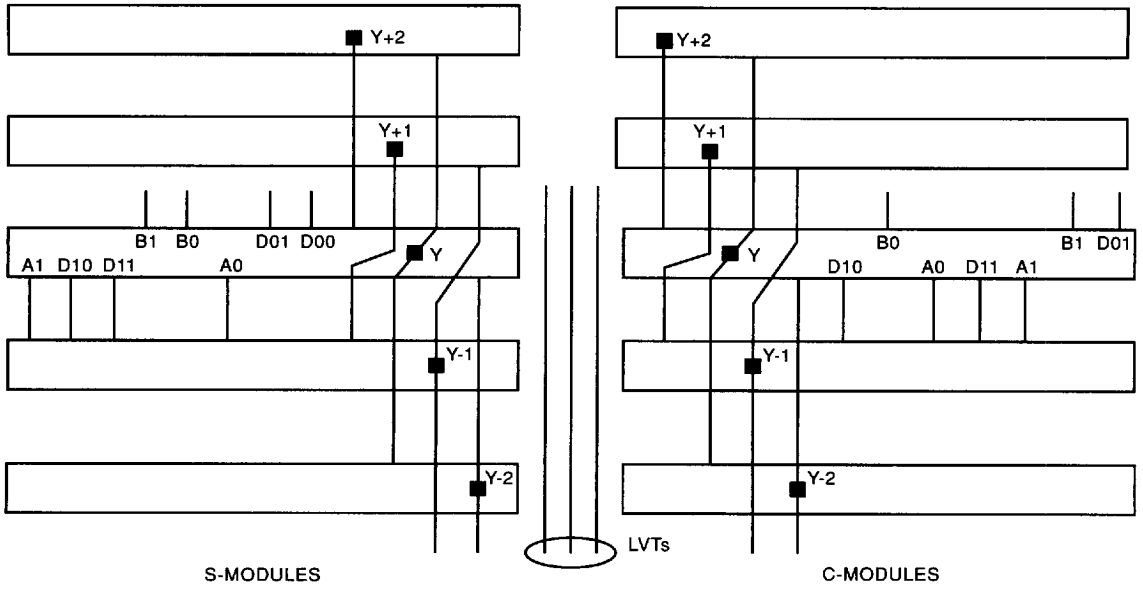

Figure 10. Logic Module Routing Interface

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Absolute Maximum Ratings[1]

Free air temperature range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage[2]	–0.5 to +7.0	V
V_I	Input Voltage	–0.5 to V_{CC} +0.5	V
V_O	Output Voltage	–0.5 to V_{CC} +0.5	V
I_{IO}	I/O Source Sink Current[3]	±20	mA
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.
2. V_{PP}, $V_{SV} = V_{CC}$, except during device programming.
3. Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5 V or less than GND – 0.5 V, the internal protection diodes will forward bias and can draw excessive current.

Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range[1]	0 to +70	–40 to +85	–55 to +125	°C
Power Supply Tolerance	±5	±10	±10	%V_{CC}

Note:

1. Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.

Electrical Specifications

Symbol	Parameter	Test Condition	Commercial		Units
			Minimum	Maximum	
V_{OH}[1,2]	HIGH Level Output	I_{OH} = –4 mA (CMOS)	3.84		V
		I_{OH} = –8 mA (TTL)	2.40		V
V_{OL}[1,2]	LOW Level Output	I_{OL} = +6 mA (CMOS)		0.33	V
		I_{OL} = +12 mA (TTL)		0.50	V
V_{IH}	HIGH Level Input	TTL Inputs	2.0	V_{CC} + 0.3	V
V_{IL}	LOW Level Input	TTL Inputs	–0.3	0.8	V
I_{IN}	Input Leakage	$V_I = V_{CC}$ or GND	–10	+10	µA
I_{OZ}	3-state Output Leakage	$V_O = V_{CC}$ or GND	–10	+10	µA
$I_{CC(S)}$	Standby V_{CC} Supply Current	$V_I = V_{CC}$ or GND,			
		I_O = 0 mA		2	mA
$I_{CC(D)}$	Dynamic V_{CC} Supply Current	See "Power Dissipation" Section			

Notes:

1. Actel devices can drive and receive either CMOS or TTL signal levels. No assignment of I/Os as TTL or CMOS is required.
2. Tested one output at a time, V_{CC} = min.

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Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a CPGA 177-pin package at commercial temperature and still air is as follows:

$$\text{Absolute Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta ja\ (°C/W)} = \frac{150°C - 70°C}{18°C/W} = 4.4\ W$$

Package Type	Pin Count	θjc	θja Still Air	θja 300 ft/min	Units
Ceramic Pin Grid Array	100	8	35	17	°C/W
	133	8	30	15	°C/W
	175	8	25	14	°C/W
	207	8	22	13	°C/W
	257	2	15	8	°C/W
Plastic Quad Flatpack[1]	100	13	55	47	°C/W
	160	15	33	26	°C/W
	208	15	33	26	°C/W
Plastic Leaded Chip Carrier[2]	84	15	44	38	°C/W

Notes:
1. Maximum Power Dissipation for 160-pin PQFP package is 1.75 Watts, 208-pin PQFP package is 2.0 Watts, and 100-pin PQFP package is 1.0 Watt.
2. Maximum Power Dissipation for PLCC package is 1.5 Watts.

Power Dissipation

$P = [I_{CC} + I_{active}] * V_{CC} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CC} - V_{OH}) * M$

Where:

I_{CC} is the current flowing when no inputs or outputs are changing.

I_{active} is the current flowing due to CMOS switching.

I_{OL}, I_{OH} are TTL sink/source currents.

V_{OL}, V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL}.

M equals the number of outputs driving TTL loads to V_{OH}.

An accurate determination of N and M is problematical because their values depend on the design and on the system I/O. The power can be divided into two components: static and active.

Static Power

Static power dissipation is typically a small component of the overall power. From the values provided in the Electrical Specifications, the maximum static power (commercial) dissipation is:

1 mA x 5.25 V = 5.25 mW

The static power dissipation by TTL loads depends on the number of outputs that drive high or low and the DC lead current flowing. Again, this number is typically small. For instance, a 32-bit bus driving TTL loads will generate 42 mW with all outputs driving low or 140 mA with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

Active Time

The active power component in CMOS devices is frequency dependent and depends on the user's logic and the external I/O. Active power dissipation results from charging internal chip capacitance such as that associated with the interconnect tracks, unprogrammed antifuses, module inputs, and module outputs plus external capacitance due to PC board traces and load device inputs. An additional component of active power dissipation is due to totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by Equation 1.

$$\text{Power}\ (\mu W) = C_{EQ} * V_{CC}^2 * f \qquad (1)$$

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Where:

C_{EQ} is the equivalent capacitance expressed in picofarads (pF).

V_{CC} is power supply in volts (V).

f is the switching frequency in megahertz (MHz).

Equivalent capacitance is calculated by measuring I_{active} at a specified frequency and voltage for each circuit component of interest. The results for ACT 3 devices are:

	C_{EQ} (pF)
Modules	8.2
Input Buffers	1.5
Output Buffers	2.3
I/O Clock Buffer Loads	0.4
Dedicated Array Clock Buffer Loads	0.5
Routed Array Clock Buffer Loads	0.5 + fixed/device

To calculate the active power dissipated from the complete design, you must solve Equation 1 for each component. To do this, you must know the switching frequency of each part of the logic. The exact equation is a piece-wise linear summation over all components, as shown in Equation 2.

$$\text{Power } (\mu W) = [(m \times 8.2 \times f_1) + (n \times 1.5 \times f_2) + (p \times (2.3 + C_L) \times f_3) + (q \times 0.5 \times f_4) + ((r_1 + 0.5\, r_2) \times f_5) + (s \times 0.4 \times f_6)] \times V_{CC}^2 \quad (2)$$

Where:

m = Number of logic modules switching at f_1

n = Number of input buffers switching at f_2

p = Number of output buffers switching at f_3

q = Number of clock loads on the dedicated array clock network

A1415A: q = 104

A1425A: q = 160

A1440A: q = 288

A1460A: q = 432

A14100A: q = 697

r_1 = Fixed capacitance due to routed array clock network

A1415A: r_1 = 60

A1425A: r_1 = 75

A1440A: r_1 = 105

A1460A: r_1 = 145

A14100A: r_1 = 195

r_2 = Number of clock loads on the routed array clock network

s = Number of clock loads on the dedicated I/O clock network

A1415A: s = 80

A1425A: s = 100

A1440A: s = 140

A1460A: s = 168

A14100A: s = 228

f_1 = Average logic module switching rate in MHz

f_2 = Average input buffer switching rate in MHz

f_3 = Average output buffer switching rate in MHz

f_4 = Average dedicated array clock rate in MHz

f_5 = Average routed array clock rate in MHz

f_6 = Average dedicated I/O clock rate in MHz

C_L = Output load capacitance in pF

Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following rules are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These rules are as follows:

Logic Modules (m)	=	80% of modules
Average module switching rate (f_1)	=	F/10
Inputs switching (n)	=	# I/Os used/12
Average input switching rate (f_2)	=	F
Outputs switching (p)	=	# I/Os used/15
Output loading (C_L)	=	35
Average output switching rate (f_3)	=	F/2
Dedicated array clock loads (q)	=	fixed by device
Average dedicated array switching rate (f_4)	=	F
Routed array fixed capacitance (r_1)	=	fixed by device
Routed array clock loads (r_2)	=	40% of sequential modules
Average routed array switching rate (f_5)	=	F/2
I/O clock loads (s)	=	# I/Os used
Average I/O switching rate (f_6)	=	F

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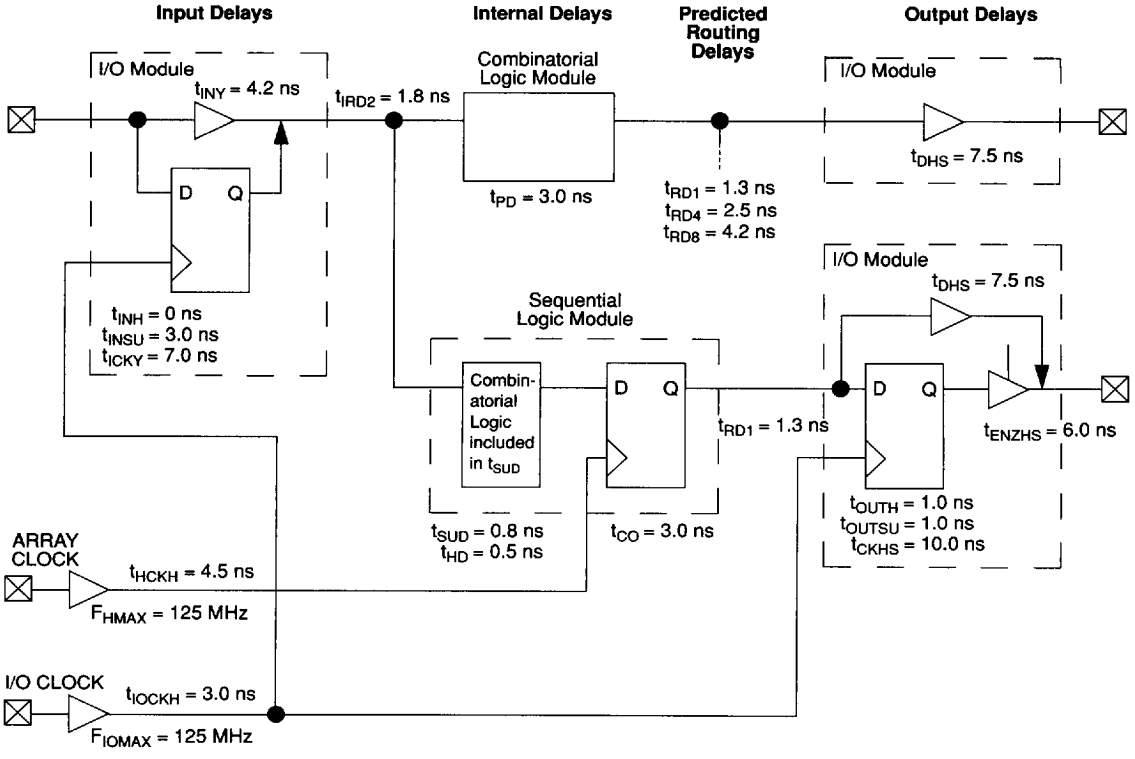
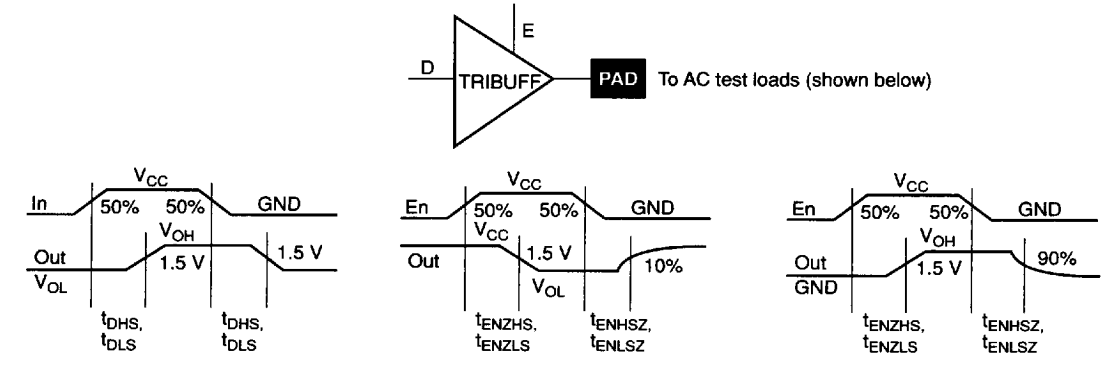
ACT 3 Timing Model*



*Values shown for A1425A.

Output Buffer Delays



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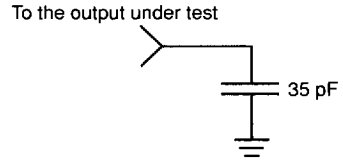
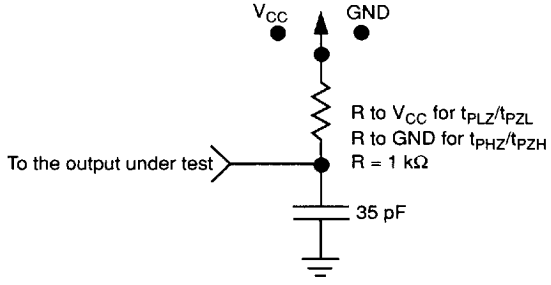
AC Test Loads

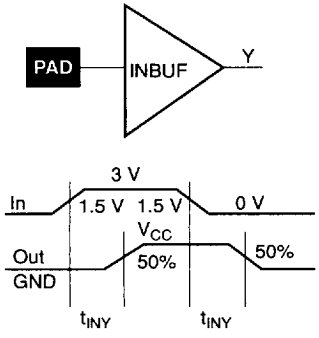
Load 1
(Used to measure propagation delay)



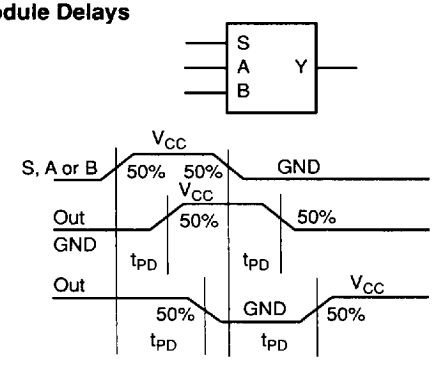
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

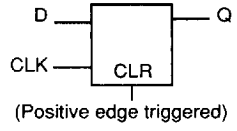


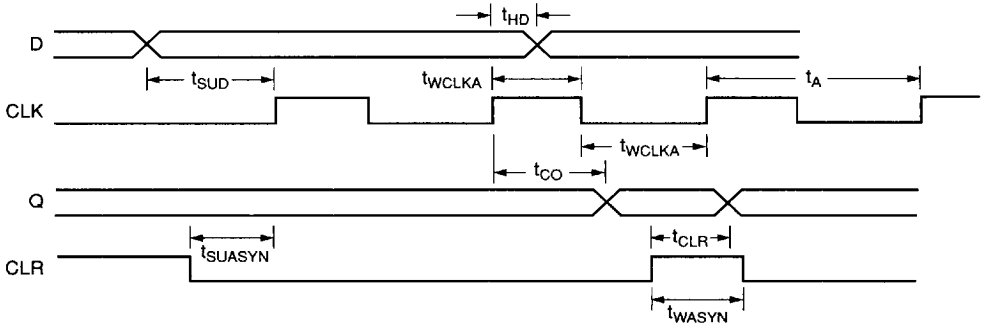
Module Delays



Sequential Module Timing Characteristics

Flip-Flops





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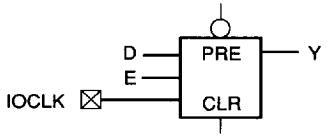
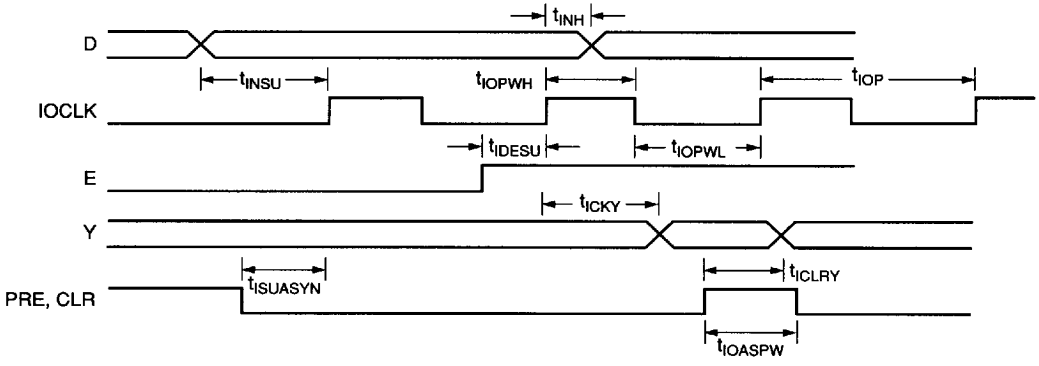
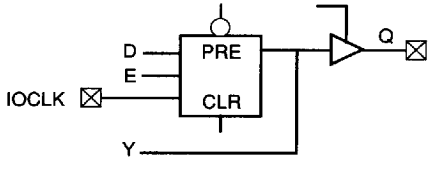
I/O Module: Sequential Input Timing Characteristics



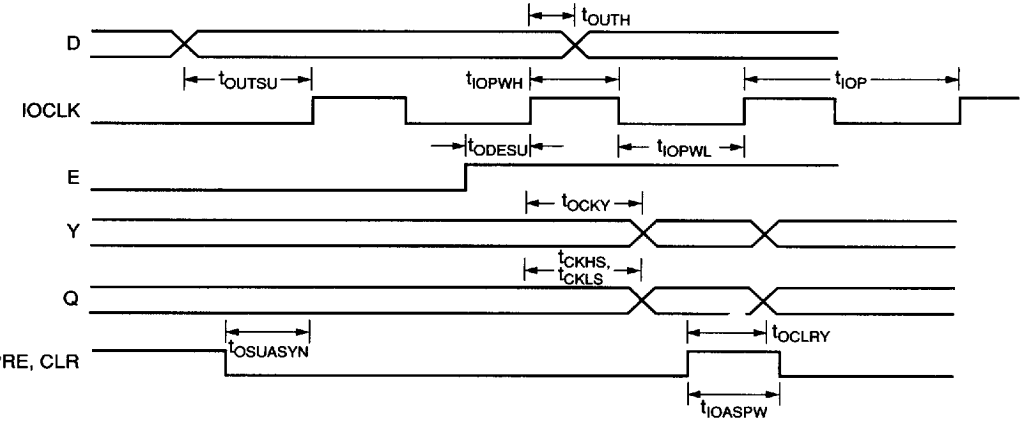
(Positive edge triggered)



I/O Module: Sequential Output Timing Characteristics



(Positive edge triggered)



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Predictable Performance: Tightest Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increases.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer lengths of routing track.

The ACT 3 family delivers the tightest fanout delay distribution of any FPGA. This tight distribution is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Actel's patented PLICE antifuse offers a very low resistive/capacitive interconnect. The ACT 3 family's antifuses, fabricated in 0.8 µm lithography, offer nominal levels of 200Ω resistance and 6 femtofarad (fF) capacitance per antifuse.

The ACT 3 fanout distribution is also tighter than alternative devices due to the low number of antifuses required per interconnect path. The ACT 3 family's proprietary architecture limits the number of antifuses per path to only four, with 90% of interconnects using only two antifuses.

Table 3. Logic Module + Routing Delay, by fanout (ns)[1] (Worst-Case Commercial Conditions)

Family	FO=1	FO=2	FO=3	FO=4	FO=8
ACT 1	5.0	5.7	6.6	7.9	12.5
ACT 2	5.5	6.2	6.9	7.4	9.2
ACT 3	3.7	4.2	4.4	4.8	6.2

Note:
1. '–1' Speed Devices Specified

The ACT 3 family's tight fanout delay distribution offers an FPGA design environment in which fanout can be traded for the increased performance of reduced logic level designs. This also simplifies performance estimates when designing with ACT 3 devices.

Timing Characteristics

Timing characteristics for ACT 3 devices fall into three categories: family dependent, device dependent, and design dependent. The input and output buffer characteristics are common to all ACT 3 family members. Internal routing delays are device dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the ALS Timer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically up to 6% of nets in a fully utilized device require long tracks. Long tracks contribute approximatley 4 ns to 14 ns delay. This additional delay is represented statistically in higher fanout (FO=8) routing delays in the data sheet specifications section.

Timing Derating

ACT 3 devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

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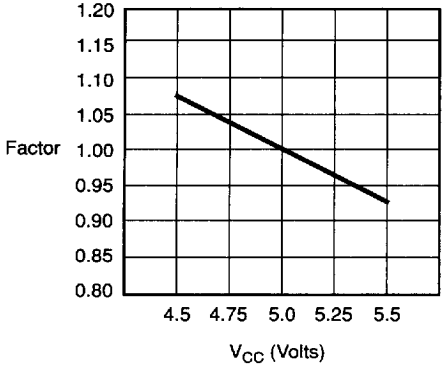
Timing Derating Factor, Temperature and Voltage

	Industrial		Military	
	Minimum	Maximum	Minimum	Maximum
(Commercial Minimum/Maximum Specification) x	0.85	1.07	0.81	1.16

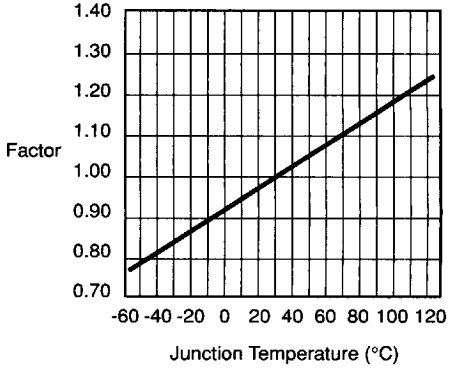
Timing Derating Factor for Designs at Typical Temperature (T_J = 25°C) and Voltage (5.0 V)

(Commercial Maximum Specification) x	0.87

Voltage Derating Curve



Temperature Derating Curve



Note:
This derating factor applies to all routing and propagation delays.

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A1415A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

		Preliminary Information		Advanced Information*		
Logic Module Propagation Delays[1]		**'Std' Speed**		**'–1' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		3.0		2.6	ns
t_{CO}	Sequential Clock to Q		3.0		2.6	ns
t_{CLR}	Asynchronous Clear to Q		3.0		2.6	ns
Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		1.3		1.1	ns
t_{RD2}	FO=2 Routing Delay		1.8		1.6	ns
t_{RD3}	FO=3 Routing Delay		2.1		1.8	ns
t_{RD4}	FO=4 Routing Delay		2.5		2.2	ns
t_{RD8}	FO=8 Routing Delay		4.2		3.6	ns
Logic Module Sequential Timing						
t_{SUD}	Flip-Flop Data Input Setup	0.8		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.5		0.5		ns
t_{SUD}	Latch Data Input Setup	0.8		0.8		ns
t_{HD}	Latch Data Input Hold	0.5		0.5		ns
t_{SUASYN}	Asynchronous Input Setup	TBD		TBD		ns
t_{WASYN}	Asynchronous Pulse Width	3.8		3.2		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	3.8		3.2		ns
t_A	Flip-Flop Clock Input Period	8.0		6.8		ns
f_{MAX}	Flip-Flop Clock Frequency		125		150	MHz

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

**Actel is offering "Advanced Information" only on '–1' Speed devices. Consult Actel for '–1' device availability.*

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A1415A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		Advanced Information*		
I/O Module Input Propagation Delays		**'Std' Speed**		**'–1' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INY}	Input Data Pad to Y		4.2		3.6	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		7.0		6.0	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		7.0		6.0	ns
t_{ICLRY}	Input Asynchronous Clear to Y		7.0		6.0	ns
t_{OCLRY}	Output Asynchronous Clear to Y		7.0		6.0	ns
Predicted Input Routing Delays[1]						
t_{IRD1}	FO=1 Routing Delay		1.3		1.1	ns
t_{IRD2}	FO=2 Routing Delay		1.8		1.6	ns
t_{IRD3}	FO=3 Routing Delay		2.1		1.8	ns
t_{IRD4}	FO=4 Routing Delay		2.5		2.2	ns
t_{IRD8}	FO=8 Routing Delay		4.2		3.6	ns
I/O Module Sequential Timing						
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	3.0		3.0		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	9.0		9.0		ns
$t_{ISUASYN}$	Input Asynchronous Setup	TBD		TBD		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	1.0		1.0		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	1.0		1.0		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.5		0.5		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	2.0		2.0		ns
$t_{OSUASYN}$	Output Asynchronous Setup	TBD		TBD		ns

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

**Actel is offering "Advanced Information" only on '–1' Speed devices. Consult Actel for '–1' device availability.*

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A1415A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		Advanced Information*		
I/O Module – TTL Output Timing[1]		**'Std' Speed**		**'–1' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DHS}	Data to Pad, High Slew		7.5		6.4	ns
t_{DLS}	Data to Pad, Low Slew		12.0		10.2	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		6.0		5.1	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		11.0		9.4	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		10.0		8.5	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		10.0		8.5	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		10.0		9.0	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		15.0		13.5	ns
d_{TLHHS}	Delta Low to High, Hi Slew		TBD		TBD	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		TBD		TBD	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		TBD		TBD	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		TBD		TBD	ns/pF
I/O Module – CMOS Output Timing[1]						
t_{DHS}	Data to Pad, High Slew		9.3		7.9	ns
t_{DLS}	Data to Pad, Low Slew		17.5		14.9	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		7.8		6.6	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		13.3		11.3	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		10.0		8.5	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		10.0		9.0	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		11.8		10.7	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		17.3		15.6	ns
d_{TLHHS}	Delta Low to High, Hi Slew		TBD		TBD	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		TBD		TBD	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		TBD		TBD	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		TBD		TBD	ns/pF

Note:
1. Delays based on 35pF loading.

**Actel is offering "Advanced Information" only on '–1' Speed devices. Consult Actel for '–1' device availability.*

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A1415A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		Advanced Information*		
Dedicated (Hard-Wired) I/O Clock Network		'Std' Speed		'–1' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		3.0		2.6	ns
t_{IOPWH}	Minimum Pulse Width High	3.8		3.3		ns
t_{IOPWL}	Minimum Pulse Width Low	3.8		3.3		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	3.8		3.3		ns
t_{IOCKSW}	Maximum Skew		0.4		0.4	ns
t_{IOP}	Minimum Period	8.0		6.8		ns
f_{IOMAX}	Maximum Frequency		125		150	MHz
Dedicated (Hard-Wired) Array Clock Network						
t_{HCKH}	Input Low to High (Pad to S-Module Input)		4.5		3.9	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		4.5		3.9	ns
t_{HPWH}	Minimum Pulse Width High	3.8		3.3		ns
t_{HPWL}	Minimum Pulse Width Low	3.8		3.3		ns
t_{HCKSW}	Maximum Skew		0.3		0.3	ns
t_{HP}	Minimum Period	8.0		6.8		ns
f_{HMAX}	Maximum Frequency		125		150	MHz
Routed Array Clock Networks						
t_{RCKH}	Input Low to High (FO=64)		5.5		4.7	ns
t_{RCKL}	Input High to Low (FO=64)		6.0		5.1	ns
t_{RPWH}	Min. Pulse Width High (FO=64)	4.9		4.2		ns
t_{RPWL}	Min. Pulse Width Low (FO=64)	4.9		4.2		ns
t_{RCKSW}	Maximum Skew (FO=128)		1.0		0.9	ns
t_{RP}	Minimum Period (FO=64)	10.0		8.7		ns
f_{RMAX}	Maximum Frequency (FO=64)		100		115	MHz
Clock-to-Clock Skews						
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	1.3	0.0	3.0	ns
$t_{IOHCKSW}$	I/O Clock to R-Clock Skew	0.0	3.0	0.0	3.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew	0.0	1.0	0.0	1.0	ns

Note:
1. Delays based on 35pF loading.

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A1425A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

		Preliminary Information		Preliminary Information		Advanced Information*		
Logic Module Propagation Delays[1]		**'Std' Speed**		**'–1' Speed**		**'–2' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		3.0		2.6		2.3	ns
t_{CO}	Sequential Clock to Q		3.0		2.6		2.3	ns
t_{CLR}	Asynchronous Clear to Q		3.0		2.6		2.3	ns
Predicted Routing Delays[2]								
t_{RD1}	FO=1 Routing Delay		1.3		1.1		1.0	ns
t_{RD2}	FO=2 Routing Delay		1.8		1.6		1.4	ns
t_{RD3}	FO=3 Routing Delay		2.1		1.8		1.6	ns
t_{RD4}	FO=4 Routing Delay		2.5		2.2		1.9	ns
t_{RD8}	FO=8 Routing Delay		4.2		3.6		3.2	ns
Logic Module Sequential Timing								
t_{SUD}	Flip-Flop Data Input Setup	0.8		0.8		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.5		0.5		0.5		ns
t_{SUD}	Latch Data Input Setup	0.8		0.8		0.8		ns
t_{HD}	Latch Data Input Hold	0.5		0.5		0.5		ns
t_{SUASYN}	Asynchronous Input Setup	TBD		TBD		TBD		ns
t_{WASYN}	Asynchronous Pulse Width	3.8		3.2		2.9		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	3.8		3.2		2.9		ns
t_A	Flip-Flop Clock Input Period	8.0		6.8		6.0		ns
f_{MAX}	Flip-Flop Clock Frequency		125		150		167	MHz

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

**Actel is offering "Advanced Information" only on '–2' Speed devices. Consult Actel for '–2' device availability.*

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A1425A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		Preliminary Information		Advanced Information*		
I/O Module Input Propagation Delays		'Std' Speed		'–1' Speed		'–2' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INY}	Input Data Pad to Y		4.2		3.6		3.2	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		7.0		6.0		5.3	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		7.0		6.0		5.3	ns
t_{ICLRY}	Input Asynchronous Clear to Y		7.0		6.0		5.3	ns
t_{OCLRY}	Output Asynchronous Clear to Y		7.0		6.0		5.3	ns
Predicted Input Routing Delays[1]								
t_{IRD1}	FO=1 Routing Delay		1.3		1.1		1.0	ns
t_{IRD2}	FO=2 Routing Delay		1.8		1.6		1.4	ns
t_{IRD3}	FO=3 Routing Delay		2.1		1.8		1.6	ns
t_{IRD4}	FO=4 Routing Delay		2.5		2.2		1.9	ns
t_{IRD8}	FO=8 Routing Delay		4.2		3.6		3.2	ns
I/O Module Sequential Timing								
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	3.0		3.0		3.0		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	9.0		9.0		9.0		ns
$t_{ISUASYN}$	Input Asynchronous Setup	TBD		TBD		TBD		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	1.0		1.0		1.0		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	1.0		1.0		1.0		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.5		0.5		0.5		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	2.0		2.0		2.0		ns
$t_{OSUASYN}$	Output Asynchronous Setup	TBD		TBD		TBD		ns

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

**Actel is offering "Advanced Information" only on '–2' Speed devices. Consult Actel for '–2' device availability.*

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A1425A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		Preliminary Information		Advanced Information*		
I/O Module – TTL Output Timing[1]		**'Std' Speed**		**'–1' Speed**		**'–2' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DHS}	Data to Pad, High Slew		7.5		6.4		5.6	ns
t_{DLS}	Data to Pad, Low Slew		12.0		10.2		9.0	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		6.0		5.1		4.5	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		11.0		9.4		8.3	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		10.0		8.5		7.5	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		10.0		8.5		7.5	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		10.0		9.0		7.5	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		15.0		13.5		11.3	ns
d_{TLHHS}	Delta Low to High, Hi Slew		TBD		TBD		TBD	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		TBD		TBD		TBD	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		TBD		TBD		TBD	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		TBD		TBD		TBD	ns/pF
I/O Module – CMOS Output Timing[1]								
t_{DHS}	Data to Pad, High Slew		9.3		7.9		7.0	ns
t_{DLS}	Data to Pad, Low Slew		17.5		14.9		13.1	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		7.8		6.6		5.9	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		13.3		11.3		10.0	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		10.0		8.5		7.5	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		10.0		9.0		7.5	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		11.8		10.7		8.9	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		17.3		15.6		13.0	ns
d_{TLHHS}	Delta Low to High, Hi Slew		TBD		TBD		TBD	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		TBD		TBD		TBD	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		TBD		TBD		TBD	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		TBD		TBD		TBD	ns/pF

Note:
1. Delays based on 35pF loading.

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A1425A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		Preliminary Information		Advanced Information*		
Dedicated (Hard-Wired) I/O Clock Network		**'Std' Speed**		**'–1' Speed**		**'–2' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		3.0		2.6		2.3	ns
t_{IOPWH}	Minimum Pulse Width High	3.8		3.3		2.9		ns
t_{IOPWL}	Minimum Pulse Width Low	3.8		3.3		2.9		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	3.8		3.3		2.9		ns
t_{IOCKSW}	Maximum Skew		0.4		0.4		0.4	ns
t_{IOP}	Minimum Period	8.0		6.8		6.0		ns
f_{IOMAX}	Maximum Frequency		125		150		167	MHz
Dedicated (Hard-Wired) Array Clock Network								
t_{HCKH}	Input Low to High (Pad to S-Module Input)		4.5		3.9		3.4	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		4.5		3.9		3.4	ns
t_{HPWH}	Minimum Pulse Width High	3.8		3.3		2.9		ns
t_{HPWL}	Minimum Pulse Width Low	3.8		3.3		2.9		ns
t_{HCKSW}	Maximum Skew		0.3		0.3		0.3	ns
t_{HP}	Minimum Period	8.0		6.8		6.0		ns
f_{HMAX}	Maximum Frequency		125		150		167	MHz
Routed Array Clock Networks								
t_{RCKH}	Input Low to High (FO=64)		5.5		4.7		4.1	ns
t_{RCKL}	Input High to Low (FO=64)		6.0		5.1		4.5	ns
t_{RPWH}	Min. Pulse Width High (FO=64)	4.9		4.2		3.8		ns
t_{RPWL}	Min. Pulse Width Low (FO=64)	4.9		4.2		3.8		ns
t_{RCKSW}	Maximum Skew (FO=128)		1.0		0.9		0.8	ns
t_{RP}	Minimum Period (FO=64)	10.0		8.7		8.0		ns
f_{RMAX}	Maximum Frequency (FO=64)		100		115		125	MHz
Clock-to-Clock Skews								
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	1.3	0.0	3.0	0.0	3.0	ns
$t_{IOHCKSW}$	I/O Clock to R-Clock Skew	0.0	3.0	0.0	3.0	0.0	3.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew	0.0	1.0	0.0	1.0	0.0	1.0	ns

Note:
1. Delays based on 35pF loading.

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A1440A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

		Preliminary Information		Advanced Information*		
Logic Module Propagation Delays[1]		**'Std' Speed**		**'–1' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		3.0		2.6	ns
t_{CO}	Sequential Clock to Q		3.0		2.6	ns
t_{CLR}	Asynchronous Clear to Q		3.0		2.6	ns
Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		1.3		1.1	ns
t_{RD2}	FO=2 Routing Delay		1.8		1.6	ns
t_{RD3}	FO=3 Routing Delay		2.1		1.8	ns
t_{RD4}	FO=4 Routing Delay		2.5		2.2	ns
t_{RD8}	FO=8 Routing Delay		4.2		3.6	ns
Logic Module Sequential Timing						
t_{SUD}	Flip-Flop Data Input Setup	0.8		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.5		0.5		ns
t_{SUD}	Latch Data Input Setup	0.8		0.8		ns
t_{HD}	Latch Data Input Hold	0.5		0.5		ns
t_{SUASYN}	Asynchronous Input Setup	TBD		TBD		ns
t_{WASYN}	Asynchronous Pulse Width	3.8		3.2		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	3.8		3.2		ns
t_A	Flip-Flop Clock Input Period	8.0		6.8		ns
f_{MAX}	Flip-Flop Clock Frequency		125		150	MHz

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

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A1440A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		Advanced Information*		
I/O Module Input Propagation Delays		'Std' Speed		'–1' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INY}	Input Data Pad to Y		4.2		3.6	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		7.0		6.0	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		7.0		6.0	ns
t_{ICLRY}	Input Asynchronous Clear to Y		7.0		6.0	ns
t_{OCLRY}	Output Asynchronous Clear to Y		7.0		6.0	ns
Predicted Input Routing Delays[1]						
t_{IRD1}	FO=1 Routing Delay		1.3		1.1	ns
t_{IRD2}	FO=2 Routing Delay		1.8		1.6	ns
t_{IRD3}	FO=3 Routing Delay		2.1		1.8	ns
t_{IRD4}	FO=4 Routing Delay		2.5		2.2	ns
t_{IRD8}	FO=8 Routing Delay		4.2		3.6	ns
I/O Module Sequential Timing						
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	3.0		3.0		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	9.0		9.0		ns
$t_{ISUASYN}$	Input Asynchronous Setup	TBD		TBD		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	1.0		1.0		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	1.0		1.0		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.5		0.5		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	2.0		2.0		ns
$t_{OSUASYN}$	Output Asynchronous Setup	TBD		TBD		ns

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

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A1440A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		Advanced Information*		
I/O Module – TTL Output Timing[1]		**'Std' Speed**		**'–1' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DHS}	Data to Pad, High Slew		7.5		6.4	ns
t_{DLS}	Data to Pad, Low Slew		12.0		10.2	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		6.0		5.1	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		11.0		9.4	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		11.0		9.4	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		11.0		9.4	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		11.0		10.0	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		15.0		13.5	ns
d_{TLHHS}	Delta Low to High, Hi Slew		TBD		TBD	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		TBD		TBD	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		TBD		TBD	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		TBD		TBD	ns/pF
I/O Module – CMOS Output Timing[1]						
t_{DHS}	Data to Pad, High Slew		9.3		7.9	ns
t_{DLS}	Data to Pad, Low Slew		17.5		14.9	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		7.8		6.6	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		13.3		8.5	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		11.0		9.4	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		11.0		9.4	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		11.8		10.7	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		17.3		15.6	ns
d_{TLHHS}	Delta Low to High, Hi Slew		TBD		TBD	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		TBD		TBD	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		TBD		TBD	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		TBD		TBD	ns/pF

Note:
1. Delays based on 35pF loading.

**Actel is offering "Advanced Information" only on '–1' Speed devices. Consult Actel for '–1' device availability.*

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A1440A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		Advanced Information*		
Dedicated (Hard-Wired) I/O Clock Network		'Std' Speed		'–1' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		3.0		2.6	ns
t_{IOPWH}	Minimum Pulse Width High	3.8		3.3		ns
t_{IOPWL}	Minimum Pulse Width Low	3.8		3.3		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	3.8		3.3		ns
t_{IOCKSW}	Maximum Skew		0.4		0.4	ns
t_{IOP}	Minimum Period	8.0		6.8		ns
f_{IOMAX}	Maximum Frequency		125		150	MHz
Dedicated (Hard-Wired) Array Clock Network						
t_{HCKH}	Input Low to High (Pad to S-Module Input)		4.5		3.9	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		4.5		3.9	ns
t_{HPWH}	Minimum Pulse Width High	3.8		3.3		ns
t_{HPWL}	Minimum Pulse Width Low	3.8		3.3		ns
t_{HCKSW}	Maximum Skew		0.3		0.3	ns
t_{HP}	Minimum Period	8.0		6.8		ns
f_{HMAX}	Maximum Frequency		125		150	MHz
Routed Array Clock Networks						
t_{RCKH}	Input Low to High (FO=64)		5.5		4.7	ns
t_{RCKL}	Input High to Low (FO=64)		6.0		5.1	ns
t_{RPWH}	Min. Pulse Width High (FO=64)	4.9		4.2		ns
t_{RPWL}	Min. Pulse Width Low (FO=64)	4.9		4.2		ns
t_{RCKSW}	Maximum Skew (FO=128)		1.0		0.9	ns
t_{RP}	Minimum Period (FO=64)	10.0		8.7		ns
f_{RMAX}	Maximum Frequency (FO=64)		100		115	MHz
Clock-to-Clock Skews						
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	1.3	0.0	3.0	ns
$t_{IOHCKSW}$	I/O Clock to R-Clock Skew	0.0	3.0	0.0	3.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew	0.0	1.0	0.0	1.0	ns

Note:
1. Delays based on 35pF loading.

**Actel is offering "Advanced Information" only on '–1' Speed devices. Consult Actel for '–1' device availability.*

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A1460A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

		Preliminary Information		Advanced Information*		
Logic Module Propagation Delays[1]		**'Std' Speed**		**'–1' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		3.0		2.6	ns
t_{CO}	Sequential Clock to Q		3.0		2.6	ns
t_{CLR}	Asynchronous Clear to Q		3.0		2.6	ns
Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		1.3		1.1	ns
t_{RD2}	FO=2 Routing Delay		1.8		1.6	ns
t_{RD3}	FO=3 Routing Delay		2.1		1.8	ns
t_{RD4}	FO=4 Routing Delay		2.5		2.2	ns
t_{RD8}	FO=8 Routing Delay		4.2		3.6	ns
Logic Module Sequential Timing						
t_{SUD}	Flip-Flop Data Input Setup	0.8		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.5		0.5		ns
t_{SUD}	Latch Data Input Setup	0.8		0.8		ns
t_{HD}	Latch Data Input Hold	0.5		0.5		ns
t_{SUASYN}	Asynchronous Input Setup	TBD		TBD		ns
t_{WASYN}	Asynchronous Pulse Width	4.8		4.1		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	4.8		4.1		ns
t_A	Flip-Flop Clock Input Period	10.0		8.5		ns
f_{MAX}	Flip-Flop Clock Frequency		100		120	MHz

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

**Actel is offering "Advanced Information" only on '–1' Speed devices. Consult Actel for '–1' device availability.*

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A1460A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		Advanced Information*		
I/O Module Input Propagation Delays		'Std' Speed		'–1' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INY}	Input Data Pad to Y		4.2		3.6	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		7.0		6.0	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		7.0		6.0	ns
t_{ICLRY}	Input Asynchronous Clear to Y		7.0		6.0	ns
t_{OCLRY}	Output Asynchronous Clear to Y		7.0		6.0	ns
Predicted Input Routing Delays[1]						
t_{IRD1}	FO=1 Routing Delay		1.3		1.1	ns
t_{IRD2}	FO=2 Routing Delay		1.8		1.6	ns
t_{IRD3}	FO=3 Routing Delay		2.1		1.8	ns
t_{IRD4}	FO=4 Routing Delay		2.5		2.2	ns
t_{IRD8}	FO=8 Routing Delay		4.2		3.6	ns
I/O Module Sequential Timing						
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	3.0		3.0		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	9.0		9.0		ns
$t_{ISUASYN}$	Input Asynchronous Setup	TBD		TBD		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	1.0		1.0		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	1.0		1.0		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.5		0.5		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	2.0		2.0		ns
$t_{OSUASYN}$	Output Asynchronous Setup	TBD		TBD		ns

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

**Actel is offering "Advanced Information" only on '–1' Speed devices. Consult Actel for '–1' device availability.*

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A1460A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		Advanced Information*		
I/O Module – TTL Output Timing[1]		**'Std' Speed**		**'–1' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DHS}	Data to Pad, High Slew		7.5		6.4	ns
t_{DLS}	Data to Pad, Low Slew		12.0		10.2	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		6.0		5.1	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		11.0		9.4	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		11.6		9.9	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		11.0		9.4	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		11.6		10.4	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		17.0		15.3	ns
d_{TLHHS}	Delta Low to High, Hi Slew		TBD		TBD	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		TBD		TBD	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		TBD		TBD	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		TBD		TBD	ns/pF
I/O Module – CMOS Output Timing[1]						
t_{DHS}	Data to Pad, High Slew		9.3		7.9	ns
t_{DLS}	Data to Pad, Low Slew		17.5		14.9	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		7.8		6.6	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		13.3		11.3	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		11.0		9.4	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		11.0		9.4	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		13.8		12.4	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		19.3		17.4	ns
d_{TLHHS}	Delta Low to High, Hi Slew		TBD		TBD	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		TBD		TBD	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		TBD		TBD	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		TBD		TBD	ns/pF

Note:
1. Delays based on 35pF loading.

**Actel is offering "Advanced Information" only on '–1' Speed devices. Consult Actel for '–1' device availability.*

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A1460A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		Advanced Information*		
Dedicated (Hard-Wired) I/O Clock Network		**'Std' Speed**		**'–1' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		3.5		3.0	ns
t_{IOPWH}	Minimum Pulse Width High	4.8		4.1		ns
t_{IOPWL}	Minimum Pulse Width Low	4.8		4.1		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	3.8		3.3		ns
t_{IOCKSW}	Maximum Skew		0.8		0.7	ns
t_{IOP}	Minimum Period	10.0		8.5		ns
f_{IOMAX}	Maximum Frequency		100		120	MHz
Dedicated (Hard-Wired) Array Clock Network						
t_{HCKH}	Input Low to High (Pad to S-Module Input)		5.5		4.7	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		5.5		4.7	ns
t_{HPWH}	Minimum Pulse Width High	4.8		4.1		ns
t_{HPWL}	Minimum Pulse Width Low	4.8		4.1		ns
t_{HCKSW}	Maximum Skew		0.8		0.7	ns
t_{HP}	Minimum Period	10.0		8.5		ns
f_{HMAX}	Maximum Frequency		100		120	MHz
Routed Array Clock Networks						
t_{RCKH}	Input Low to High (FO=256)		9.0		7.7	ns
t_{RCKL}	Input High to Low (FO=256)		9.0		7.7	ns
t_{RPWH}	Min. Pulse Width High (FO=256)	6.1		5.4		ns
t_{RPWL}	Min. Pulse Width Low (FO=256)	6.1		5.4		ns
t_{RCKSW}	Maximum Skew (FO=128)		1.8		1.6	ns
t_{RP}	Minimum Period (FO=256)	12.5		11.1		ns
f_{RMAX}	Maximum Frequency (FO=256)		80		90	MHz
Clock-to-Clock Skews						
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	3.5	0.0	3.5	ns
$t_{IOHCKSW}$	I/O Clock to R-Clock Skew	0.0	5.0	0.0	5.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew	0.0	3.0	0.0	3.0	ns

Note:
1. Delays based on 35pF loading.

**Actel is offering "Advanced Information" only on '–1' Speed devices. Consult Actel for '–1' device availability.*

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A14100A Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

		Preliminary Information		Advanced Information*		
Logic Module Propagation Delays[1]		**'Std' Speed**		**'–1' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{PD}	Internal Array Module		3.0		2.6	ns
t_{CO}	Sequential Clock to Q		3.0		2.6	ns
t_{CLR}	Asynchronous Clear to Q		3.0		2.6	ns
Predicted Routing Delays[2]						
t_{RD1}	FO=1 Routing Delay		1.3		1.1	ns
t_{RD2}	FO=2 Routing Delay		1.8		1.6	ns
t_{RD3}	FO=3 Routing Delay		2.1		1.8	ns
t_{RD4}	FO=4 Routing Delay		2.5		2.2	ns
t_{RD8}	FO=8 Routing Delay		4.2		3.6	ns
Logic Module Sequential Timing						
t_{SUD}	Flip-Flop Data Input Setup	0.8		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.5		0.5		ns
t_{SUD}	Latch Data Input Setup	0.8		0.8		ns
t_{HD}	Latch Data Input Hold	0.5		0.5		ns
t_{SUASYN}	Asynchronous Input Setup	TBD		TBD		ns
t_{WASYN}	Asynchronous Pulse Width	4.8		4.1		ns
t_{WCLKA}	Flip-Flop Clock Pulse Width	4.8		4.1		ns
t_A	Flip-Flop Clock Input Period	10.0		8.5		ns
f_{MAX}	Flip-Flop Clock Frequency		100		120	MHz

Notes:

1. For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.
2. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

**Actel is offering "Advanced Information" only on '–1' Speed devices. Consult Actel for '–1' device availability.*

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A14100A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		Advanced Information*		
I/O Module Input Propagation Delays		**'Std' Speed**		**'–1' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{INY}	Input Data Pad to Y		4.2		3.6	ns
t_{ICKY}	Input Reg IOCLK Pad to Y		7.0		6.0	ns
t_{OCKY}	Output Reg IOCLK Pad to Y		7.0		6.0	ns
t_{ICLRY}	Input Asynchronous Clear to Y		7.0		6.0	ns
t_{OCLRY}	Output Asynchronous Clear to Y		7.0		6.0	ns
Predicted Input Routing Delays[1]						
t_{IRD1}	FO=1 Routing Delay		1.3		1.1	ns
t_{IRD2}	FO=2 Routing Delay		1.8		1.6	ns
t_{IRD3}	FO=3 Routing Delay		2.1		1.8	ns
t_{IRD4}	FO=4 Routing Delay		2.5		2.2	ns
t_{IRD8}	FO=8 Routing Delay		4.2		3.6	ns
I/O Module Sequential Timing						
t_{INH}	Input F-F Data Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{INSU}	Input F-F Data Setup (w.r.t. IOCLK Pad)	3.0		3.0		ns
t_{IDEH}	Input Data Enable Hold (w.r.t. IOCLK Pad)	0.0		0.0		ns
t_{IDESU}	Input Data Enable Setup (w.r.t. IOCLK Pad)	9.0		9.0		ns
$t_{ISUASYN}$	Input Asynchronous Setup	TBD		TBD		ns
t_{OUTH}	Output F-F Data Hold (w.r.t. IOCLK Pad)	1.0		1.0		ns
t_{OUTSU}	Output F-F Data Setup (w.r.t. IOCLK Pad)	1.0		1.0		ns
t_{ODEH}	Output Data Enable Hold (w.r.t. IOCLK Pad)	0.5		0.5		ns
t_{ODESU}	Output Data Enable Setup (w.r.t. IOCLK Pad)	2.0		2.0		ns
$t_{OSUASYN}$	Output Asynchronous Setup	TBD		TBD		ns

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.

**Actel is offering "Advanced Information" only on '–1' Speed devices. Consult Actel for '–1' device availability.*

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A14100A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		Advanced Information*		
I/O Module – TTL Output Timing[1]		**'Std' Speed**		**'–1' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{DHS}	Data to Pad, High Slew		7.5		6.4	ns
t_{DLS}	Data to Pad, Low Slew		12.0		10.2	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		6.0		5.1	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		11.0		9.4	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		12.0		10.2	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		11.0		9.4	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		12.0		10.8	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		17.0		15.3	ns
d_{TLHHS}	Delta Low to High, Hi Slew		TBD		TBD	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		TBD		TBD	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		TBD		TBD	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		TBD		TBD	ns/pF
I/O Module – CMOS Output Timing[1]						
t_{DHS}	Data to Pad, High Slew		9.3		7.9	ns
t_{DLS}	Data to Pad, Low Slew		17.5		14.9	ns
t_{ENZHS}	Enable to Pad, Z to H/L, Hi Slew		7.8		6.6	ns
t_{ENZLS}	Enable to Pad, Z to H/L, Lo Slew		13.3		11.3	ns
t_{ENHSZ}	Enable to Pad, H/L to Z, Hi Slew		12.0		10.0	ns
t_{ENLSZ}	Enable to Pad, H/L to Z, Lo Slew		11.0		9.4	ns
t_{CKHS}	IOCLK Pad to Pad H/L, Hi Slew		13.8		12.4	ns
t_{CKLS}	IOCLK Pad to Pad H/L, Lo Slew		19.3		17.4	ns
d_{TLHHS}	Delta Low to High, Hi Slew		TBD		TBD	ns/pF
d_{TLHLS}	Delta Low to High, Lo Slew		TBD		TBD	ns/pF
d_{THLHS}	Delta High to Low, Hi Slew		TBD		TBD	ns/pF
d_{THLLS}	Delta High to Low, Lo Slew		TBD		TBD	ns/pF

Note:
1. Delays based on 35pF loading.

**Actel is offering "Advanced Information" only on '–1' Speed devices. Consult Actel for '–1' device availability.*

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A14100A Timing Characteristics (continued)

(Worst-Case Commercial Conditions)

		Preliminary Information		Advanced Information*		
Dedicated (Hard-Wired) I/O Clock Network		**'Std' Speed**		**'–1' Speed**		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{IOCKH}	Input Low to High (Pad to I/O Module Input)		3.5		3.0	ns
t_{IOPWH}	Minimum Pulse Width High	4.8		4.1		ns
t_{IOPWL}	Minimum Pulse Width Low	4.8		4.1		ns
t_{IOSAPW}	Minimum Asynchronous Pulse Width	3.8		3.3		ns
t_{IOCKSW}	Maximum Skew		0.8		0.7	ns
t_{IOP}	Minimum Period	10.0		8.5		ns
f_{IOMAX}	Maximum Frequency		100		120	MHz
Dedicated (Hard-Wired) Array Clock Network						
t_{HCKH}	Input Low to High (Pad to S-Module Input)		5.5		4.7	ns
t_{HCKL}	Input High to Low (Pad to S-Module Input)		5.5		4.7	ns
t_{HPWH}	Minimum Pulse Width High	4.8		4.1		ns
t_{HPWL}	Minimum Pulse Width Low	4.8		4.1		ns
t_{HCKSW}	Maximum Skew		0.8		0.7	ns
t_{HP}	Minimum Period	10.0		8.5		ns
f_{HMAX}	Maximum Frequency		100		120	MHz
Routed Array Clock Networks						
t_{RCKH}	Input Low to High (FO=256)		9.0		7.7	ns
t_{RCKL}	Input High to Low (FO=256)		9.0		7.7	ns
t_{RPWH}	Min. Pulse Width High (FO=256)	6.1		5.4		ns
t_{RPWL}	Min. Pulse Width Low (FO=256)	6.1		5.4		ns
t_{RCKSW}	Maximum Skew (FO=128)		1.8		1.6	ns
t_{RP}	Minimum Period (FO=256)	12.5		11.1		ns
f_{RMAX}	Maximum Frequency (FO=256)		80		90	MHz
Clock-to-Clock Skews						
$t_{IOHCKSW}$	I/O Clock to H-Clock Skew	0.0	3.5	0.0	3.5	ns
$t_{IOHCKSW}$	I/O Clock to R-Clock Skew	0.0	5.0	0.0	5.0	ns
t_{HRCKSW}	H-Clock to R-Clock Skew	0.0	3.0	0.0	3.0	ns

Note:
1. Delays based on 35pF loading.

**Actel is offering "Advanced Information" only on '–1' Speed devices. Consult Actel for '–1' device availability.*

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Macro Library

Hard Macros—Combinatorial

Function	Macro	Description	Modules S	Modules C
ACT 3 Combinatorial Logic Module	CM8	Combinational Module (Full ACT 3 Logic Module)		1
ACT 3 Sequential Logic Module	DFM8A	4-bit D-Type Flip-Flop with Multiplexed Data, active low Clear, and active high clock	1	
	DFM8B	4-bit D-Type Flip-Flop with Multiplexed Data, active low Clear, and active low clock	1	
Adder	FA1A	1-bit adder, carry in and carry out active low, A-input active low		2
	FA1B	1-bit adder, carry in and carry out active low		2
	FA2A	2-bit adder, carry in and carry out active low, A0 and A1 inputs active low		2
	HA1	Half-Adder		2
	HA1A	Half-Adder with active low A-input		2
	HA1B	Half-Adder with active low carry out and sum		2
	HA1C	Half-Adder with active low carry out		2
AND	AND2	2-input AND		1
	AND2A	2-input AND with active low A-input		1
	AND2B	2-input AND with active low inputs		1
	AND3	3-input AND		1
	AND3A	3-input AND with active low A-input		1
	AND3B	3-input AND with active low A- and B-inputs		1
	AND3C	3-input AND with active low inputs		1
	AND4	4-input AND		1
	AND4A	4-input AND with active low A-input		1
	AND4B	4-input AND with active low A- and B-inputs		1
	AND4C	4-input AND with active low A-, B-, and C-inputs		1
	AND4D	4-input AND with active low inputs		2
	AND5B	5-input AND with active low A- and B-inputs		1
AND-OR	AO1	3-input AND-OR		1
	AO10	5-input AND-OR-AND		1
	AO11	3-input AND-OR		1
	AO1A	3-input AND-OR with active low A-input		1
	AO1B	3-input AND-OR with active low C-input		1
	AO1C	3-input AND-OR with active low A- and C-inputs		1
	AO1D	3-input AND-OR with active low A- and B-inputs		1
	AO1E	3-input AND-OR with active low inputs		1
	AO2	4-input AND-OR		1
	AO2A	4-input AND-OR with active low A-input		1
	AO2B	4-input AND-OR with active low A- and B-inputs		1
	AO2C	4-input AND-OR with active low A- and C-inputs		1
	AO2D	4-input AND-OR with active low A-, B-, and C-inputs		1
	AO2E	4-input AND-OR with active low inputs		1
	AO3	4-input AND-OR		1
	AO3A	4-input AND-OR		1
	AO3B	4-input AND-OR		1
	AO3C	4-input AND-OR		1
	AO4A	4-input AND-OR		1
	AO5A	4-input AND-OR		1
	AO6	2-wide 4-input AND-OR		1

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Actel

Hard Macros—Combinatorial (continued)

Function	Macro	Description	Modules S	Modules C
AND-OR	AO6A	2-wide 4-input AND-OR with active low D-input		1
	AO7	5-input AND-OR		1
	AO8	5-input AND-OR with active low C- and D-inputs		1
	AO9	5-input AND-OR		1
	AOI1	3-input AND-OR-INVERT		1
	AOI1A	3-input AND-OR-INVERT with active low A-input		1
	AOI1B	3-input AND-OR-INVERT with active low C-input		1
	AOI1C	3-input AND-OR-INVERT with active low A- and B-inputs		1
	AOI1D	3-input AND-OR-INVERT with active low inputs		1
	AOI2A	4-input AND-OR-INVERT with active low A-input		1
	AOI2B	4-input AND-OR-INVERT with active low A- and C-inputs		1
	AOI3A	4-input AND-OR-INVERT with active low inputs		1
	AOI4	2-wide 4-input AND-OR-INVERT		2
	AOI4A	2-wide 4-input AND-OR-INVERT with active low C-input		1
AND-XOR	AX1	3-input AND-XOR with active low A-input		1
	AX1A	3-input AND-XOR-INVERT with active low A-input		2
	AX1B	3-input AND-XOR with active low A- and B-inputs		1
	AX1C	3-input AND-XOR		1
Buffer	BUF	Buffer, with active high input and output		1
	BUFA	Buffer, with active low input and output		1
Clock Net	CLKINT	Clock Net Interface	0	0
	GAND2	2-input AND Clock Net		1
	GMX4	4-to-1 Multiplexor Clock Net		1
	GNAND2	2-input NAND Clock Net		1
	GNOR2	2-input NOR Clock Net		1
	GOR2	2-input OR Clock Net		1
	GXOR2	2-input Exclusive OR Clock Net		1
Inverter	INV	Inverter with active low output		1
	INVA	Inverter with active low input		1
Majority	MAJ3	3-input complex AND-OR		1
MUX	MX2	2-to-1 Multiplexor		1
	MX2A	2-to-1 Multiplexor with active low A-input		1
	MX2B	2-to-1 Multiplexor with active low B-input		1
MUX	MX2C	2-to-1 Multiplexor with active low output		1
	MX4	4-to-1 Multiplexor		1
	MXC1	Boolean		2
	MXT	Boolean		2
NAND	NAND2	2-input NAND		1
	NAND2A	2-input NAND with active low A-input		1
	NAND2B	2-input NAND with active low inputs		1
	NAND3	3-input NAND		1
	NAND3A	3-input NAND with active low A-input		1
	NAND3B	3-input NAND with active low A- and B-inputs		1
	NAND3C	3-input NAND with active low inputs		1
	NAND4	4-input NAND		2
	NAND4A	4-input NAND with active low A-input		1
	NAND4B	4-input NAND with active low A- and B-inputs		1
	NAND4C	4-input NAND with active low A-, B-, and C-inputs		1
	NAND4D	4-input NAND with active low inputs		1

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Hard Macros—Combinatorial (continued)

Function	Macro	Description	Modules S	Modules C
NAND	NAND5C	5-input NAND with active low A-, B-, and C-inputs		1
NOR	NOR2	2-input NOR		1
NOR	NOR2A	2-input NOR with active low A-input		1
	NOR2B	2-input NOR with active low inputs		1
	NOR3	3-input NOR		1
	NOR3A	3-input NOR with active low A-input		1
	NOR3B	3-input NOR with active low A- and B-inputs		1
	NOR3C	3-input NOR with active low inputs		1
	NOR4	4-input NOR		2
	NOR4A	4-input NOR with active low A-input		1
	NOR4B	4-input NOR with active low A- and B-inputs		1
	NOR4C	4-input NOR with active low A-, B-, and C-inputs		1
	NOR4D	4-input NOR with active low inputs		1
	NOR5C	5-input NOR with active low A-, B-, and C-inputs		1
OR	OR2	2-input OR		1
	OR2A	2-input OR with active low A-input		1
	OR2B	2-input OR with active low inputs		1
	OR3	3-input OR		1
	OR3A	3-input OR with active low A-input		1
	OR3B	3-input OR with active low A- and B-inputs		1
	OR3C	3-input OR with active low inputs		1
	OR4	4-input OR		1
	OR4A	4-input OR with active low A-input		1
	OR4B	4-input OR with active low A- and B-input		1
	OR4C	4-input OR with active low A-, B-, and C-inputs		1
	OR4D	4-input OR with active low inputs		2
	OR5B	5-input OR with active low A- and B-inputs		1
OR-AND	OA1	3-input OR-AND		1
	OA1A	3-input OR-AND with active low A-input		1
	OA1B	3-input OR-AND with active low C-input		1
	OA1C	3-input OR-AND with active low A- and C-inputs		1
	OA2	2-wide 4-input OR-AND		1
	OA2A	2 wide 4-input OR-AND with active low A-input		1
	OA3	4-input OR-AND		1
	OA3A	4-input OR-AND with active low C-input		1
	OA3B	4-input OR-AND with active low A- and C-inputs		1
	OA4	4-input OR-AND		1
	OA4A	4-input OR-AND with active low C-input		1
	OA5	4-input complex OR-AND		1
	OAI1	3-input OR-AND-INVERT		1
	OAI2A	4-input OR-AND-INVERT with active low D-input		1
	OAI3	4-input OR-AND-INVERT		1
	OAI3A	4-input OR-AND-INVERT with active low C- and D-inputs		1
XNOR	XNOR	2-input XNOR		1
XNOR-AND	XA1A	3-input XNOR-AND		1
XNOR-OR	XO1A	3-input XNOR-OR		1
XOR	XOR	2-input XOR		1
XOR-AND	XA1	3-input XOR-AND		1
XOR-OR	XO1	3-input XOR-OR		1

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Hard Macros—Sequential

Function	Macro	Description	Modules S	Modules C
D-Type	DF1	D-Type Flip-Flop	1	
	DF1A	D-Type Flip-Flop with active low output	1	
	DF1B	D-Type Flip-Flop with active low clock	1	
	DF1C	D-Type Flip-Flop with active low clock and output	1	
	DFC1	D-Type Flip-Flop with active high Clear	1	1
	DFC1A	D-Type Flip-Flop with active high Clear and active low clock	1	1
	DFC1B	D-Type Flip-Flop with active low Clear	1	
	DFC1D	D-Type Flip-Flop with active low Clear and clock	1	
	DFE	D-Type Flip-Flop with active high Enable	1	
	DFE1B	D-Type Flip-Flop with active low Enable	1	
	DFE1C	D-Type Flip-Flop with active low Enable and clock	1	
	DFE3A	D-Type Flip-Flop with Enable and active low Clear	1	
	DFE3B	D-Type Flip-Flop with Enable and active low Clear and clock	1	
	DFE3C	D-Type Flip-Flop with active low Enable and Clear	1	
	DFE3D	D-Type Flip-Flop with active low Enable, Clear, and clock	1	
	DFEA	D-Type Flip-Flop with Enable and active low clock	1	
	DFM	2-bit D-Type Flip-Flop with Multiplexed Data	1	
	DFM1B	2-bit D-Type Flip-Flop with Multiplexed Data and active low output	1	
	DFM1C	2-bit D-Type Flip-Flop with Multiplexed Data and active low clock and output	1	
	DFM3	2-bit D-Type Flip-Flop with Multiplexed Data and Clear	1	1
	DFM3B	2-bit D-Type Flip-Flop with Multiplexed Data and active low Clear and clock	1	
	DFM3E	2-bit D-Type Flip-Flop with Multiplexed Data, Clear, and active low clock	1	1
	DFM4C	2-bit D-Type Flip-Flop with Multiplexed Data and active low Preset and output	1	
	DFM4D	2-bit D-Type Flip-Flop with Multiplexed Data and active low Preset, clock, and output	1	
	DFM6A	4-bit D-Type Flip-Flop with Multiplexed Data, active low Clear, and active high Clock	1	
	DFM6B	4-bit D-Type Flip-Flop with Multiplexed Data, active low Clear, and clock	1	
	DFM7A	4-bit D-Type Flip-Flop with Multiplexed Data, active low Clear, and active high clock	1	
	DFM7B	4-bit D-Type Flip-Flop with Multiplexed Data, active low Clear and clock	1	
	DFMA	2-bit D-Type Flip-Flop with Multiplexed Data and active low clock	1	
	DFMB	2-bit D-Type Flip-Flop with Multiplexed Data and active low Clear	1	
	DFME1A	2-bit D-Type Flip-Flop with Multiplexed Data and active low Enable	1	
	DFP1	D-Type Flip-Flop with active high Preset		2
	DFP1A	D-Type Flip-Flop with active high Preset and active low clock		2
	DFP1B	D-Type Flip-Flop with active low Preset		2
	DFP1C	D-Type Flip-Flop with active high Preset and active low output	1	1
	DFP1D	D-Type Flip-Flop with active low Preset and clock		2
	DFP1E	D-Type Flip-Flop with active low Preset and output	1	
	DFP1F	D-Type Flip-Flop with active high Preset and active low clock and output	1	1
	DFP1G	D-Type Flip-Flop with active low Preset, clock, and output	1	
	DFPC	D-Type Flip-Flop with active high Preset, active low Clear, and active high clock		2
	DFPCA	D-Type Flip-Flop with active high Preset, and active low Clear and clock		2
J-K Type	JKF	JK Flip-Flop with active low K-input	1	

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Hard Macros—Sequential (continued)

Function	Macro	Description	Modules S	Modules C
J-K Type	JKF1B	JK Flip-Flop with active low clock and K-input	1	
	JKF2A	JK Flip-Flop with active low Clear and K-input	1	
	JKF2B	JK Flip-Flop with active low Clear, clock, and K-input	1	
	JKF2C	JK Flip-Flop with active high Clear and active low K-input	1	1
	JKF2D	JK Flip-Flop with active high Clear and active low clock and K-input	1	1
T-Type	TF1A	T-Type Flip-Flop with active low Clear	1	
	TF1B	T-Type Flip-Flop with active low Clear and clock	1	
Latch	DL1	Data Latch	1	
	DL1A	Data Latch with active low output	1	
	DL1B	Data Latch with active low clock	1	
	DL1C	Data Latch with active low clock and output	1	
	DLC	Data Latch with active low Clear	1	
	DLC1	Data Latch with active high Clear		1
	DLC1A	Data Latch with active high Clear and active low clock		1
	DLC1F	Data Latch with active high Clear and active low output		1
	DLC1G	Data Latch with active high Clear and active low clock and output		1
	DLCA	Data Latch with active low Clock and Clear	1	
	DLE	Data Latch with active high Enable	1	
	DLE1D	Data Latch with active high Enable and clock and active low input and output	1	
	DLE2B	Data Latch with active low Enable, Clear, and clock	1	
	DLE2C	Data Latch with active low Enable and clock and active high Clear		1
	DLE3B	Data Latch with active low Enable and clock and active low Preset		1
	DLE3C	Data Latch with active low Enable, Preset, and clock		1
	DLEA	Data Latch with active low Enable and active high clock	1	
	DLEB	Data Latch with active high Enable and active high clock	1	
	DLEC	Data Latch with active low Enable and clock	1	
	DLM	2-bit Data Latch with Multiplexed Data	1	
	DLM3	4-bit Data Latch with Multiplexed Data	1	
	DLM3A	4-bit Data Latch with Multiplexed Data and active low clock	1	
	DLM4	Data Latch with Multiplexed Data	1	
	DLM4A	Data Latch with Multiplexed Data	1	
	DLMA	2-bit Data Latch with Multiplexed Data, and active low clock	1	
	DLME1A	2-bit Data Latch with Multiplexed Data and Enable and active low clock	1	
	DLP1	Data Latch with active high Preset and clock		1
	DLP1A	Data Latch with active high Preset and active low clock		1
	DLP1B	Data Latch with active low Preset and active high clock		1
	DLP1C	Data Latch with active low Preset and clock		1
	DLP1D	Data Latch with active low Preset and output and active high clock	1	
	DLP1E	Data Latch with active low Preset, clock, and output	1	

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Input/Output Macros

Function	Macro	Description	I/O Modules
Buffer	BBHS	Bidirectional Buffer, High Slew	1
	BBUFTH	Bidirectional Buffer, Tristate Enable, High Slew	1
	BBUFTL	Bidirectional Buffer, Tristate Enable, Low Slew	1
	BIBUF	Bidirectional Buffer, High Slew (with hidden buffer at Y pin)	1
	HCLKBUF	Dedicated High-Speed S-Module Clock Buffer	1
	IBUF	Input Buffer	1
	INBUF	Input Buffer	1
	IOCLKBUF	Dedicated I/O Module Clock Buffer	1
	IOPCLBUF	Dedicated I/O Module IOPCL Buffer	1
	OBHS	Output buffer, High Slew	1
	OBUFTH	Output Buffer, Tristate Enable, High Slew	1
	OBUFTL	Output Buffer, Tristate Enable, Low Slew	1
	OUTBUF	Output Buffer, High Slew	1
Bidirectional	BRECTH	Bidirectional, Output Register with Clear, Data Enable, Tristate Enable, High Slew	1
	BRECTL	Bidirectional, Output Register with Clear, Data Enable, Tristate Enable, Low Slew	1
	BREPTH	Bidirectional, Output Register with Preset, Data Enable, Tristate Enable, High Slew	1
	BREPTL	Bidirectional, Output Register with Preset, Data Enable, Tristate Enable, Low Slew	1
	CLKBIBUF	Bidirectional with Input Dedicated to Clock Network	1
	DECETH	Bidirectional, Double Registered with Clear, Data Enable, Tristate Enable, High Slew	1
	DECETL	Bidirectional, Double Registered with Clear, Data Enable, Tristate Enable, Low Slew	1
	DEPETH	Bidirectional, Double Registered with Preset, Data Enable, Tristate Enable, High Slew	1
	DEPETL	Bidirectional, Double Registered with Preset, Data Enable, Tristate Enable, Low Slew	1
Input	CLKBUF	Input for Dedicated Routed Clock Network	1
	IREC	Input Register with Clear	1
	IREP	Input Register with Preset	1
Output	FECTMH	Output Register with Muxed Feedback, Clear, Data Enable, Tristate Enable, High Slew	1
	FECTML	Output Register with Muxed Feedback, Clear, Data Enable, Tristate Enable, Low Slew	1
	FEPTMH	Output Register with Muxed Feedback, Preset, Data Enable, Tristate Enable, High Slew	1
	FEPTML	Output Register with Muxed Feedback, Preset, Data Enable, Tristate Enable, Low Slew	1
	ORECTH	Output Register with Clear, Data Enable, Tristate Enable, High Slew	1
	ORECTL	Output Register with Clear, Data Enable, Tristate Enable, Low Slew	1
	OREPTH	Output Register with Preset, Data Enable, Tristate Enable, High Slew	1
	OREPTL	Output Register with Preset, Data Enable, Tristate Enable, Low Slew	1
	TBHS	Tristate output, High Slew	1
	TRIBUFF	Tristate output, High Slew	1

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Soft Macros

Function	Macro	Description	Maximum Logic Levels	Modules S	Modules C
Adder	FADD10	10-bit adder	3		56
	FADD12	12-bit adder	4		9
	FADD16	16-bit adder	5		97
	FADD8	8-bit adder	4		44
	FADD9	9-bit adder with active low carry out	3		49
	VAD16C	Very fast 16-bit adder, no Carry in	3		97
	VADC16C	Very fast 16-bit adder with Carry in	3		97
Comparator	ICMP4	4-bit Identity Comparator	2		5
	ICMP8	8-bit Identity Comparator	3		9
	MCMPC2	2-bit Magnitude Comparator with Enable	3		9
	MCMPC4	4-bit Magnitude Comparator with Enable	4		18
	MCMPC8	8-bit Magnitude Comparator with Enable	6		36
Counter	CNT4A	4-bit binary counter with load and clear	4	4	8
	CNT4B	4-bit binary counter with load, clear, carry-in, carry-out	4	4	7
	FCTD16C	Fast 16-bit Down Counter, parallel loadable	2	19	33
	FCTD8A	Fast 8-bit Down Counter, parallel loadable	1	10	18
	FCTD8B	Fast 8-bit Down Counter, parallel loadable	1	9	13
	FCTU16C	Fast 16-bit Up Counter, parallel loadable	2	19	31
	FCTU8A	Fast 8-bit Up Counter, parallel loadable	1	10	17
	FCTU8B	Fast 8-bit Up Counter, parallel loadable	1	9	12
	UDCNT4A	4-bit up/down counter with load, carry-in, and carry-out	5	4	13
	VCTD16C	Very fast 16-bit down counter, delay after load, registered control inputs	1	34	41
	VCTD2CP	2-bit down counter, prescaler, delay after load, use to build VCTD counters	1	5	2
	VCTD2CU	2-bit down counter, upper bits, delay after load, use to build VCTD counters	1	2	3
	VCTD4CL	4-bit down counter, lower bits, delay after load, use to build VCTD counters	1	4	7
	VCTD4CM	4-bit down counter, middle bits, delay after load, use to build VCTD counters	1	4	8
Decoder	DEC2X4	2-to-4 decoder	1		4
	DEC2X4A	2-to-4 decoder with active low outputs	1		4
	DEC3X8	3-to-8 decoder	1		8
	DEC3X8A	3-to-8 decoder with active low outputs	1		8
	DEC4X16A	4-to-16 decoder with active low outputs	2		20
	DECE2X4	2-to-4 decoder with enable	1		4
	DECE2X4A	2-to-4 decoder with enable and active low outputs	1		4
	DECE3X8	3-to-8 decoder with enable	2		11
	DECE3X8A	3-to-8 decoder with enable and active low outputs	2		11
Latch	DLC8A	octal latch with clear active low 8-bit Data Latch with active low Clear	1	8	
	DLE8	octal latch with enable 8-bit Data Latch with active high Enable	1	8	
	DLM8	octal latch with multiplexed data 8-bit Data Latch with Multiplexed Data	1	8	
MUX	MX16	16-to-1 Multiplexor	2		5
	MX8	8-to-1 Multiplexor with active high output	2		3
	MX8A	8-to-1 Multiplexor with active low output	2		3
Multiplier	SMULT8	8-bit by 8-bit Multiplier			242
Shift Register	SREG4A	4-bit shift register with clear active low	1	4	
	SREG8A	8-bit shift register with clear active low	1	8	

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Actel

Soft Macros—TTL Equivalent

Function	Macro	Description	Maximum Logic Levels	Modules S	Modules C
	TA00	2-input NAND	1		1
	TA02	2-input NOR	1		1
	TA04	Inverter	1		1
	TA07	Buffer	1		1
	TA08	2-input AND	1		1
	TA10	3-input NAND	1		1
	TA11	3-input AND	1		1
	TA138	3-to-8 decoder with enable and active low outputs	2		12
	TA139	2-to-4 decoder with active low enable and outputs	1		4
	TA150	16-to-1 multiplexor with active low enable	3		6
	TA151	8-to-1 multiplexor with enable and both active low and active high output	3		5
	TA153	4-to-1 multiplexor with active low enable	2		2
	TA154	4-to-16 decoder with active low outputs and select lines	2		22
	TA157	2-to-1 multiplexor with active low enable	1		1
	TA160	4-bit decade counter with active low clear and load	4	4	8
	TA161	4-bit binary counter with active low clear and load	3	4	6
	TA164	8-bit serial in, parallel out shift register, active low clear	1	8	
	TA169	4-bit Up/Down Counter	6	4	14
	TA174	hex D-type flip-flop with active low clear	1	6	
	TA175	quadruple D-type flip-flop with active low clear	1	4	
	TA181	ALU			37
	TA190	4-bit up/down decode counter with up/down mode	7	4	31
	TA191	4-bit up/down binary counter with up/down mode	7	4	30
	TA194	4-bit bidirectional universal shift register	1	4	4
	TA195	4-bit parallel-access shift register	1	4	1
	TA20	4-input NAND	1		2
	TA21	4-input AND	1		1
	TA269	8-bit up/down binary counter	8	8	28
	TA27	3-input NOR	1		1
	TA273	octal register with clear	1	8	
	TA280	9-bit odd/even parity generator and checker	4		9
	TA32	2-input OR	1		1
	TA377	octal register with active low enable	1	8	
	TA40	4-input NAND	1		2
	TA42	4 to 10 decoder	1		10
	TA51	AND-OR-Invert	1		2
	TA54	4-wide 2-input AND-OR-Invert	2		5
	TA55	2-wide 4-input AND-OR-Invert	2		3
	TA688	8-bit identity comparator	3		9
	TA86	2-input exclusive OR	1		1

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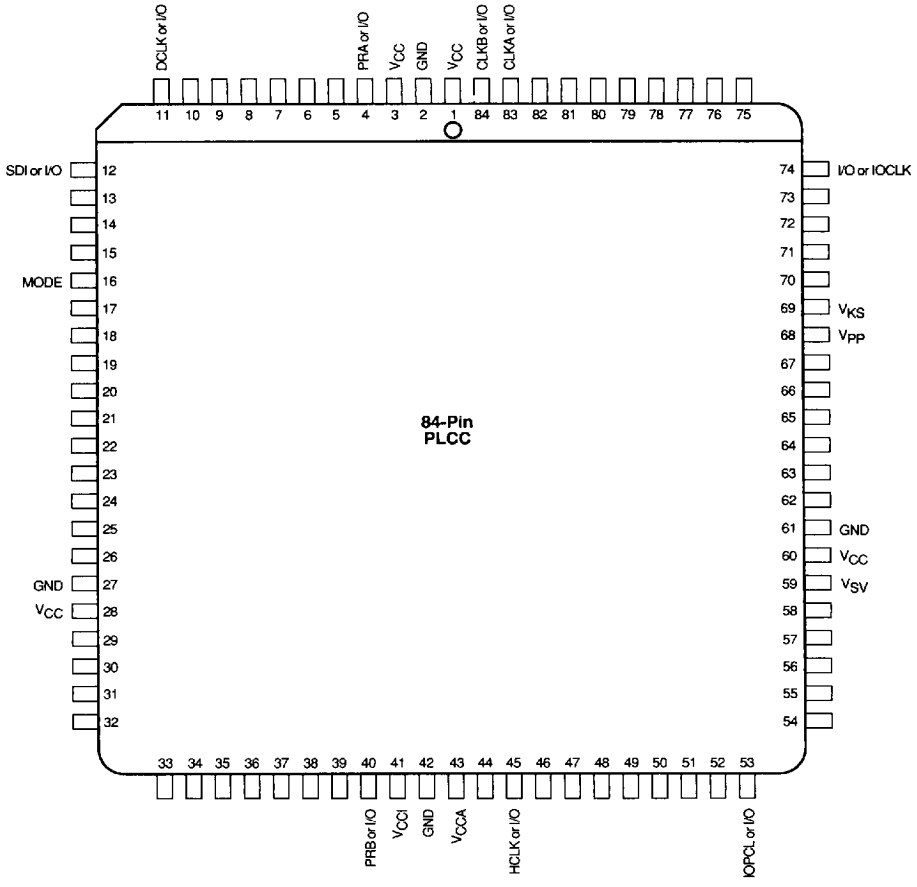
Package Pin Assignments

84-Pin PLCC (Top View)



Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE must be terminated to circuit ground, except during device programming or debugging.
4. $V_{PP} = V_{CC}$, except during device programming.
5. $V_{SV} = V_{CC}$, except during device programming.
6. V_{KS} = GND, except during device programming.

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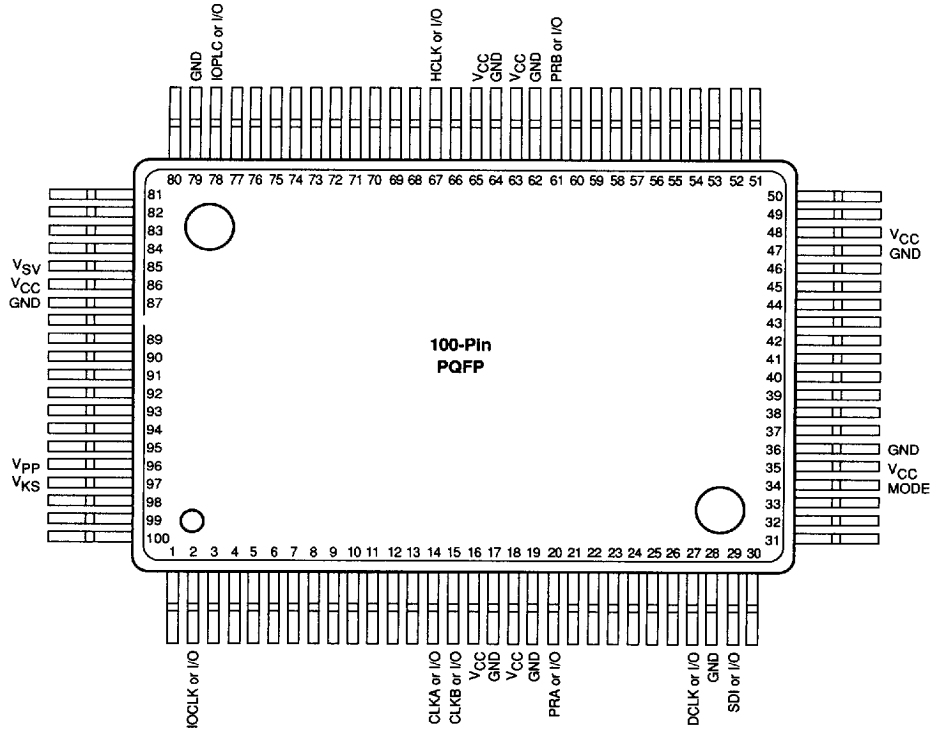
Package Pin Assignments (continued)

100-Pin PQFP (Top View)



Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE must be terminated to circuit ground, except during device programming or debugging.
4. $V_{PP} = V_{CC}$, except during device programming.
5. $V_{SV} = V_{CC}$, except during device programming.
6. V_{KS} = GND, except during device programming.

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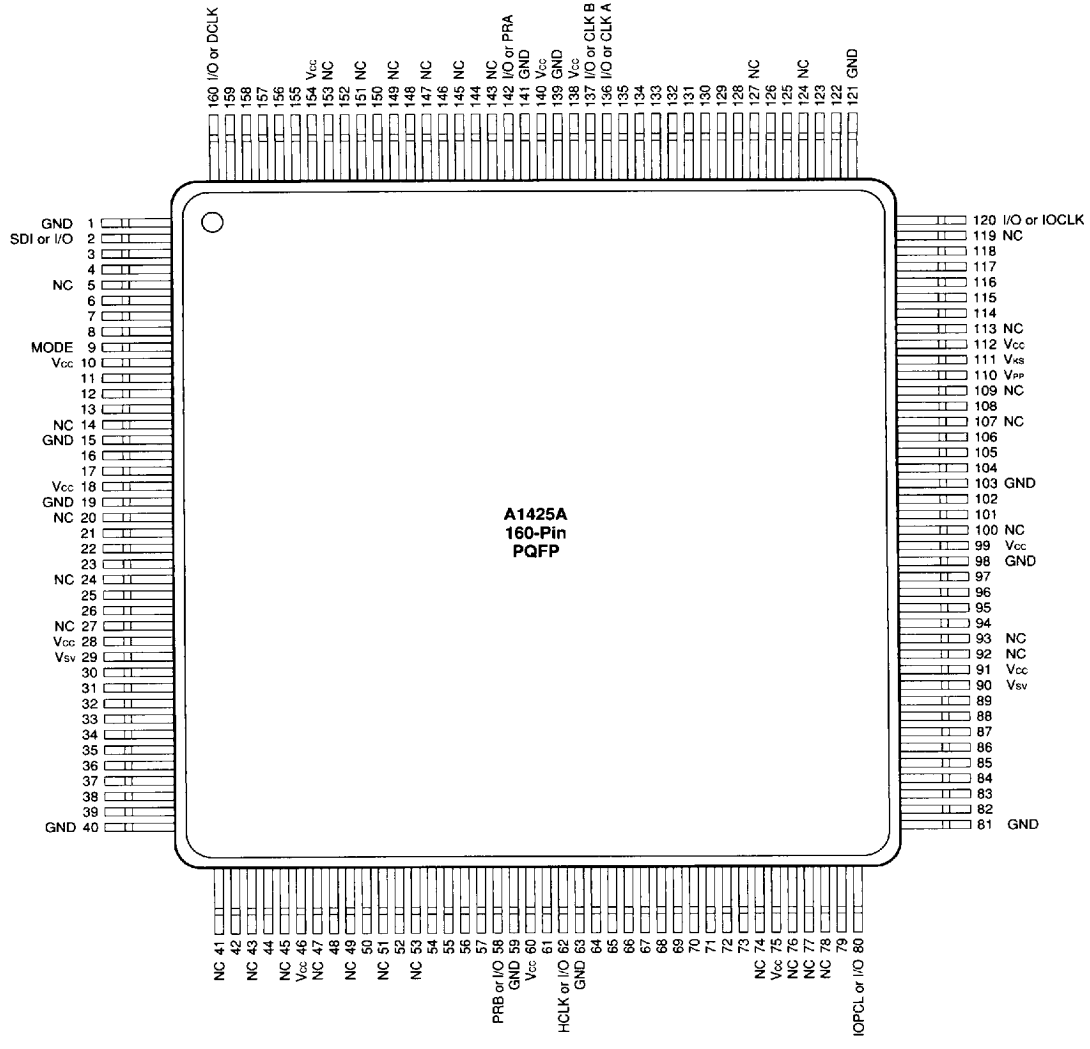
Package Pin Assignments (continued)

160-Pin PQFP (Top View)



Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE must be terminated to circuit ground, except during device programming or debugging.
4. $V_{PP} = V_{CC}$, except during device programming.
5. $V_{SV} = V_{CC}$, except during device programming.
6. V_{KS} = GND, except during device programming.

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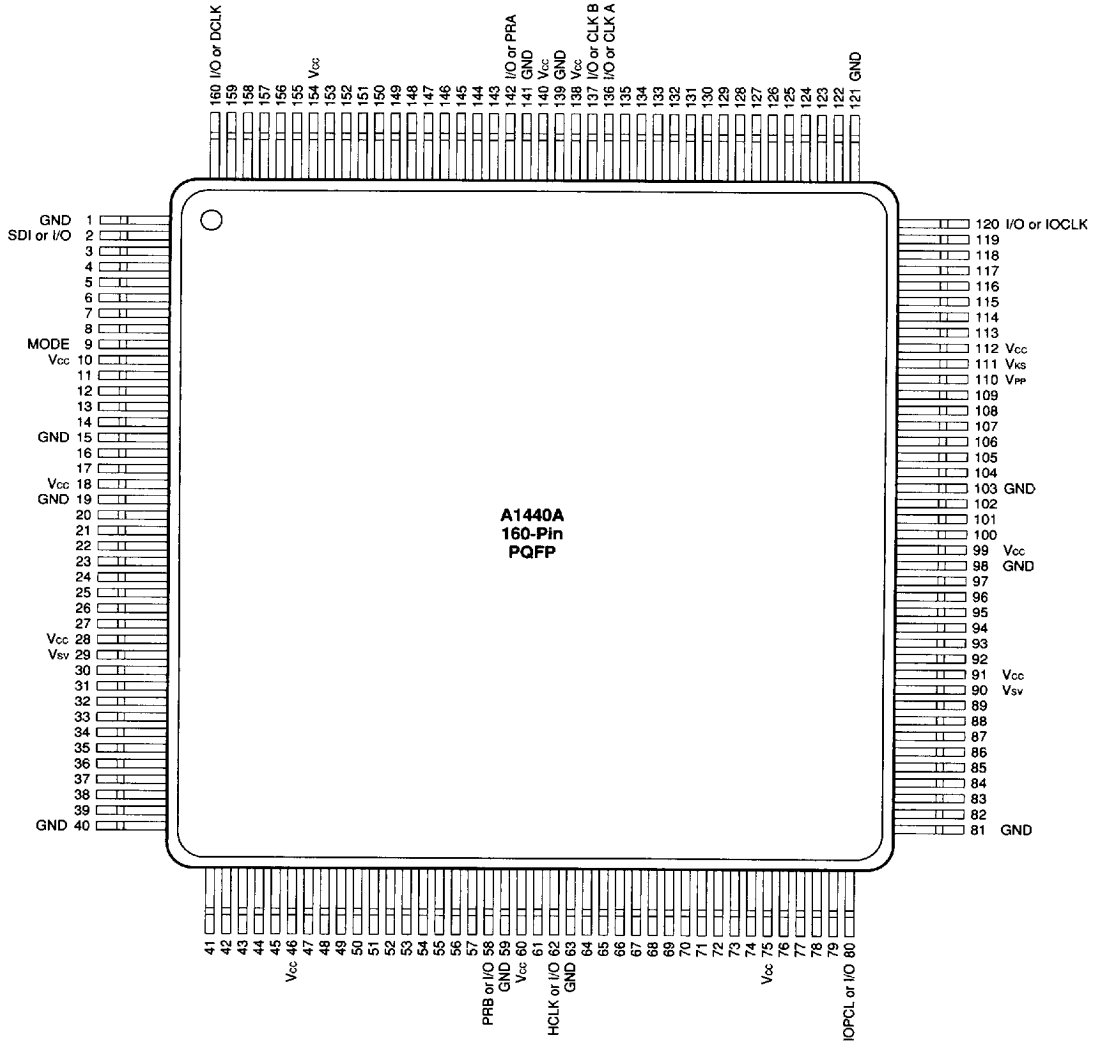
Package Pin Assignments (continued)

160-Pin PQFP (Top View)



Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE must be terminated to circuit ground, except during device programming or debugging.
4. $V_{PP} = V_{CC}$, except during device programming.
5. $V_{SV} = V_{CC}$, except during device programming.
6. V_{KS} = GND, except during device programming.

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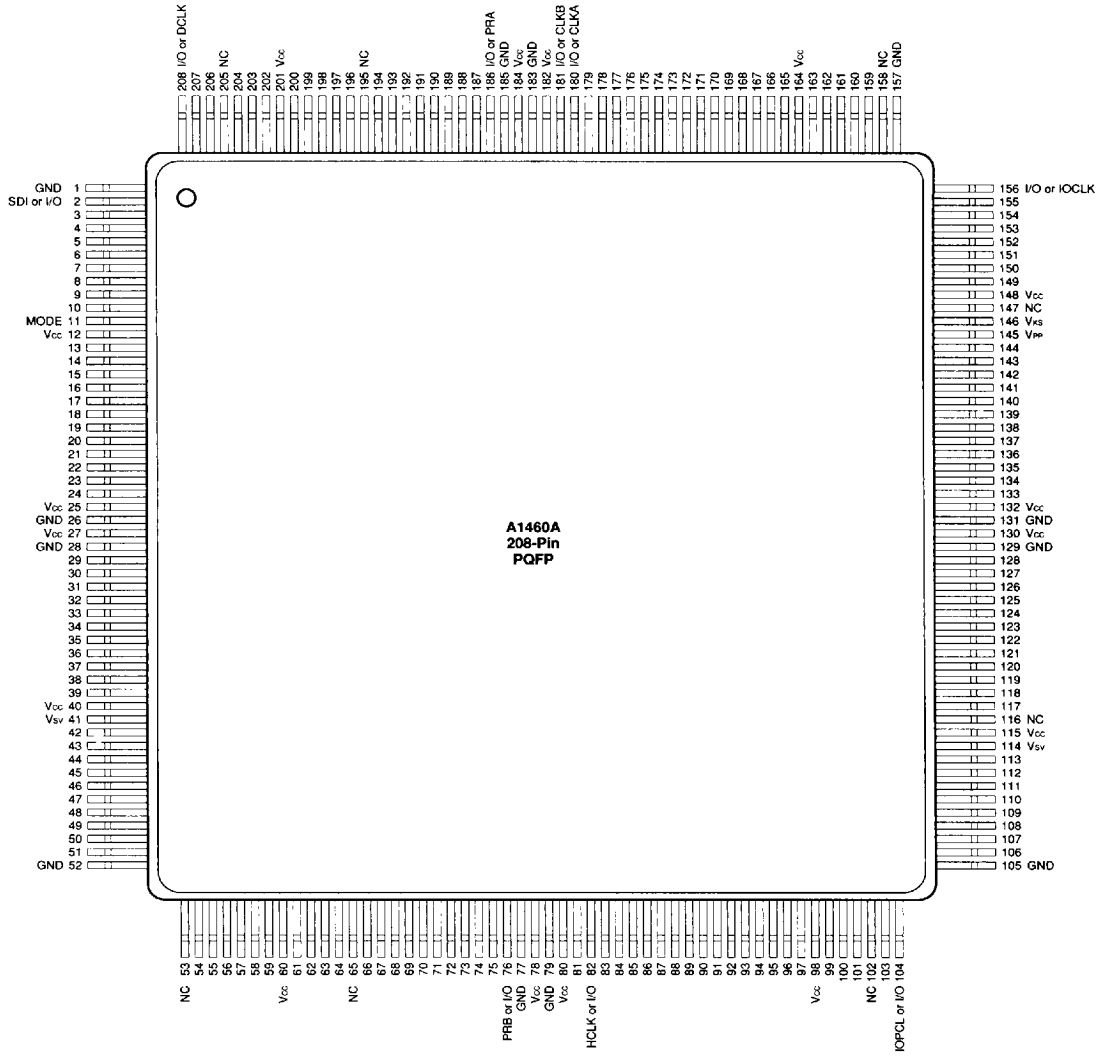
Package Pin Assignments (continued)

208-Pin PQFP (Top View)



Notes:

1. V_{PP} must be terminated to V_{CC}, except during device programming.
2. MODE must be terminated to circuit ground, except during device programming or debugging.
3. Unused I/O pins are designated as outputs by ALS and are driven low.
4. All unassigned pins are available for use as I/Os.

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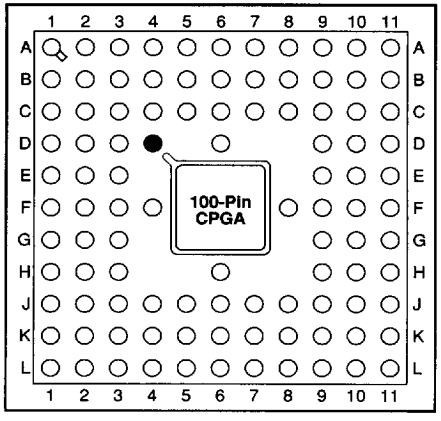
Package Pin Assignments (continued)

100-Pin CPGA (Top View)



Signal	Pad Number	Location
CLKA or I/O	94	C7
CLKB or I/O	95	D6
DCLK or I/O	107	C4
GND	1, 9, 21, 37, 39, 49, 55, 63, 75, 87, 97, 99	C3, F3, J3, C6, J6, J8, C9, F9, J9
HCLK or I/O	42	H6
IOCLK or I/O	81	C10
IOPCL or I/O	54	K9
MODE	7	C2
PRA OR I/O	100	A6
PRB or I/O	36	L3
SDI or I/O	2	B3
V_{CC}	8, 14, 22, 38, 40, 62, 68, 76, 96, 98	F2, K2, B6, K6, B10, F10, K10
V_{KS}	74	E9
V_{PP}	73	E11
V_{SV}	23, 61	G2

Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE must be terminated to circuit ground, except during device programming or debugging.
4. $V_{PP} = V_{CC}$, except during device programming.
5. $V_{SV} = V_{CC}$, except during device programming.
6. V_{KS} = GND, except during device programming.

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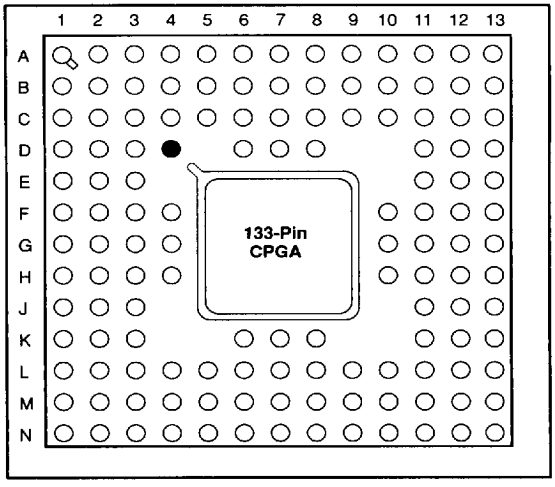
Package Pin Assignments (continued)

133-Pin CPGA (Top View)



Signal	Pad Number	Location
CLKA or I/O	115	D7
CLKB or I/O	116	B6
DCLK or I/O	134	D4
GND	1, 10, 22, 35, 36, 48, 50, 64, 68, 79, 93, 101, 106, 118, 120, 132	A2, C3, C7, C11, C12, G3, G11, L3, L7, L11, M3, N1
HCLK or I/O	53	K7
IOCLK or I/O	100	C10
IOPCL or I/O	67	L10
MODE	8	E3
NC	—	A1, A7, A13, G1, G13, N1, N7, N13
PRA OR I/O	121	A6
PRB or I/O	47	L6
SDI or I/O	2	C2
V_{CC}	9, 16, 23, 39, 49, 51, 65, 78, 84, 94, 117, 119, 127	B2, B7, B12, G2, G12, M2, M7, M12
V_{KS}	92	F10
V_{PP}	91	E11
V_{SV}	24, 77	J2, J12

Notes:
1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE must be terminated to circuit ground, except during device programming or debugging.
4. $V_{PP} = V_{CC}$, except during device programming.
5. $V_{SV} = V_{CC}$, except during device programming.
6. V_{KS} = GND, except during device programming.

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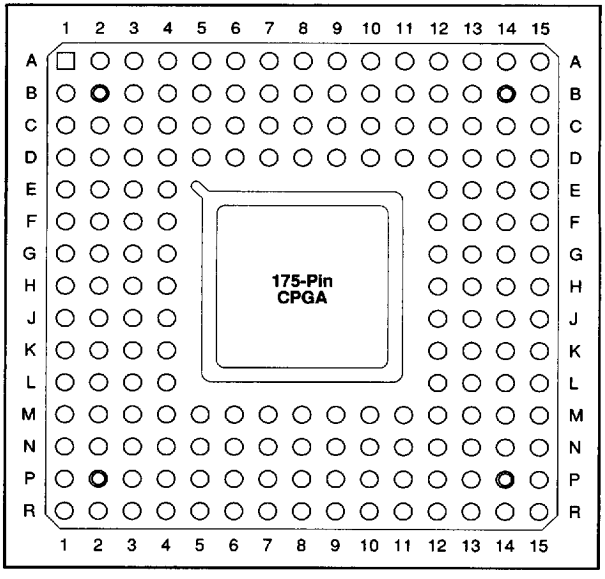
Package Pin Assignments (continued)

175-Pin CPGA (Bottom View)



Signal	Pad Number	Location
CLKA or I/O	159	C9
CLKB or I/O	160	A9
DCLK or I/O	185	D5
GND	1, 12, 22, 24, 33, 46, 47, 57, 67, 69, 80, 90, 93, 104, 113, 115, 128, 138, 139, 151, 162, 164, 175, 183	D4, D8, D11, D12, E4, H4, H12, L4, L12, M4, M8, M12
HCLK or I/O	72	R8
IOCLK or I/O	137	E12
IOPCL or I/O	92	P13
MODE	10	F3
NC	—	A2, A15, B2, B3, P2, P14, R1, R2, R14, R15
PRA OR I/O	165	B8
PRB or I/O	66	R7
SDI or I/O	2	D3
V_{CC}	11, 21, 23, 34, 53, 68, 70, 86, 103, 114, 116, 129, 144, 161, 163, 178	C3, C8, C13, H3, H13, N3, N8, N13
V_{KS}	127	E14
V_{PP}	126	E15
V_{SV}	35, 102	L1, L14

Notes:

1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE must be terminated to circuit ground, except during device programming or debugging.
4. $V_{PP} = V_{CC}$, except during device programming.
5. $V_{SV} = V_{CC}$, except during device programming.
6. V_{KS} = GND, except during device programming.

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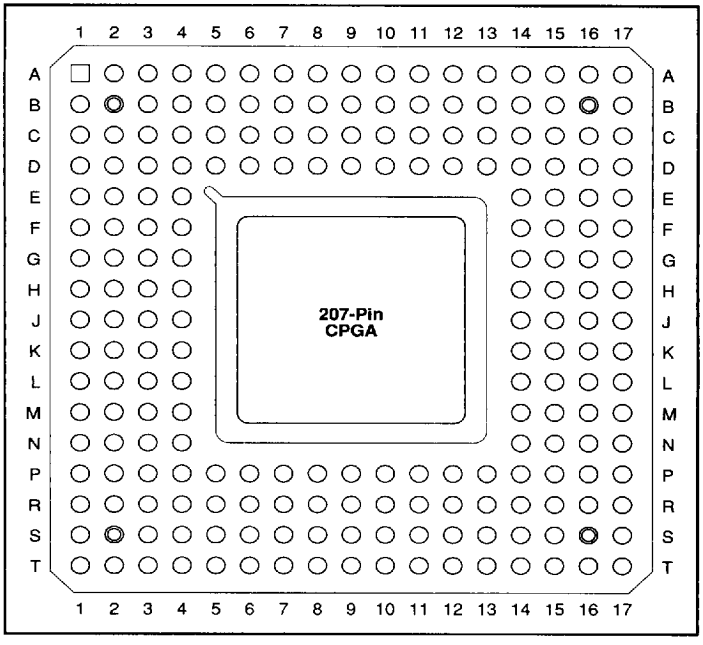
Package Pin Assignments (continued)

207-Pin CPGA (Top View)



Signal	Pad Number	Location
CLKA or I/O	185	K1
CLKB or I/O	186	J3
DCLK or I/O	213	E4
GND	1, 13, 27, 29, 41, 55, 56, 68, 80, 82, 94, 106, 109, 120, 133, 135, 151, 161, 162, 175, 188, 190, 200, 210	C15, D4, D5, D9, D14, J4, J14, P3, P4, P9, P14, R1
HCKL or I/O	85	J15
IOCLK or I/O	160	P5
IOPCL or I/O	108	N14
MODE	11	D7
NC	—	A1, A2, A16, A17, B1, B17, C1, C2, S1, S3, S17, T1, T2, T16, T17
PRA OR I/O	191	H1
PRB or I/O	79	K16
SDI or I/O	2	C3
V_{CC}	12, 26, 28, 42, 63, 81, 83, 102, 119, 134, 136, 152, 168, 187, 189, 206	B2, B9, B16, J2, J16, S2, S9, S16
V_{KS}	150	P7
V_{PP}	149	T5
V_{SV}	43, 118	D11, P12

Notes:
1. Unused I/O pins are designated as outputs by ALS and are driven low.
2. All unassigned pins are available for use as I/Os.
3. MODE must be terminated to circuit ground, except during device programming or debugging.
4. $V_{PP} = V_{CC}$, except during device programming.
5. $V_{SV} = V_{CC}$, except during device programming.
6. V_{KS} = GND, except during device programming.

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