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ADE-203-454A (Z)

HM6264B Series

8,192-word $\times$ 8-bit High Speed CMOS Static RAM**HITACHI**Rev. 1.0
Dec. 6, 1995

The Hitachi HM6264B is 64k-bit static RAM organized 8-kword $\times$ 8-bit. It realizes higher performance and low power consumption by 1.5 μ m CMOS process technology.

The device, packaged in 450 mil SOP (foot print pitch width), 600 mil plastic DIP, 300 mil plastic DIP, is available for high density mounting.

Features

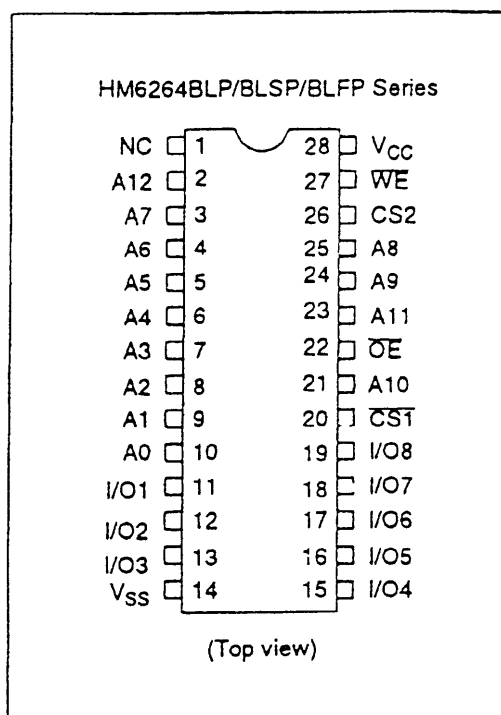
- High speed
Fast access time: 85/100 ns (max)
- Low power
Standby: 10 μ W (typ)
Operation: 15 mW (typ) ($f = 1$ MHz)
- Single 5 V supply
- Completely static memory
No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
Three state output
- Directly TTL compatible
All inputs and outputs
- Battery back up operation capability

Ordering Information

Type No.	Access time	Package
HM6264BLP-8L	85 ns	600-mil, 28-pin plastic DIP
HM6264BLP-10L	100 ns	(DP-28)
HM6264BLSP-8L	85 ns	300-mil, 28-pin plastic DIP
HM6264BLSP-10L	100 ns	(DP-28N)
HM6264BLFP-8LT	85 ns	450-mil, 28-pin plastic SOP
HM6264BLFP-10LT	100 ns	(FP-28DA)

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Pin Arrangement

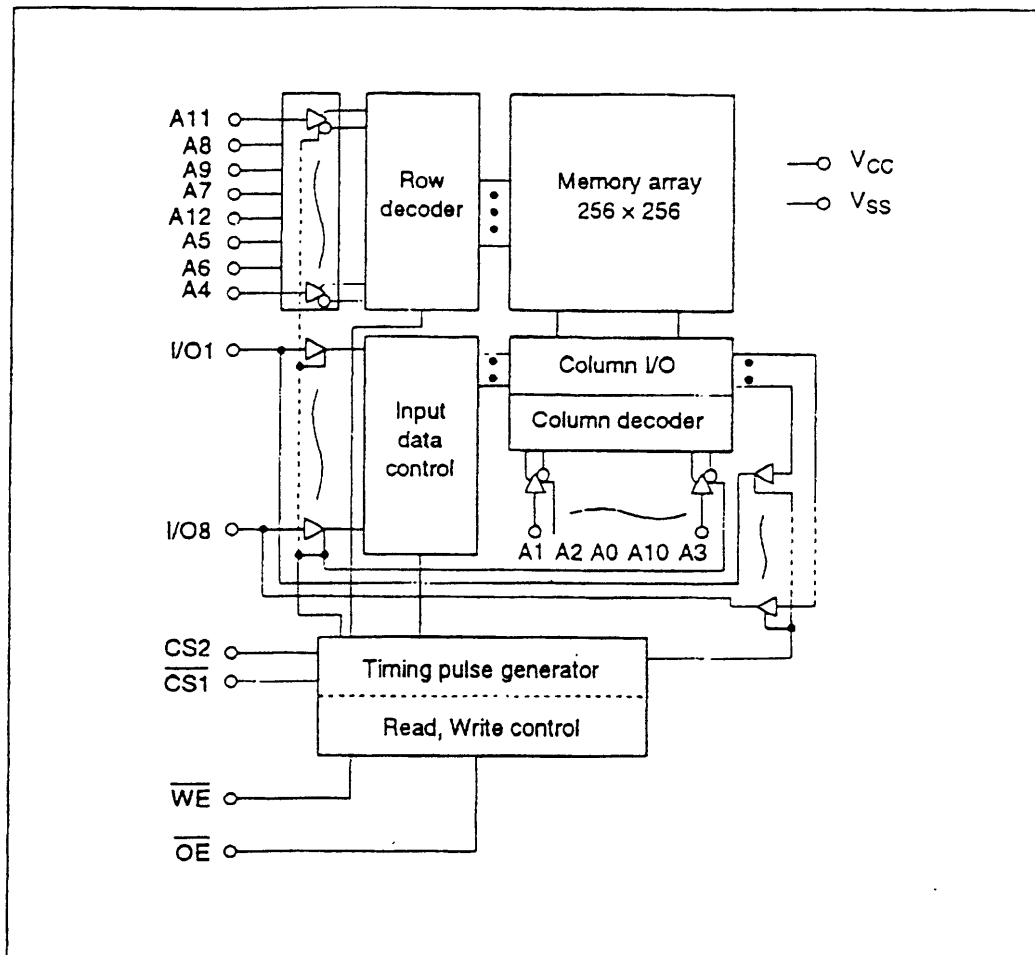


Pin Description

Symbol	Function
A0 to A12	Address input
I/O1 to I/O8	Data input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
NC	No connection
Vcc	Power supply
Vss	Ground

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Block Diagram



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Function Table

WE	CS1	CS2	OE	Mode	V _{CC} current	VO pin	Ref. cycle
x	H	x	x	Not selected(power down)	I _{SB} , I _{SB1}	High-Z	—
x	x	L	x	Not selected(power down)	I _{SB} , I _{SB1}	High-Z	—
H	L	H	H	Output disable	I _{CC}	High-Z	—
H	L	H	L	Read	I _{CC}	Dout	Read cycle (1)~(3)
L	L	H	H	Write	I _{CC}	Din	Write cycle (1)
L	L	H	L	Write	I _{CC}	Din	Write cycle (2)

Note: x: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage ^{*1}	V _{CC}	-0.5 to +7.0	V
Terminal voltage ^{*1}	V _T	-0.5 ^{*2} to V _{CC} + 0.3 ^{*3}	V
Power dissipation	P _T	1.0	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +125	°C
Storage temperature under bias	T _{bias}	-10 to +85	°C

- Notes: 1. Relative to V_{SS}
2. V_T min: -3.0 V for pulse half-width ≤ 50 ns
3. Maximum voltage is 7.0 V

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	-0.3 ^{*1}	—	0.8	V

Note: 1. V_{IL} min: -3.0 V for pulse half-width ≤ 50 ns

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DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Min	Typ ¹	Max	Unit	Test conditions
Input leakage current	$ I_{LI} $	—	—	2	μA	$V_{in} = V_{SS}$ to V_{CC}
Output leakage current	$ I_{LO} $	—	—	2	μA	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{I/O} = V_{SS}$ to V_{CC}
Operating power supply current	I_{CCDC}	—	7	15	mA	$\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, $I_{I/O} = 0\text{ mA}$ others = V_{IH}/V_{IL}
Average operating power supply current	I_{CC1}	—	30	45	mA	Min cycle, duty = 100 %, $\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, $I_{I/O} = 0\text{ mA}$ others = V_{IH}/V_{IL}
	I_{CC2}	—	3	5	mA	Cycle time = 1 μs , duty = 100 %, $I_{I/O} = 0\text{ mA}$ $\overline{CS1} \leq 0.2\text{ V}$, $CS2 \geq V_{CC} - 0.2\text{ V}$, $V_{IH} \geq V_{CC} - 0.2\text{ V}$, $V_{IL} \leq 0.2\text{ V}$
Standby power supply current	I_{SB}	—	1	3	mA	$\overline{CS1} = V_{IH}$, $CS2 = V_{IL}$
	I_{SB1}	—	2	50	μA	$\overline{CS1} \geq V_{CC} - 0.2\text{ V}$, $CS2 \geq V_{CC} - 0.2\text{ V}$ or $0\text{ V} \leq CS2 \leq 0.2\text{ V}$, $0\text{ V} \leq V_{in}$
Output low voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 2.1\text{ mA}$
Output high voltage	V_{OH}	2.4	—	—	V	$I_{OH} = -1.0\text{ mA}$

Notes: 1. Typical values are at $V_{CC} = 5.0\text{ V}$, $T_a = +25^\circ\text{C}$ and not guaranteed.Capacitance ($T_a = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance ^{*1}	C_{in}	—	—	5	pF	$V_{in} = 0\text{ V}$
Input/output capacitance ^{*1}	$C_{I/O}$	—	—	7	pF	$V_{I/O} = 0\text{ V}$

Note: 1. This parameter is sampled and not 100% tested.

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AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.8 V to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall times: 10 ns
- Output load: 1 TTL Gate + C_L (100 pF) (Including scope & jig)

Read Cycle

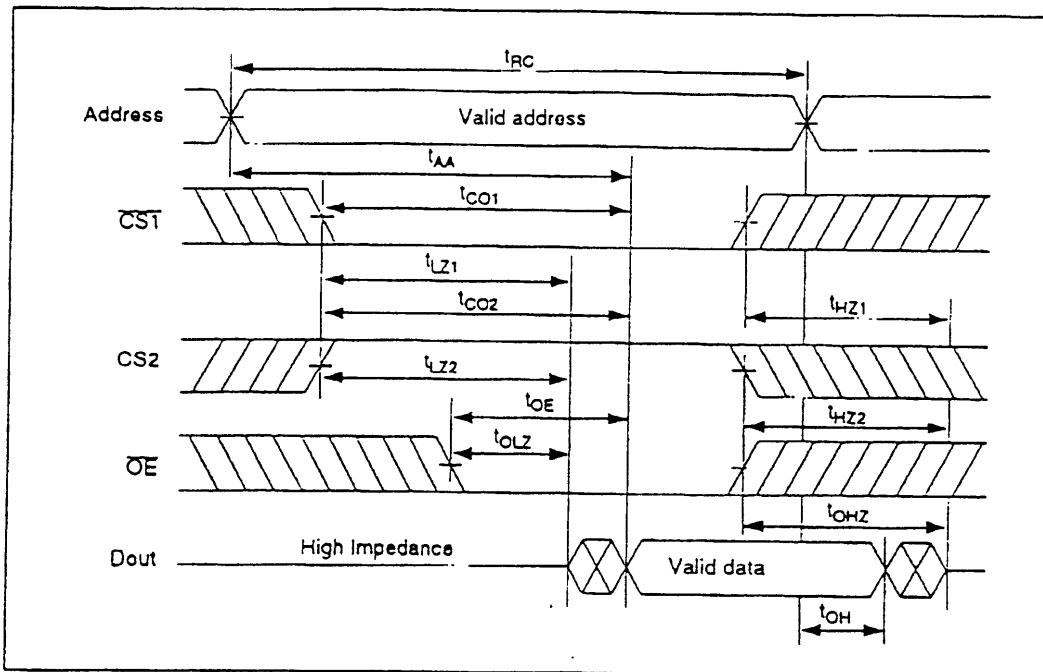
Parameter	Symbol	HM6264B-8L		HM6264B-10L		Unit	Notes
		Min	Max	Min	Max		
Read cycle time	t_{RC}	85	—	100	—	ns	
Address access time	t_{AA}	—	85	—	100	ns	
Chip select access time	$\overline{CS1}$ t_{CO1}	—	85	—	100	ns	
	$CS2$ t_{CO2}	—	85	—	100	ns	
Output enable to output valid	t_{OE}	—	45	—	50	ns	
Chip selection to output	$\overline{CS1}$ t_{LZ1}	10	—	10	—	ns	2
In low-Z	$CS2$ t_{LZ2}	10	—	10	—	ns	2
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	2
Chip deselection in to	$\overline{CS1}$ t_{HZ1}	0	30	0	35	ns	1, 2
output in high-Z	$CS2$ t_{HZ2}	0	30	0	35	ns	1, 2
Output disable to output in high-Z	t_{OHZ}	0	30	0	35	ns	1, 2
Output hold from address change	t_{OH}	10	—	10	—	ns	

Notes: 1. t_{HZ} is defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

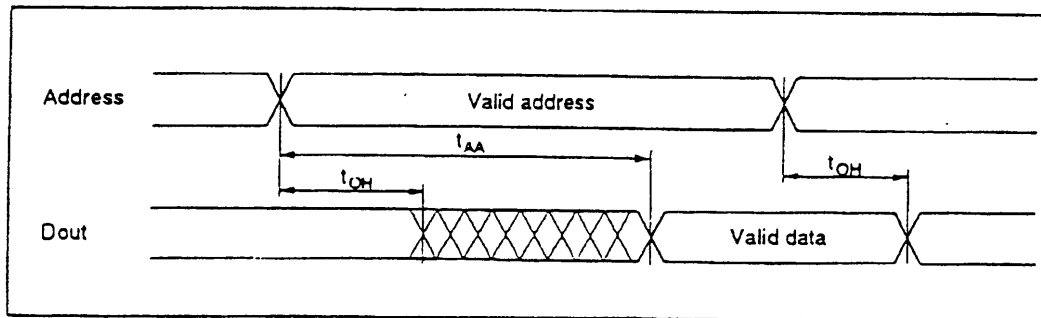
2. At any given temperature and voltage condition, t_{HZ} maximum is less than t_{LZ} minimum both for a given device and from device to device.

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Read Timing Waveform (1) ($\overline{WE} = V_{IH}$)

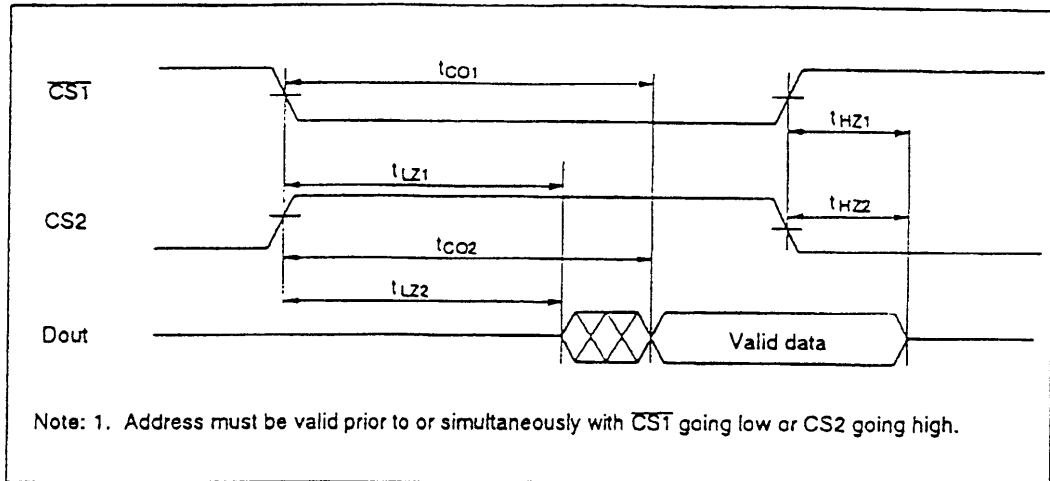


Read Timing Waveform (2) ($\overline{WE} = V_{IH}$, $\overline{OE} = V_{IL}$)



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Read Timing Waveform (3) ($\overline{WE} = V_{IH}$, $\overline{OE} = V_{IL}$)*1



HM6264B Series

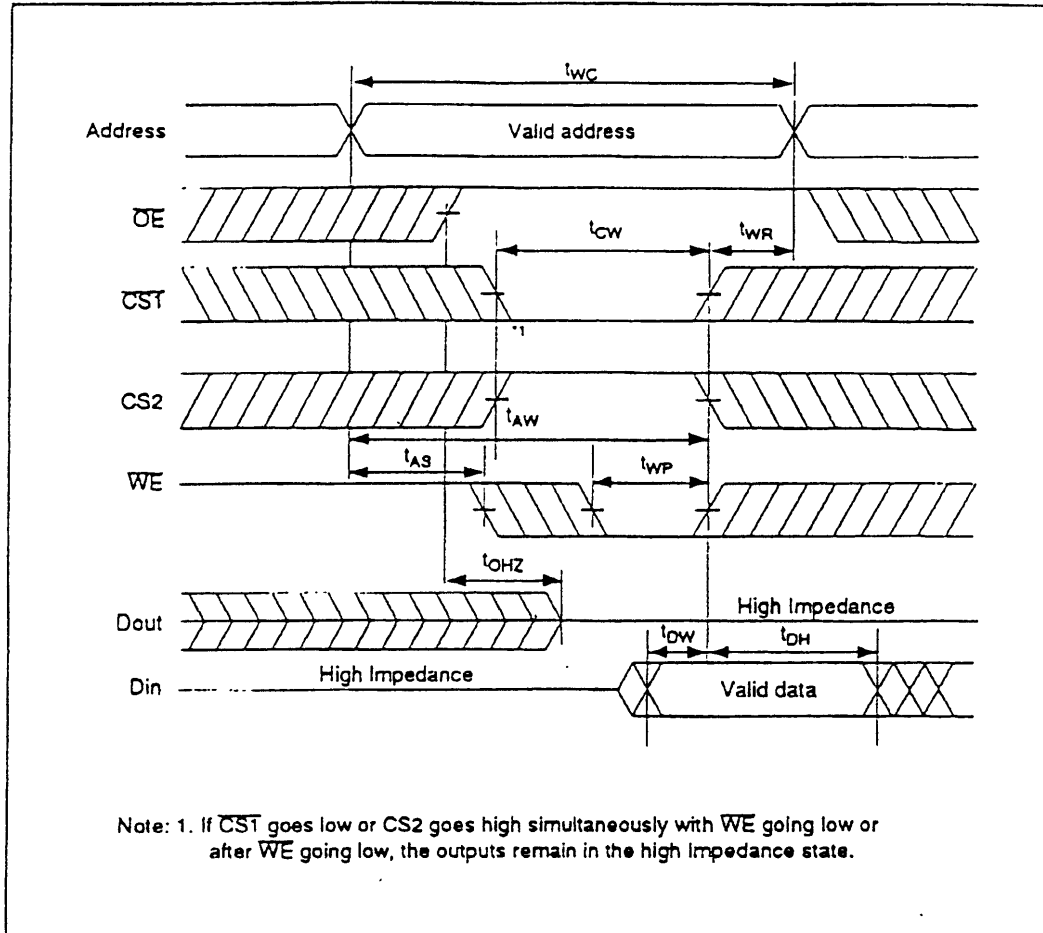
Write Cycle

Parameter	Symbol	HM6264B-8L		HM6264B-10L		Unit	Notes
		Min	Max	Min	Max		
Write cycle time	t_{wc}	85	—	100	—	ns	
Chip selection to end of write	t_{cw}	75	—	80	—	ns	2
Address setup time	t_{as}	0	—	0	—	ns	3
Address valid to end of write	t_{aw}	75	—	80	—	ns	
Write pulse width	t_{wp}	55	—	60	—	ns	1, 6
Write recovery time	t_{wr}	0	—	0	—	ns	4
WE to output in high-Z	t_{whz}	0	30	0	35	ns	5
Data to write time overlap	t_{dw}	40	—	40	—	ns	
Data hold from write time	t_{dh}	0	—	0	—	ns	
Output active from end of write	t_{ow}	5	—	5	—	ns	
Output disable to output in high-Z	t_{ohz}	0	30	0	35	ns	5

- Notes: 1. A write occurs during the overlap of a low $\overline{CS1}$, and high CS2, and a high WE. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and WE going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and WE going high. Time t_{wp} is measured from the beginning of write to the end of write.
2. t_{cw} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{as} is measured from the address valid to the beginning of write.
4. t_{wr} is measured from the earliest of $\overline{CS1}$ or WE going high or CS2 going low to the end of write cycle.
5. During this period, I/O pins are in the output state, therefore the input signals of the opposite phase to the outputs must not be applied.
6. In the write cycle with $\overline{OE}$ low fixed, t_{wp} must satisfy the following equation to avoid a problem of data bus contention
- $$t_{wp} \geq t_{whz} \max + t_{ow} \min.$$

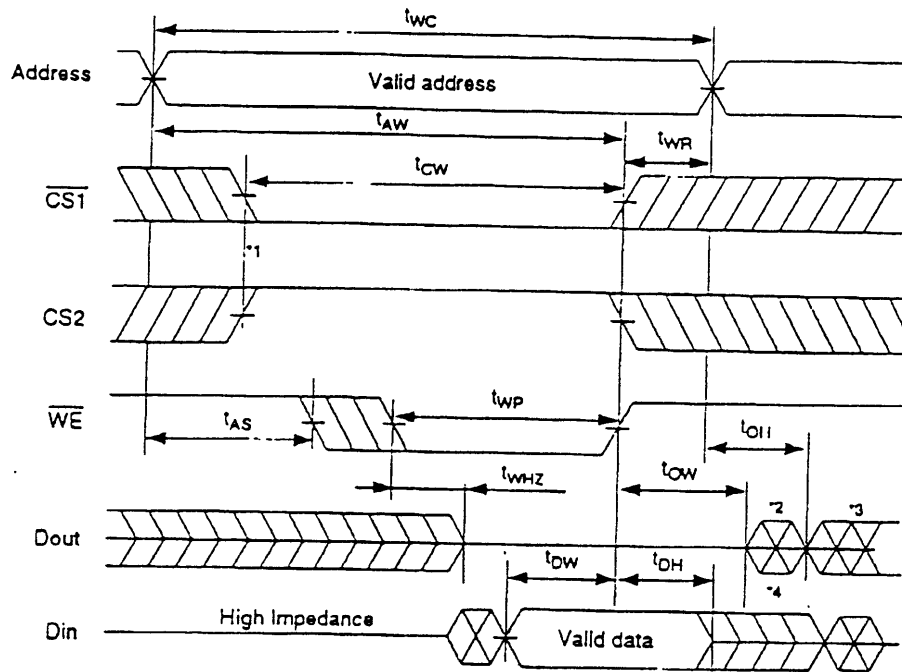
HM6264B Series

Write Timing Waveform (1) ($\overline{OE}$ Clock)



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Write Timing Waveform (2) ($\overline{OE}$ Low Fixed) ($\overline{OE} = V_{IL}$)



- Notes:
1. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ goes low, the outputs remain in high impedance state.
 2. $\overline{Dout}$ is the same phase of the written data in this write cycle.
 3. $\overline{Dout}$ is the read data of the next address.
 4. If $\overline{CS1}$ is low and $\overline{CS2}$ is high during this period, I/O pins are in the output state. Input signals of opposite phase to the outputs must not be applied to I/O pins.

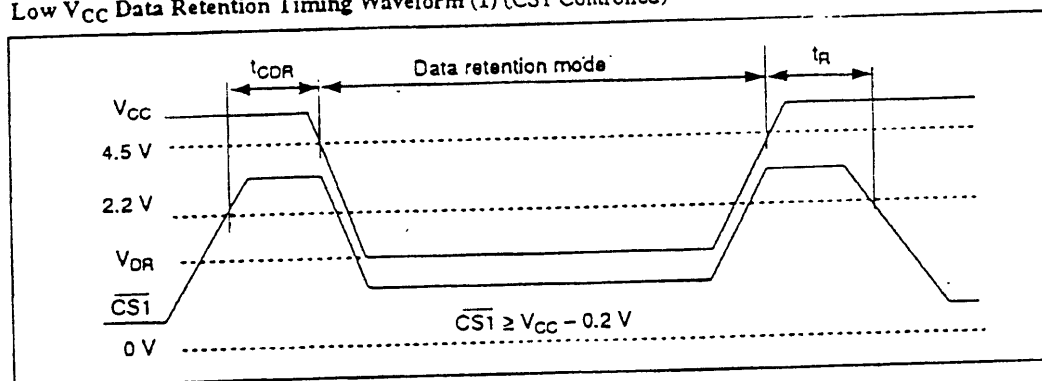
HM6264B Series

Low V_{CC} Data Retention Characteristics ($T_a = 0$ to $+70^{\circ}\text{C}$)

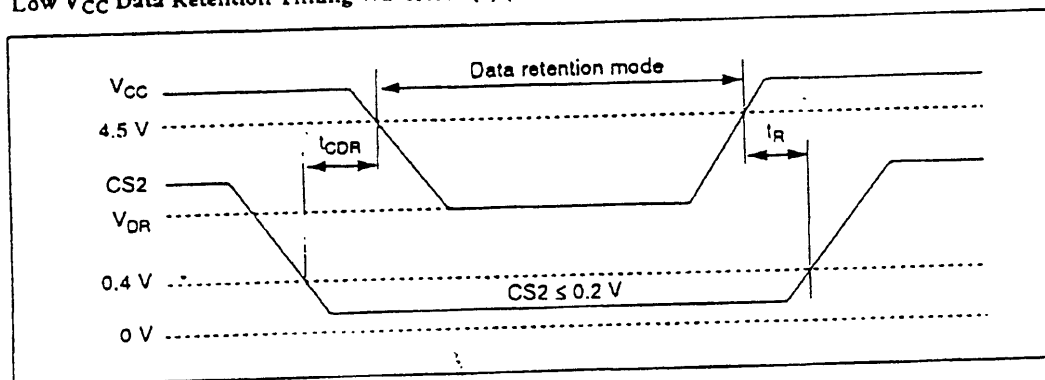
Parameter	Symbol	Min	Typ ¹	Max	Unit	Test conditions ^{2,4}
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS1} \geq V_{CC} - 0.2\text{ V}$, $CS2 \geq V_{CC} - 0.2\text{ V}$ or $CS2 \leq 0.2\text{ V}$
Data retention current	I_{CCDR}	—	1 ¹	25 ²	μA	$V_{CC} = 3.0\text{ V}$, $0\text{ V} \leq V_{in} \leq V_{CC}$ $\overline{CS1} \geq V_{CC} - 0.2\text{ V}$, $CS2 \geq V_{CC} - 0.2\text{ V}$ or $0\text{ V} \leq CS2 \leq 0.2\text{ V}$
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC} ³	—	—	ns	

- Notes: 1. Reference data at $T_a = 25^{\circ}\text{C}$.
2. $10\text{ }\mu\text{A}$ max at $T_a = 0$ to $+40^{\circ}\text{C}$.
3. t_{RC} = read cycle time.
4. $CS2$ controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, $\overline{OE}$ buffer, and Din buffer. If $CS2$ controls data retention mode, V_{in} levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, $CS2$ must be $CS2 \geq V_{CC} - 0.2\text{ V}$ or $0\text{ V} \leq CS2 \leq 0.2\text{ V}$. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



Low V_{CC} Data Retention Timing Waveform (2) ($CS2$ Controlled)

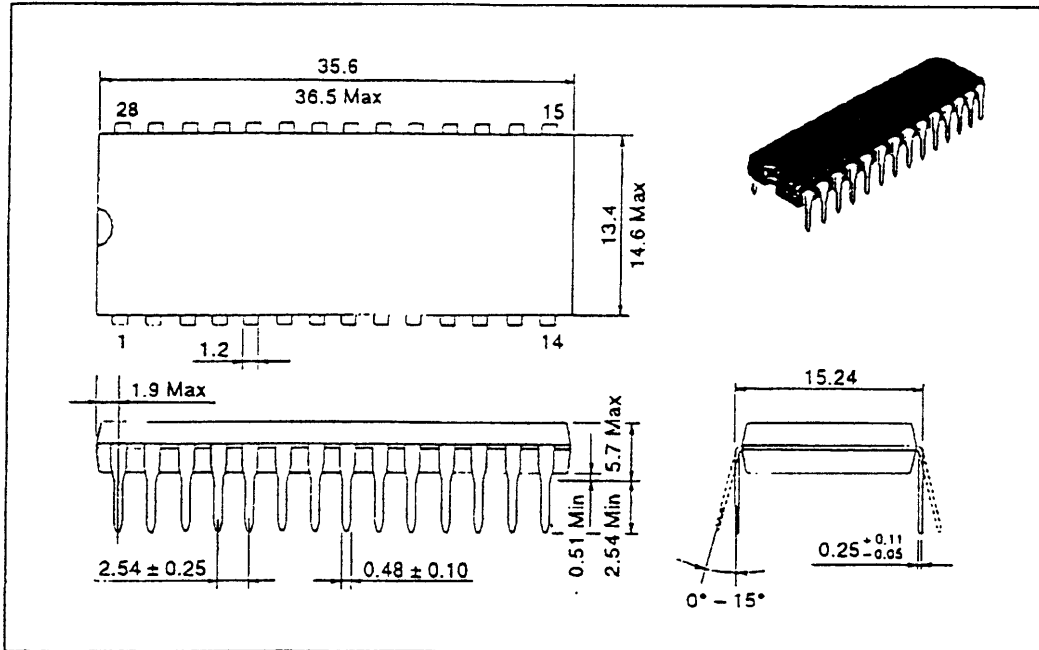


HM6264B Series

Package Dimensions

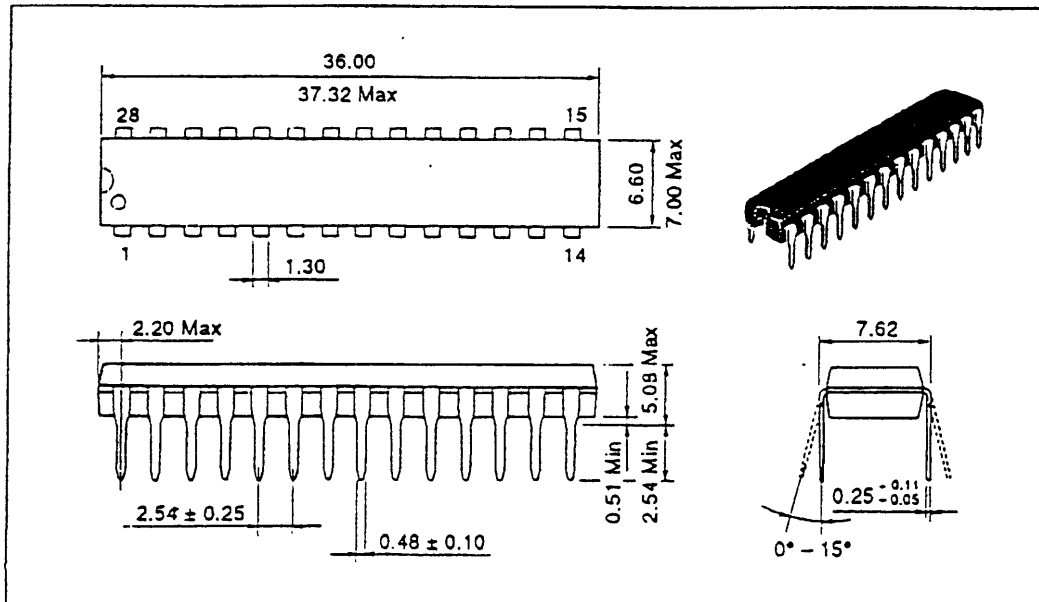
HM6264BLP Series (DP-28)

Unit: mm



HM6264BLSP Series (DP-28N)

Unit: mm



HM6264B Series

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Semiconductor & IC Div.
Nippon Bldg., 2-4-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel : Tokyo (03) 3270-2111
Fax : (03) 3270-5109

For further information write to:

Hitachi America, Ltd.
Semiconductor & IC Div.
2000 Sierra Point Parkway
Brisbane, CA 94005-1835
U. S. A.
Tel : 415-589-8300
Fax : 415-583-4207

Hitachi Europe GmbH
Electronic Components Group
Continental Europe
Domagaler Strasse 3
D-85622 Feldkirchen
München
Tel : 089-9 91 80-0
Fax : 089-9 29 30 00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel : 0628-565000
Fax : 0628-778322

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road,
Tsim Sha Tsui, Kowloon,
Hong Kong
Tel : 27359218
Fax : 27306071

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 0104
Tel : 535-2100
Fax : 535-1533

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HM6264B Series

Package Dimensions (cont)

HM6264BLFP Series (FP-28DA)

Unit: mm

