N-Channel 20-V (D-S) MOSFETs

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.4 @ V_{GS} = 4.5 V	0.73
	0.5 @ V_{GS} = 2.5 V	0.65

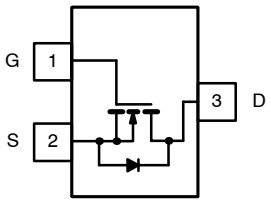
FEATURES

- TrenchFET® Power MOSFET
- ESD Protected: 4000 V

APPLICATIONS

- Direct Logic-Level Interface: TTL/CMOS
- Drivers: Relays, Solenoids, Lamps, Hammers
- Battery Operated Systems, DC/DC Converters
- Solid-State Relays
- Load/Power Switching-Cell Phones, Pagers

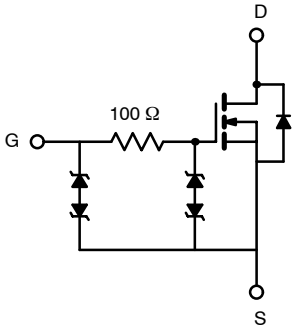
TO-236
(SOT-23)



Top View

Marking Code: *K2ywl*

K2 = Part Number Code for TN0200K
y = Year Code
w = Week Code
l = Lot Traceability



Ordering Information: TN0200K-T1—E3 (Lead Free)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limits	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Drain Current (T_J = 150°C)[b]	T_A= 25°C	I_D	0.73	A
	T_A= 70°C		0.58	
Pulsed Drain Current[a]		I_{DM}	4	
Continuous Source Current (Diode Conduction)[b]		I_S	0.3	
Power Dissipation[b]	T_A= 25°C	P_D	0.35	W
	T_A= 70°C		0.22	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limits	Unit
Maximum Junction-to-Ambient[b]	R_{thJA}	357	°C/W

Notes
a. Pulse width limited by maximum junction temperature.
b. Surface Mounted on FR4 Board, t ≤ 10 sec.

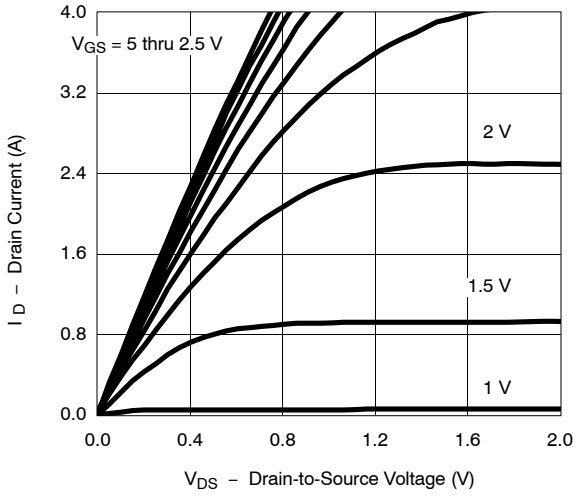
SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Conditions	Limits Min	Limits Typ	Limits Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 μA	20			V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 50 μA	0.45	0.6	1.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±4.5 V			±5	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			1	μA
		T_J = 55°C			10	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 4.5 V	2.5			A
		V_{DS} ≥ 5 V, V_{GS} = 2.5 V	1.5			A
Drain-Source On-Resistance[a]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 0.6 A		0.2	0.4	Ω
		V_{GS} = 2.5 V, I_D = 0.6 A		0.25	0.5	Ω
Forward Transconductance[a]	g_{fs}	V_{DS} = 5 V, I_D = 0.6 A		2.2		S
Diode Forward Voltage[a]	V_{SD}	I_S = 0.3 A, V_{GS} = 0 V		0.8	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 0.6 A		1400	2000	pC
Gate-Source Charge	Q_{gs}			190		pC
Gate-Drain Charge	Q_{gd}			300		pC
Gate Resistance	R_g			105		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 16 Ω I_D ≅ 0.6 A, V_{GEN} = 4.5 V, R_g = 6 Ω		17	25	ns
Rise Time	t_r			20	30	ns
Turn-Off Delay Time	$t_{d(off)}$			55	85	ns
Fall-Time	t_f			30	45	ns

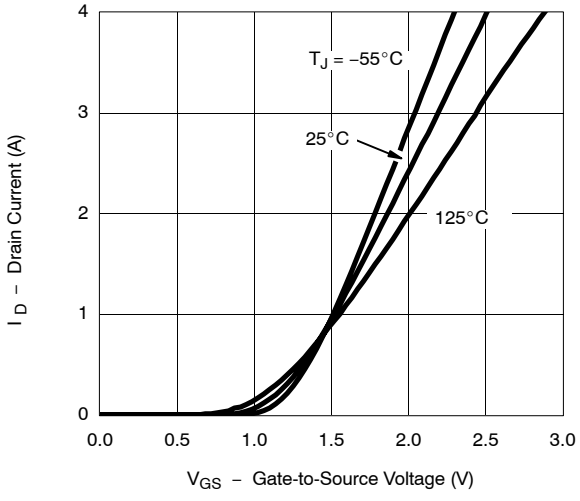
Notes
a. Pulse test: PW ≤300 μs duty cycle ≤2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Output Characteristics

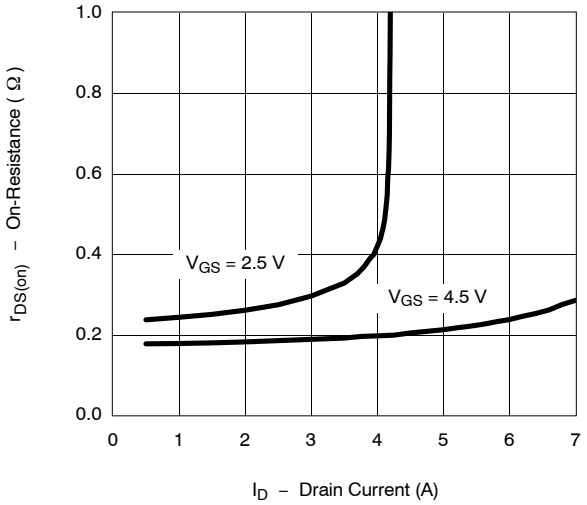


Transfer Characteristics

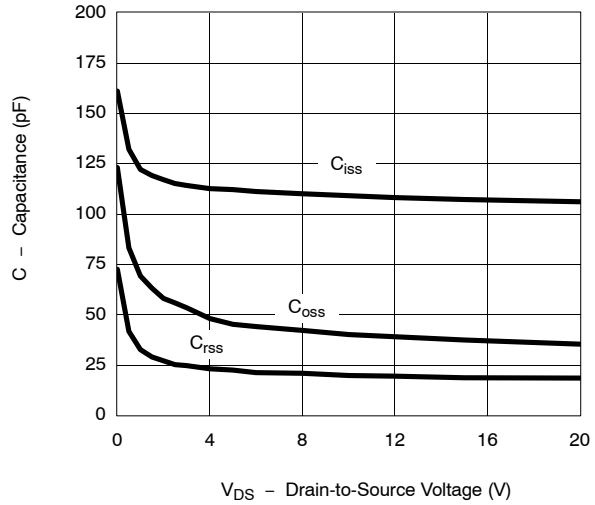


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

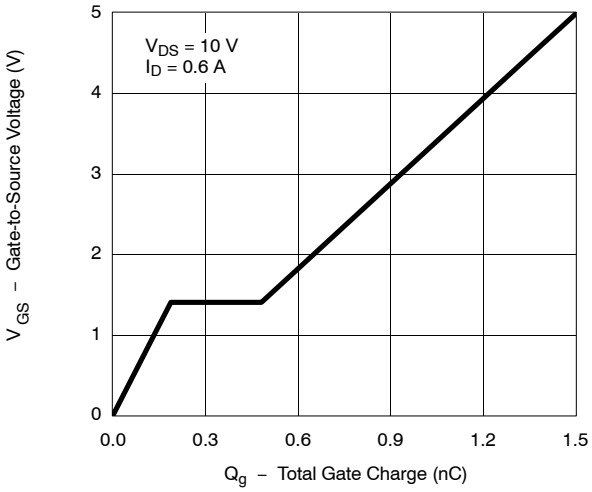
On-Resistance vs. Drain Current



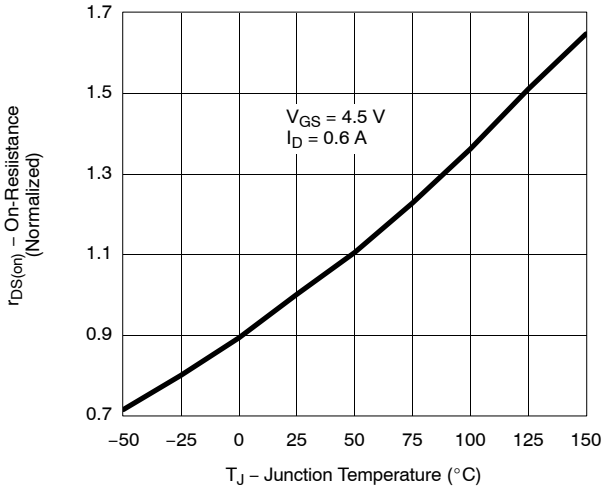
Capacitance



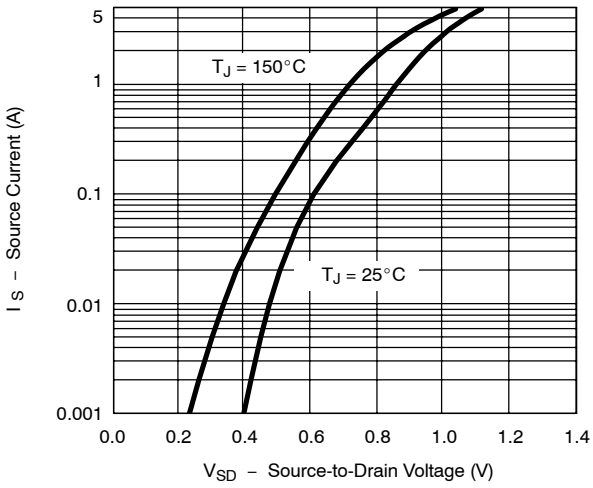
Gate Charge



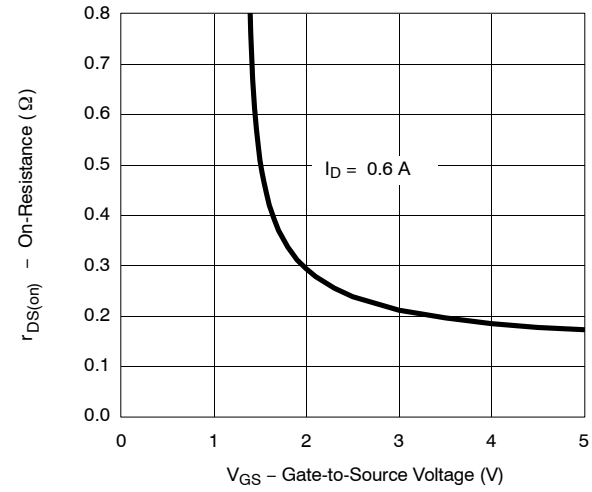
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

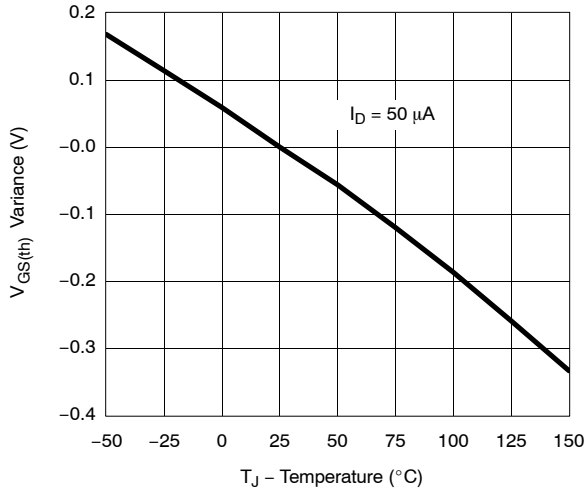


On-Resistance vs. Gate-to-Source Voltage

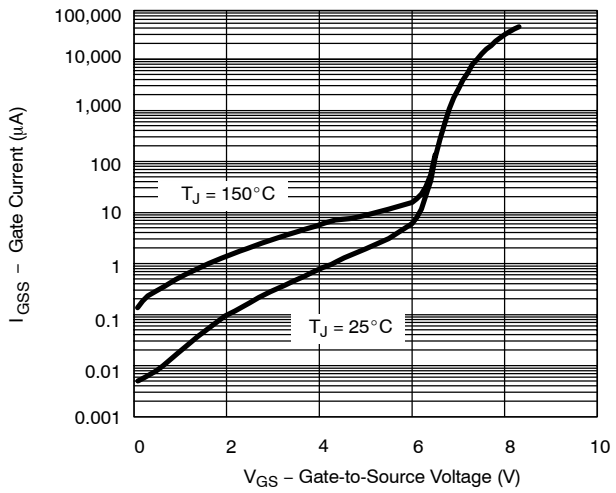


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

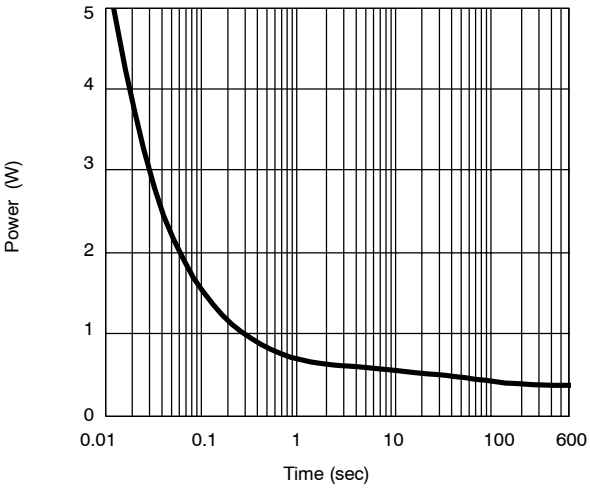
Threshold Voltage



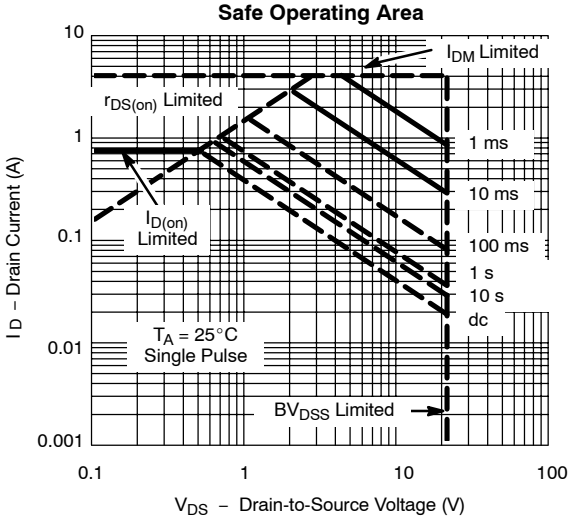
Gate Current vs. Gate-Source Voltage



Single Pulse Power, Junction-to-Ambient



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient