FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with the JEDEC 3.3 V ±0.3 V supply**
- **CMOS low power consumption**
- **Flow-through pin-out architecture**
- **Low inductance, multiple centre power and ground pins for minimum noise and ground bounce**
- **3-state outputs**
- **Direct interface with TTL levels**

DESCRIPTION

The 74HL33646 consist of 8 non-inverting bus transceiver circuits with 3-state outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the 'A' or 'B' bus will be clocked in the internal registers, as the appropiate clock (CP_{AB} or CP_{BA}) goes to a HIGH logic level. Output enable ($\overline{OE}$) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the 'A' or 'B' register, or in both.The select source inputs (S_{AB} and S_{BA}) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when $\overline{OE}$ is active (LOW). In the isolation mode ($\overline{OE}$ = HIGH), 'A' data may be stored in the 'B' register and/or 'B' data may be stored in the 'A' register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, 'A' or 'B' may be driven at a time.

The '646' is functionally identical to the '648', but has non-inverting data paths.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.0 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	C_L = 50 pF V_{CC} = 3.3 V	3.2	ns
f_{max}	maximum clock frequency		350	MHz
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	50	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PACKAGE	MATERIAL	CODE
74HL33646D	28	SO	plastic	SOT136-1
74HL33646DB	28	SSOP	plastic	SOT341-1
74HL33646PW	28	TSSOP	plastic	SOT361-1

PINNING

PIN	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	output enable input (active LOW)
2, 3, 4, 5, 10, 11, 12, 13	A_0 to A_7	'A' data inputs/outputs
6, 7, 8, 9	GND	ground (0 V)
14	DIR	direction control input
15	S_{BA}	select 'B' to 'A' source input
16	CP_{BA}	'B' to 'A' clock input (Low-to-High, edge-triggered)
26, 25, 24, 23, 20, 19, 18, 17	B_0 to B_7	'B' data inputs/outputs
21, 22	V_{CC}	positive supply voltage
27	S_{AB}	select 'A' to 'B' source input
28	CP_{AB}	'A' to 'B' clock input (Low-to-High, edge-triggered)

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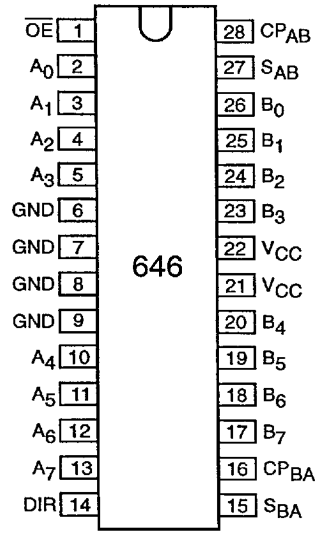
Fig.1 Pin configuration.

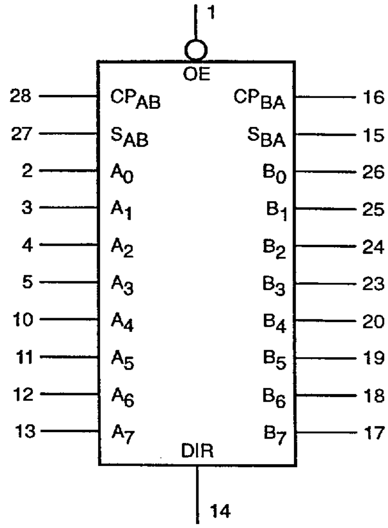
Fig.2 Logic symbol.

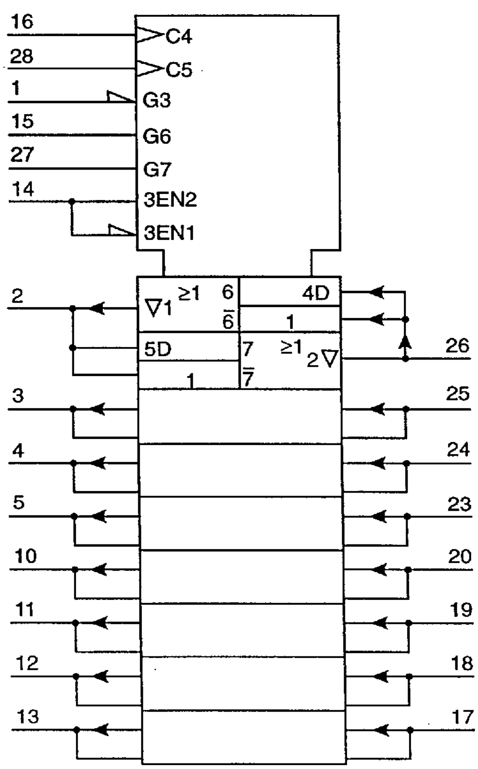
Fig3. IEC logic symbol.

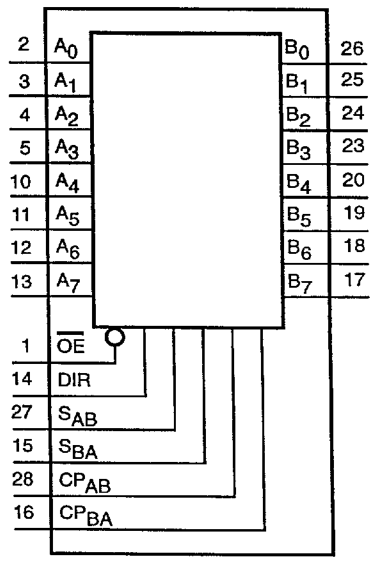
Fig.4 Functional diagram.

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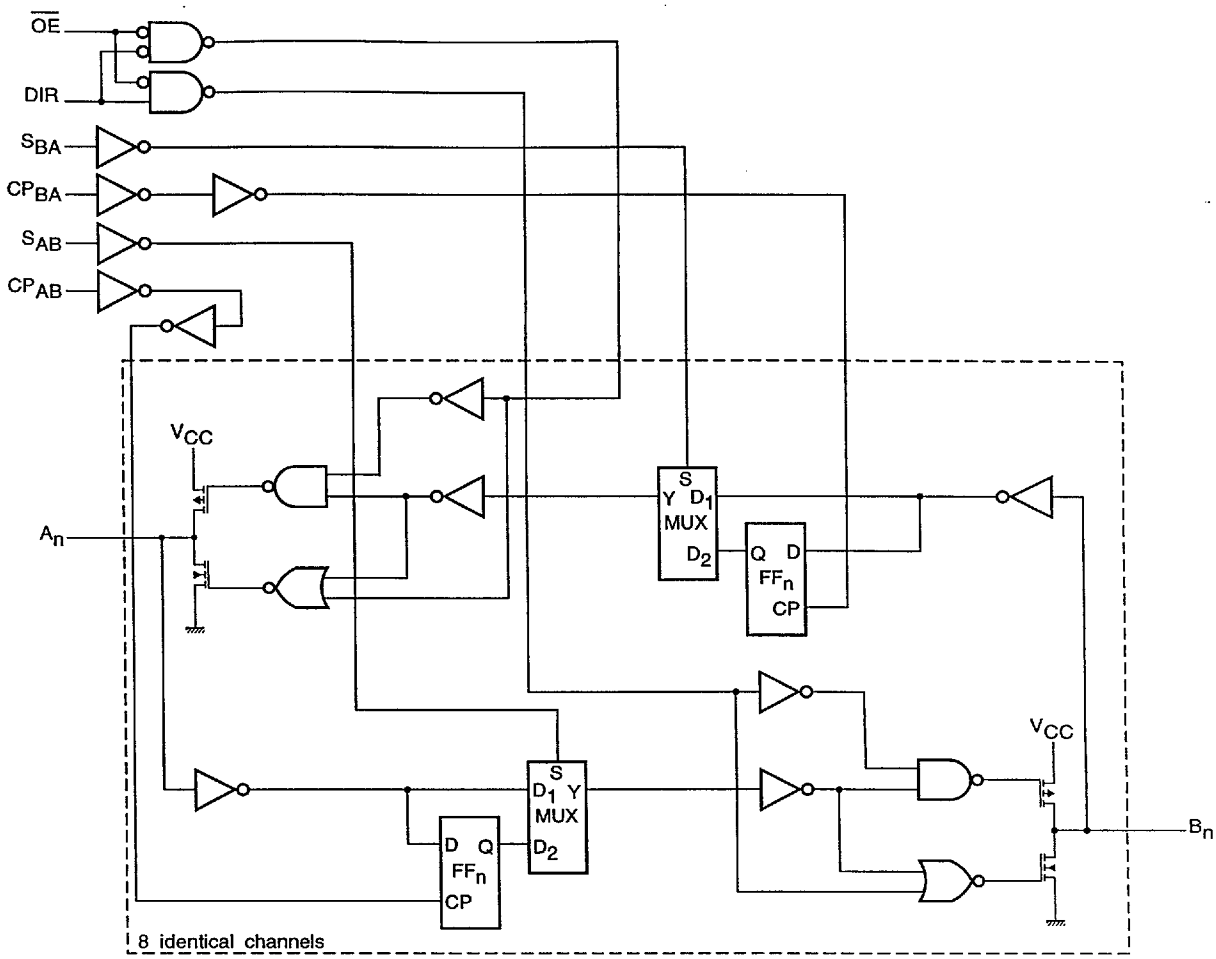

Fig.5 Logic diagram.

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FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A_0 to A_7	B_0 to B_7	
X X	X X	↑ X	X ↑	X X	X X	input un*	un* input	store A, B unspecified* store B, A unspecified*
H H	X X	↑ H or L	↑ H or L	X X	X X	input	input	store A and B data, isolation hold storage
L L	L L	X X	X H or L	X X	L H	output	input	real-time B data to A bus stored B data to A bus
L L	H H	X H or L	X X	L H	X X	input	output	real-time A data to B bus stored A data to B bus

* The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH level transition

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DC CHARACTERISTICS FOR 74HL33646

For the DC characteristics see chapter "HLL family characteristics", section "Family specifications".
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HL33646

GND = 0 V; $t_r = t_f = 2.0$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) +25 MIN.	T_{amb} (°C) +25 MAX.	T_{amb} (°C) -40 to +85 MIN.	T_{amb} (°C) -40 to +85 MAX.	UNIT	TEST CONDITIONS V_{CC} (V)	TEST CONDITIONS WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay A_n, B_n to B_n, A_n	– – –	19.2 7.2 4.8	– – –	22.0 8.3 5.5	ns	1.2 2.0 3.0	Fig.6
t_{PHL}/t_{PLH}	propagation delay CP_{AB}, CP_{BA} to B_n, A_n	– – –	23.2 8.7 5.8	– – –	26.8 10.1 6.7	ns	1.2 2.0 3.0	Fig.7
t_{PHL}/t_{PLH}	propagation delay S_{AB}, S_{BA} to B_n, A_n	– – –	24.4 9.2 6.1	– – –	28.0 10.5 7.0	ns	1.2 2.0 3.0	Fig.8
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to A_n, B_n	– – –	24.4 9.2 6.1	– – –	28.0 10.5 7.0	ns	1.2 2.0 3.0	Fig.9
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to A_n, B_n	– – –	19.5 8.1 5.8	– – –	22.3 9.1 6.5	ns	1.2 2.0 3.0	Fig.9
t_{PZH}/t_{PZL}	3-state output enable time DIR to A_n, B_n	– – –	26.0 9.8 6.5	– – –	30.0 11.3 7.5	ns	1.2 2.0 3.0	Fig.10
t_{PHZ}/t_{PLZ}	3-state output disable time DIR to A_n, B_n	– – –	20.3 8.4 6.0	– – –	23.1 9.5 6.7	ns	1.2 2.0 3.0	Fig.10
t_W	clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	3.0 2.0	– –	3.7 2.5	– –	ns	2.0 3.0	Figs 6 and 8
t_{su}	set-up time A_n, B_n to CP_{AB}, CP_{BA}	– – 1.0	– – –	– – 1.0	– – –	ns	1.2 2.0 3.0	Fig.7
t_h	hold time A_n, B_n to CP_{AB}, CP_{BA}	– – 1.0	– – –	– – 1.0	– – –	ns	1.2 2.0 3.0	Fig.7
f_{max}	maximum clock pulse frequency	150 200	– –	100 150	– –	ns	2.0 3.0	Fig.7

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AC WAVEFORMS

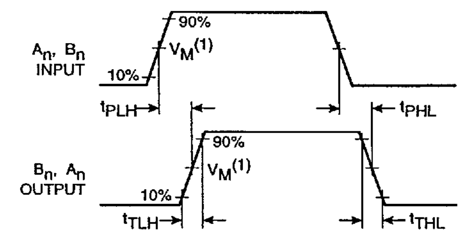

Fig.6 Waveforms showing the input A_n, B_n to output B_n, A_n propagation delays and the output transition times.

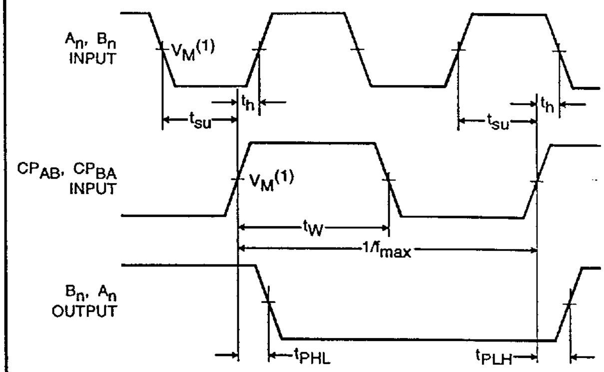

Fig.7 Waveforms showing the A_n, B_n to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB}, CP_{BA} to output B_n, A_n propagation delays.

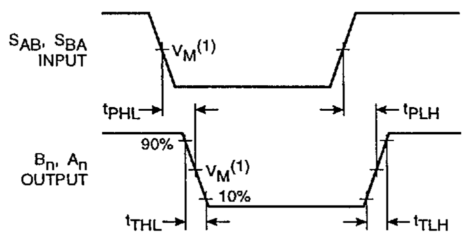

Fig.8 Waveforms showing the input S_{AB}, S_{BA} to output B_n, A_n propagation delay times and output transition times.

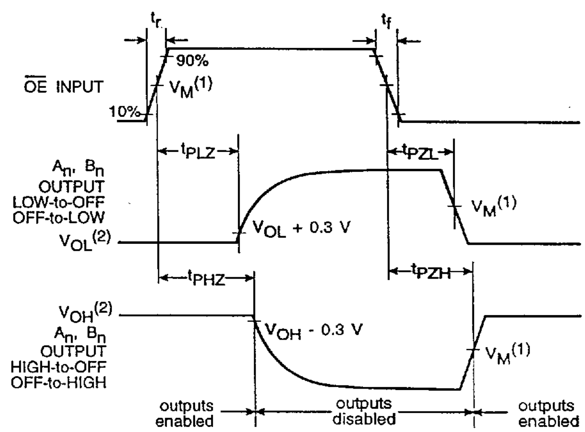

Fig.9 Waveforms showing the input $\overline{OE}$ to output A_n, B_n 3-state enable and disable times.

Notes: (1) V_M = 0.6 V at V_{CC}= 1.2 V.
V_M = 1.0 V at V_{CC}= 2.0 V.
V_M = 1.5 V at V_{CC}= 3.0 V.
(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

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AC WAVEFORMS *(Continued)*

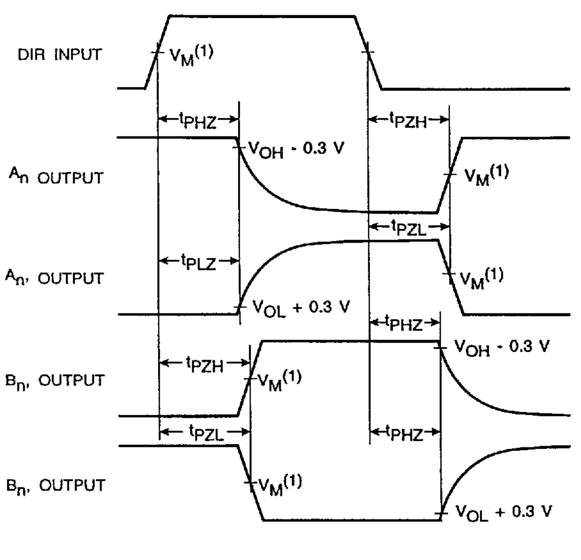

Fig.10 Waveforms showing the input DIR to output A_n, B_n 3-state enable and disable times.

Notes:
(1) $V_M = 0.6$ V at $V_{CC}= 1.2$ V.
$V_M = 1.0$ V at $V_{CC}= 2.0$ V.
$V_M = 1.5$ V at $V_{CC}= 3.0$ V.
(2) V_{OL} and V_{OH} are the typical output voltage drop that occur with the 3-state output load.

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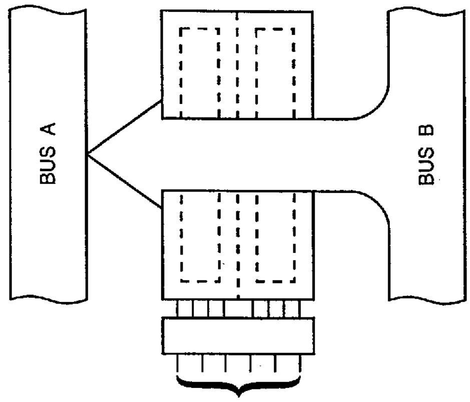
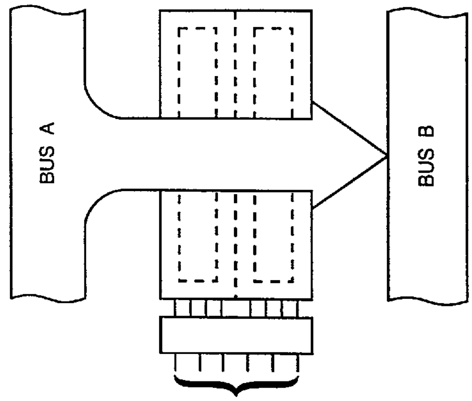
APPLICATION INFORMATION

Real-time transfer; bus B to bus A



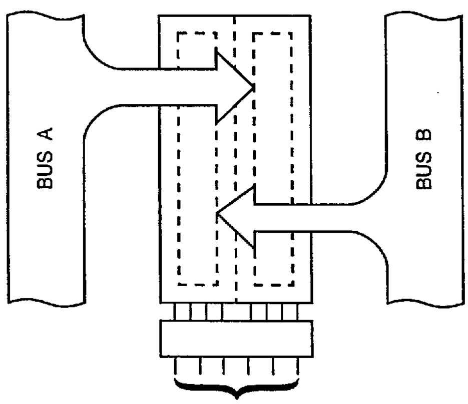
(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
L	L	X	X	X	L

Real-time transfer; bus A to bus B



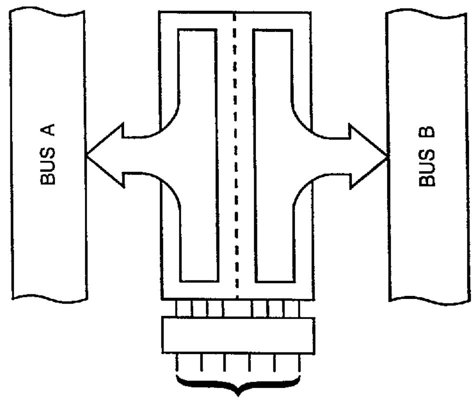
(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
L	H	X	X	L	X

Storage from A, B or A and B



(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

Transfer storage data to A or B



(1) $\overline{OE}$	(14) DIR	(28) CP_{AB}	(16) CP_{BA}	(27) S_{AB}	(15) S_{BA}
L	L	X	H or L	X	H
L	H	H or L	X	H	X

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