SC483
Dual Synchronous Buck Pseudo Fixed Frequency Power Supply Controller

POWER MANAGEMENT

Description

The SC483 is a dual output constant-on synchronous buck PWM controller intended for use in notebook computers and other battery operated portable devices. Features include high efficiency and a fast dynamic response with no minimum on time. The excellent transient response means that SC483 based solutions will require less output capacitance than competing fixed frequency converters.

The switching frequency is constant until a step in load or line voltage occurs at which time the pulse density and frequency will increase or decrease to counter the change in output or input voltage. After the transient event, the controller frequency will return to steady state operation. At light loads, Power-Save Mode enables the SC483 to skip PWM pulses for better efficiency.

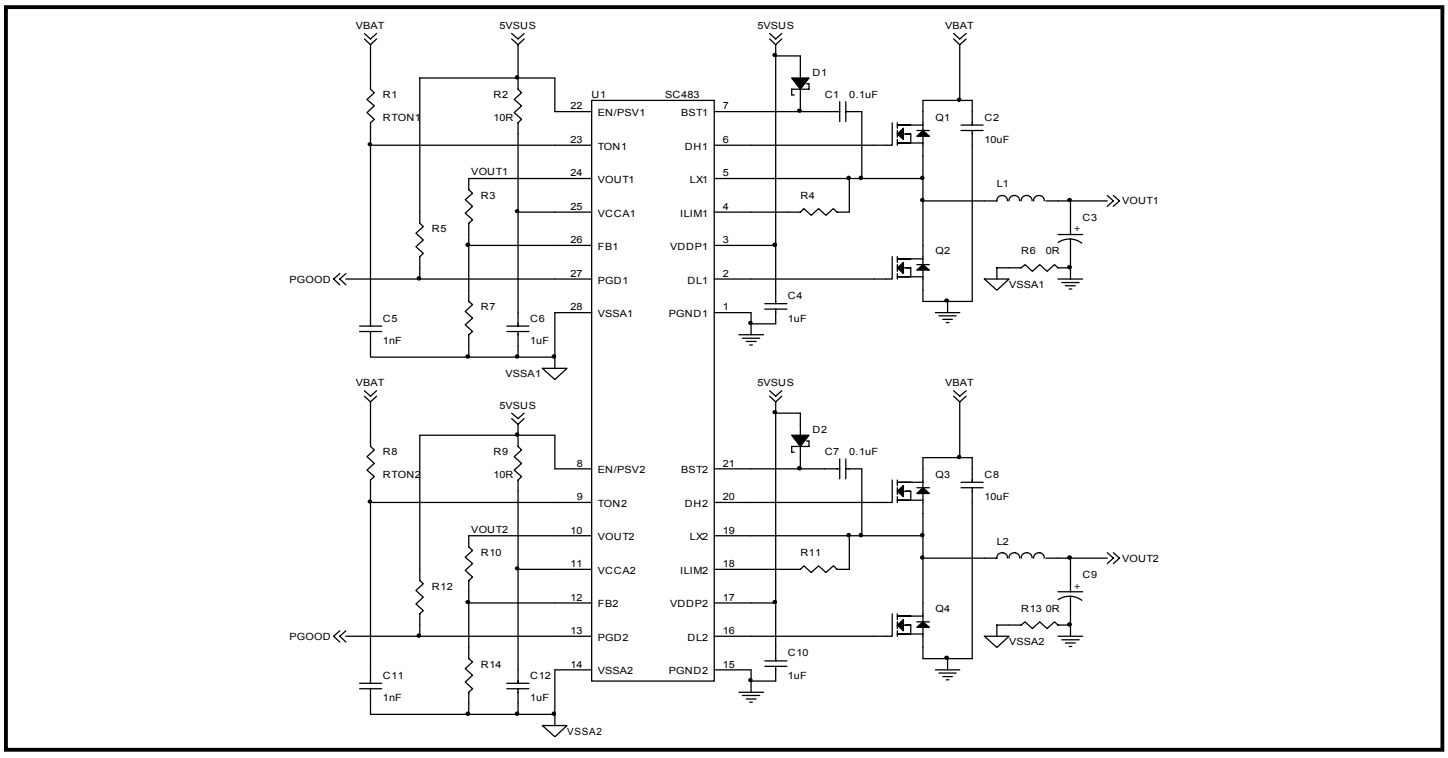
Each output voltage can be independently adjusted from 0.5V to VCCA. Two frequency setting resistors set the on-time for each buck controller. The frequency can thus be tailored to minimize crosstalk. The integrated gate drivers feature adaptive shoot-through protection and soft switching. Additional features include cycle-by-cycle current limit, digital soft-start, over-voltage and under-voltage protection, and a PGOOD output for each controller.

Features

- Constant on-time for fast dynamic response
- Programmable VOUT range = 0.5 – VCCA
- VBAT Range = 1.8V – 25V
- DC current sense using low-side RDS(ON) sensing or sense resistor
- Resistor programmable frequency
- Cycle-by-cycle current limit
- Digital soft-start
- Separate PSAVE option for each switcher
- Over-voltage/Under-voltage fault protection
- 10µA Typical shutdown current
- Low quiescent power dissipation
- Two Power Good indicators
- 1% Reference (2% system DC accuracy)
- Integrated gate drivers with soft switching
- Separate enables
- 28 Lead TSSOP
- Industrial temperature range
- Output soft discharge upon shutdown

Applications

- Notebook computers
- CPT I/O supplies
- Handheld terminals and PDAs
- LCD monitors
- Network power supplies



Absolute Maximum Ratings(1)

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Maximum	Units
TONn to VSSAn		-0.3 to +25.0	V
DHn, BSTn to PGNDn		-0.3 to +30.0	V
LXn to PGNDn		-2.0 to +25.0	V
PGNDn to VSSAn		-0.3 to +0.3	V
BSTn to LXn		-0.3 to +6.0	V
DLn, ILIMn, VDDPn to PGNDn		-0.3 to +6.0	V
EN/PSVn, FBn, PGDn, VCCAn, VOUTn to VSSAn		-0.3 to +6.0	V
VCCAn to EN/PSVn, FBn, PGDn, VOUTn		-0.3 to +6.0	V
Thermal Resistance Junction to Ambient (2)	θ_{JA}	84	°C/W
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	300	°C

Notes:
(1) This device is ESD sensitive. Use of standard ESD handling precautions is required.
(2) Measured in accordance with JESD51-1, JESD51-2 and JESD51-7.

Electrical Characteristics

Test Conditions: V_{BAT} = 15V, EN/PSV1=EN/PSV2 = 5V, VCCA1 = VDDP1 = VCCA2 = VDDP2 = 5V, V_{OUT1} = V_{OUT2} =1.25V, R_{TON1} = R_{TON2} = 1MΩ

Parameter	Conditions	25°C			-40°C to 125°C		Units
		Min	Typ	Max	Min	Max	
Input Supplies							
VCCA1, VCCA2			5.0		4.5	5.5	V
VDDP1, VDDP2			5.0		4.5	5.5	V
VBAT Voltage	Offtime > 800ns	1.8		25			V
VDDP1, VDDP2 Operating Current	FB > regulation point, I_{LOAD} = 0A		70			150	µA
VCCA1, VCCA2 Operating Current	FB > regulation point, I_{LOAD} = 0A		700			1100	µA
TON1, TON2 Operating Current	R_{TON} = 1M		15				µA
Shutdown Current	EN/PSV1, EN/PSV2 = 0V		-5			-10	µA
	VCCA1, VCCA2		5			10	µA
	VDDP1, TON1, VDDP2, TON2		0			1	µA

Electrical Characteristics (Cont.)

Test Conditions: V_{BAT} = 15V, EN/PSV1=EN/PSV2 = 5V, VCCA1 = VDDP1 = VCCA2 = VDDP2 = 5V, V_{OUT1} = V_{OUT2} =1.25V, R_{TON1} = R_{TON2} = 1MΩ

Parameter	Conditions	25°C			-40°C to 125°C		Units
		Min	Typ	Max	Min	Max	
Controller							
Error Comparator Threshold (FB turn-on threshold)(1)	VCCA = 4.5V to 5.5V		0.500		-1%	+1%	V
Output Voltage Range					0.5	VCCA	V
On-Time, V_{BAT} = 2.5V	R_{TON} = 1MΩ		1761		1497	2025	ns
	R_{TON} = 500kΩ		936		796	1076	
Minimum Off Time			400			550	ns
VOUT1, VOUT2 Input Resistance			500				kΩ
VOUT1, VOUT2 Shutdown Discharge Resistance	EN/PSV1, EN/PSV2 = GND		22				Ω
FB1, FB2 Input Bias Current					-1.0	+1.0	µA
Over-Current Sensing							
ILIM Source Current	DL high		10		9	11	µA
Current Comparator Offset	PGND - ILIM				-10	10	mV
PSAVE							
Zero-Crossing Threshold	(PGND - LX), EN/PSV = 5V		5				mV
Fault Protection							
Current Limit (Positive) (2)	(PGND - LX), R_{ILIM} = 5kΩ		50		35	65	mV
	(PGND - LX), R_{ILIM} = 10kΩ		100		80	120	mV
	(PGND - LX), R_{ILIM} = 20kΩ		200		170	230	mV
Current Limit (Negative)	(PGND - LX)		-125		-160	-90	mV
Output Under-Voltage Fault	With respect to internal ref.		-30		-40	-25	%
Output Over-Voltage Fault - OUT1	With respect to internal ref.		+16		+12	+20	%
Output Over-Voltage Fault - OUT2	With respect to internal ref.		+16		+12	+20	%
Over-Voltage Fault Delay	FB forced above OV Threshold		5				µs
PGD Low Output Voltage	Sink 1mA					0.4	V
PGD Leakage Current	FB in regulation, PGD = 5V					1	µA
PGD UV Threshold	With respect to internal ref.		-10		-12	-8	%

Electrical Characteristics (Cont.)

Test Conditions: V_{BAT} = 15V, EN/PSV1=EN/PSV2 = 5V, VCCA1 = VDDP1 = VCCA2 = VDDP2 = 5V, V_{OUT1} = V_{OUT2} =1.25V, R_{TON1} = R_{TON2} = 1MΩ

Parameter	Conditions	25°C			-40°C to 125°C		Units
		Min	Typ	Max	Min	Max	
Fault Protection (Cont.)							
PGD Fault Delay	FB forced outside PGD window		5				µs
VCCA Undervoltage Threshold	Falling (100mV Hysteresis)		4.0		3.7	4.3	V
Over Temperature Lockout	10°C Hysteresis		165				°C
Inputs/Outputs							
Logic Input Low Voltage	EN/PSV low					1.2	V
Logic Input High Voltage	EN High, PSV low (Floating)		2.0				V
Logic Input High Voltage	EN/PSV high				3.1		V
EN/PSV Input Resistance	R Pullup to VCCA		1.5				MΩ
	R Pulldown to VSSA		1.0				
Soft Start							
Soft-Start Ramp Time	EN/PSV high to PGD high		440				clks(3)
Under-Voltage Blank Time	EN/PSV high to UV high		440				clks(3)
Gate Drivers							
Shoot-Through Delay (4)	DH or DL rising		30				ns
DL Pull-Down Resistance	DL low		0.8			1.6	Ω
DL Sink Current	DL = 2.5V		3.1				A
DL Pull-Up Resistance	DL high		2			4	Ω
DL Source Current	DL = 2.5V		1.3				A
DH Pull-Down Resistance	DH low, BST - LX = 5V		2			4	Ω
DH Pull-Up Resistance(5)	DH high, BST - LX = 5V		2			4	Ω
DH Sink/Source Current	DH = 2.5V		1.3				A

Notes:

(1) When the inductor is in continuous and discontinuous conduction mode, the output voltage will have a DC regulation level higher than the error-comparator threshold by 50% of the ripple voltage.

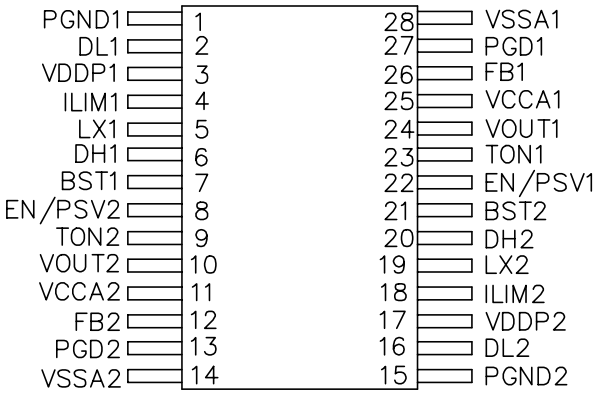
(2) Using a current sense resistor, this measurement relates to PGND minus the voltage of the source on the low-side MOSFET. These values guaranteed by the ILIM Source Current and Current Comparator Offset tests.

(3) clks = Switching cycles.

(4) Guaranteed by design. See Shoot-Through Delay Timing Diagram on Page 6.

(5) Semtech's SmartDriver™ FET drive first pulls DH high with a pullup resistance of 10Ω (typ.) until LX = 1.5V (typ.). At this point, an additional pullup device is activated, reducing the resistance to 2Ω (typ.). This negates the need for an external gate or boost resistor.

Pin Configuration



TSSOP-28

Ordering Information

Device	Package[1]
SC483ITSTRT[2]	TSSOP-28

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free product. This product is fully WEEE, RoHS and J-STD-020B compliant.

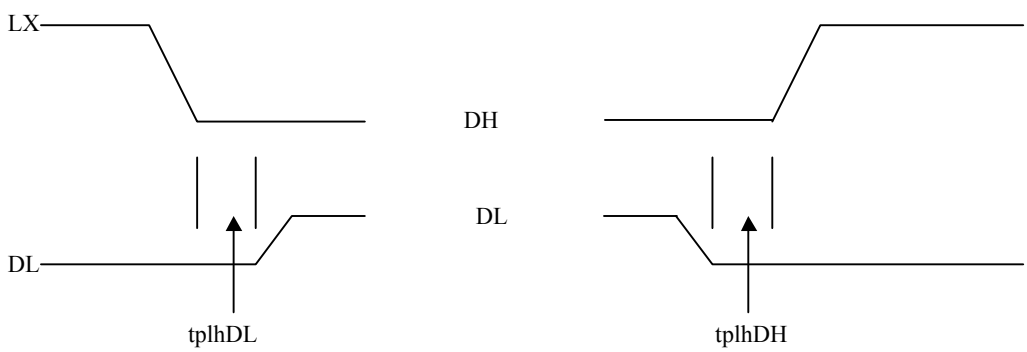
Pin Descriptions

Pin #	Pin Name	Pin Function
1	PGND1	Power ground.
2	DL1	Gate drive output for the low side MOSFET switch.
3	VDDP1	+5V supply voltage input for the gate drivers. Decouple this pin with a 1uF ceramic capacitor to PGND1.
4	ILIM1	Current limit input. Connect to drain of low-side MOSFET for RDS(on) sensing or the source for resistor sensing through a threshold sensing resistor.
5	LX1	Phase node (junction of top and bottom MOSFETs and the output inductor) connection.
6	DH1	Gate drive output for the high side MOSFET switch.
7	BST1	Boost capacitor connection for the high side gate drive.
8	EN/PSV2	Enable/Power Save input. Pull down to VSSA2 to shut down OUT2 and discharge it through 22Ω (nom). Pull up to enable OUT2 and activate PSAVE mode. Float to enable OUT2 and activate continuous conduction mode (CCM), which should be used for dynamic voltage transitioning. If floated, bypass to VSSA2 with a 10nF ceramic capacitor.
9	TON2	This pin is used to sense VBAT through a pullup resistor, RTON2, and to set the top MOSFET on-time. Bypass this pin with a 1nF ceramic capacitor to VSSA2.
10	VOUT2	Output voltage sense input for output 2. Connect to the output at the load.
11	VCCA2	Supply voltage input for the analog supply. Use a 10 Ohm / 1uF RC filter from 5VSUS to VSSA2.
12	FB2	Feedback input. Connect to a resistor divider located at the IC from VOUT2 to VSSA2 to set the output voltage from 0.5V to VCCA2.
13	PGD2	Power Good open drain NMOS output. Goes high after a fixed clock cycle delay (440 cycles) following power up.
14	VSSA2	Ground reference for analog circuitry. Connect to PGND2 at the bottom of the output capacitor.

Pin Descriptions (Cont.)

Pin#	Pin Name	Pin Function
15	PGND2	Power ground.
16	DL2	Gate drive output for the low side MOSFET switch.
17	VDDP2	+5V supply voltage input for the gate drivers. Decouple this pin with a 1uF ceramic capacitor to PGND2.
18	ILIM2	Current limit input. Connect to drain of low-side MOSFET for RDS(on) sensing or the source for resistor sensing through a threshold sensing resistor.
19	LX2	Phase node (junction of top and bottom MOSFETs and the output inductor) connection.
20	DH2	Gate drive output for the high side MOSFET switch.
21	BST2	Boost capacitor connection for the high side gate drive.
22	EN/PSV1	Enable/Power Save input. Pull down to VSSA1 to shut down OUT1 and discharge it through 22Ω (nom.). Pull up to enable OUT1 and activate PSAVE mode. Float to enable OUT1 and activate continuous conduction mode (CCM). If floated, bypass to VSSA1 with a 10nF ceramic capacitor.
23	TON1	This pin is used to sense VBAT through a pullup resistor, RTON1, and to set the top MOSFET on-time. Bypass this pin with a 1nF ceramic capacitor to VSSA1.
24	VOUT1	Output voltage sense input for output 1. Connect to the output at the load.
25	VCCA1	Supply voltage input for the analog supply. Use a 10 Ohm / 1uF RC filter from 5VSUS to VSSA1.
26	FB1	Feedback input. Connect to a resistor divider located at the IC from VOUT1 to VSSA1 to set the output voltage from 0.5V to VCCA1.
27	PGD1	Power Good open drain NMOS output. Goes high after a fixed clock cycle delay (440 cycles) following power up.
28	VSSA1	Ground reference for analog circuitry. Connect to PGND1 at the bottom of the output capacitor.

Shoot-Through Delay Timing Diagram



Block Diagram

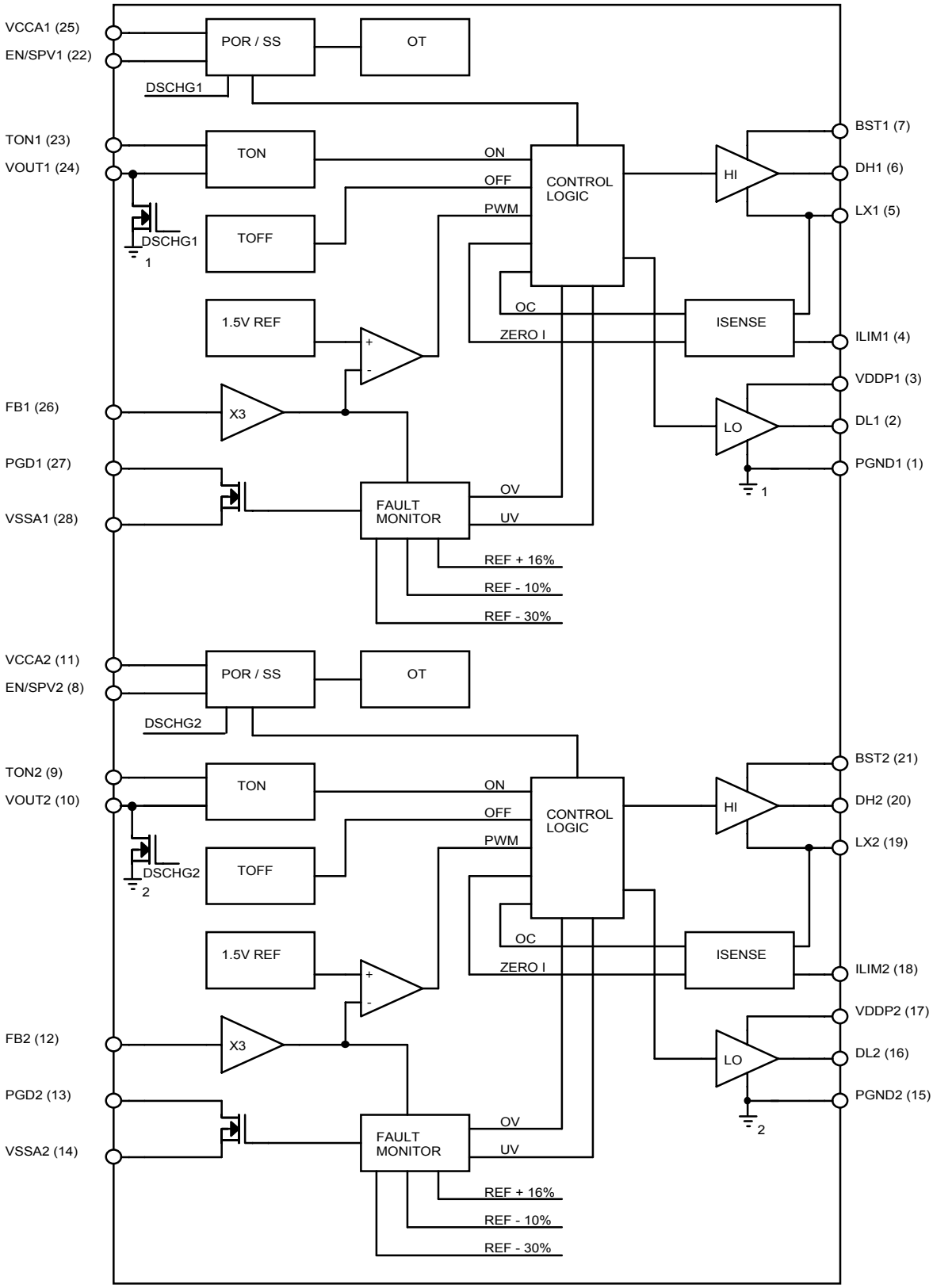


FIGURE 1.

+5V Bias Supplies

The SC483 requires an external +5V bias supply in addition to the battery. If stand-alone capability is required, the +5V supply can be generated with an external linear regulator such as the Semtech LP2951. To avoid interference between outputs, each controller has its own ground reference, VSSA, which should be tied by a single trace to PGND at the negative terminal of that controller's output capacitor (see Layout Guidelines). All external components referenced to VSSA in the schematic should be connected to the appropriate VSSA trace. The supply decoupling capacitor for controller 1 should be tied between VCCA1 and VSSA1. Likewise, the supply decoupling capacitor for controller 2 should be tied between VCCA2 and VSSA2. A 10Ω resistor should be used to decouple each VCCA supply from the main VDDP supplies. PGND can then be a separate plane which is not used for routing traces. All PGND connections are connected directly to the ground plane with special attention given to avoiding indirect connections which may create ground loops. As mentioned above, VSSA1 and VSSA2 must be connected to the PGND plane at the negative terminal of their respective output capacitors only. The VDDP1 and VDDP2 inputs provide power to the upper and lower gate drivers. A decoupling capacitor for each supply is required. No series resistor between VDDP and 5V is required. See layout guidelines for more details.

Pseudo-fixed Frequency Constant On-Time PWM Controller

The PWM control architecture consists of a constant on-time, pseudo fixed frequency PWM controller (see Figure 1, SC483 Block Diagram). The output ripple voltage developed across the output filter capacitor's ESR provides the PWM ramp signal eliminating the need for a current sense resistor. The high-side switch on-time is determined by a one-shot whose period is directly proportional to output voltage and inversely proportional to input voltage. A second one-shot sets the minimum off-time which is typically 400ns.

On-Time One-Shot (t_{ON})

The on-time one-shot comparator has two inputs. One input looks at the output voltage, while the other input samples the input voltage and converts it to a current. This input voltage-proportional current is used to charge an internal on-time capacitor. The on-time is the time required for the voltage on this capacitor to charge from zero volts to VOUT, thereby making the on-time of the high-side switch directly proportional to output voltage and inversely proportional to input voltage. This implementation results in a nearly constant switching frequency without the need for a clock generator.
For VOUT < 3.3V:

$$t_{ON} = 3.3x10^{-12} \bullet (R_{TON} + 37x10^{3}) \bullet \left(\frac{V_{OUT}}{V_{BAT}} \right) + 50ns$$

For 3.3V ≤ VOUT ≤ 5V:

$$t_{ON} = 0.85 \bullet 3.3x10^{-12} \bullet (R_{TON} + 37x10^{3}) \bullet \left(\frac{V_{OUT}}{V_{BAT}} \right) + 50ns$$

R_{TON} is a resistor connected from the input supply (VBAT) to the TON pin. Due to the high impedance of this resistor, the TON pin should always be bypassed to VSSA using a 1nF ceramic capacitor.

EN/PSV: Enable, Psave and Soft Discharge

The EN/PSV pin enables the supply. When EN/PSV is tied to VCCA the controller is enabled and power save will also be enabled. When the EN/PSV pin is tri-stated, an internal pull-up will activate the controller and power save will be disabled. If PSAVE is enabled, the SC483 PSAVE comparator will look for the inductor current to cross zero on eight consecutive switching cycles by comparing the phase node (LX) to PGND. Once observed, the controller will enter power save and turn off the low side MOSFET when the current crosses zero. To improve light-load efficiency and add hysteresis, the on-time is increased by 50% in power save. The efficiency improvement at light-loads more than offsets the disadvantage of slightly higher output ripple. If the inductor current does not cross zero on any switching cycle, the controller will immediately exit power save. Since the controller counts zero crossings, the converter can sink current as long as the current does not cross zero on eight consecutive cycles. This allows the output voltage to recover quickly in response to negative load steps even when psave is enabled.

If the EN/PSV pin is pulled low, the related output will be shut down and discharged using a switch with a nominal resistance of 22 Ohms. This will ensure that the output is in a defined state next time it is enabled and also

ensure, since this is a soft discharge, that there are no dangerous negative voltage excursions to be concerned about. In order for the soft discharge circuitry to function correctly, the chip supply must be present.

Output Voltage Selection

The output voltage (OUT2 shown) is set by the feedback resistors R9 & R13 of Figure 2 below. The internal reference is 1.5V, so the voltage at the feedback pin is multiplied by three to match the 1.5V reference. Therefore the output can be set to a minimum of 0.5V. The equation for setting the output voltage is:

$$V_{OUT} = \left(1 + \frac{R9}{R13}\right) \bullet 0.5$$

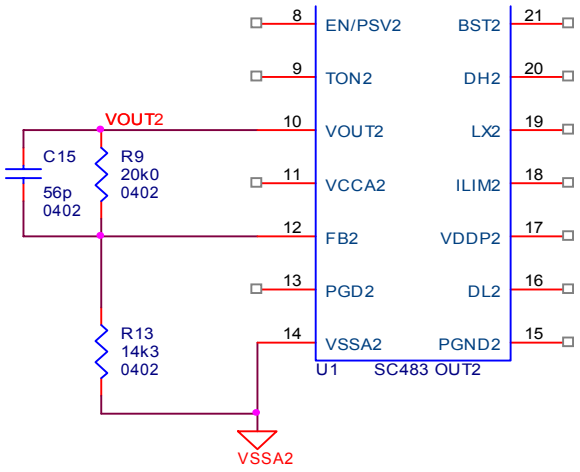


Figure 2: Setting The Output Voltage

Current Limit Circuit

Current limiting of the SC483 can be accomplished in two ways. The on-state resistance of the low-side MOSFET can be used as the current sensing element or sense resistors in series with the low-side source can be used if greater accuracy is desired. $R_{DS(ON)}$ sensing is more efficient and less expensive. In both cases, the R_{ILIM} resistor between the ILIM pin and LX pin set the over current threshold. This resistor R_{ILIM} is connected to a 10µA current source within the SC483 which is turned on when the low side MOSFET turns on. When the voltage drop across the sense resistor or low side MOSFET equals the voltage across the RILIM resistor, positive current limit will activate. The high side MOSFET will not be turned on until the voltage drop across the sense element (resistor or MOSFET) falls below the voltage across the R_{ILIM} resistor. In an extreme over-current situation, the top MOSFET will never turn back on and eventually the part will latch off due to output undervoltage (see Output Undervoltage Protection).

The current sensing circuit actually regulates the inductor valley current (see Figure 3). This means that if the current limit is set to 10A, the peak current through the inductor would be 10A plus the peak-to-peak ripple current, and the average current through the inductor would be 10A plus 1/2 the peak-to-peak ripple current. The equations for setting the valley current and calculating the average current through the inductor are shown below:

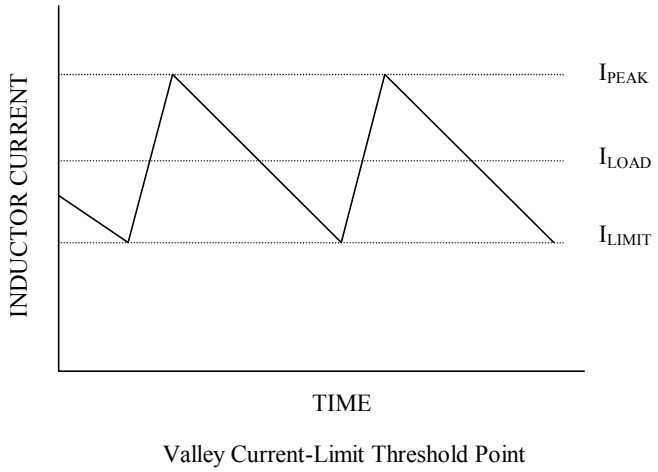


Figure 3: Valley Current Limiting

The equation for the current limit threshold is as follows:

$$I_{LIMIT} = 10e^{-6} \bullet \frac{R_{ILIM}}{R_{SENSE}} A$$

Where (referring to Figure 8 on Page 16) R_{ILIM} is R10 and R_{SENSE} is the $R_{DS(ON)}$ of Q4.

For resistor sensing, a sense resistor is placed between the source of Q4 and PGND. The current through the source sense resistor develops a voltage that opposes the voltage developed across R_{ILIM}. When the voltage developed across the R_{SENSE} resistor reaches the voltage drop across R_{ILIM}, a positive over-current exists and the high side MOSFET will not be allowed to turn on. When using an external sense resistor R_{SENSE} is the resistance of the sense resistor.

The current limit circuitry also protects against negative over-current (i.e. when the current is flowing from the load to PGND through the inductor and bottom MOSFET). In this case, when the bottom MOSFET is turned on, the phase node, LX, will be higher than PGND initially. The SC483 monitors the voltage at LX, and if it is greater than a set threshold voltage of 125mV (nom.) the bottom MOSFET is turned off. The device then waits for approximately 2.5µs and then DL goes high for 300ns (typ.) once more to sense the current. This repeats until either the over-current condition goes away or the part latches off due to output overvoltage (see Output Overvoltage Protection).

Power Good Output

The power good output is an open-drain output and requires a pull-up resistor. When the output voltage is 16% above or 10% below its set voltage, PGD gets pulled low. It is held low until the output voltage returns to within these tolerances once more. PGD is also held low during start-up and will not be allowed to transition high until soft start is over (440 switching cycles) and the output reaches 90% of its set voltage. There is a 5µs delay built into the PGD circuitry to prevent false transitions.

Output Overvoltage Protection

When the output exceeds 16% of its set voltage the low-side MOSFET is latched on. It stays latched on and the controller is latched off until reset (see below). There is a 5µs delay built into the OV protection circuit to prevent false transitions.

Output Undervoltage Protection

When the output is 30% below its set voltage the output is latched in a tri-stated condition. It stays latched and the controller is latched off until reset (see below). There is a 5µs delay built into the UV protection circuit to prevent false transitions. Note: to reset from any fault, VCCA or EN/PSV must be toggled.

POR, UVLO and Softstart

An internal power-on reset (POR) occurs when VCCA exceeds 3V, starting up the internal biasing. VCCA undervoltage lockout (UVLO) circuitry inhibits the controller until VCCA rises above 4.2V. At this time the UVLO circuitry resets the fault latch and soft start timer, and allows switching to occur if the device is enabled. Switching always starts with DL to charge up the BST capacitor. With the softstart circuit (automatically) enabled, it will progressively limit the output current (by limiting the current out of the ILIM pin) over a predetermined time period of 440 switching cycles.

The ramp occurs in four steps:
1) 110 cycles at 25% ILIM with double minimum off-time (for purposes of the on-time one-shot, there is an internal positive offset of 120mV to VOUT during this period to aid in startup)
2) 110 cycles at 50% ILIM with normal minimum off-time
3) 110 cycles at 75% ILIM with normal minimum off-time
4) 110 cycles at 100% ILIM with normal minimum off-time.
At this point the output undervoltage and power good circuitry is enabled. There is 100mV of hysteresis built into the UVLO circuit and when VCCA falls to 4.1V (nom.) the output drivers are shut down and tristated.

MOSFET Gate Drivers

The DH and DL drivers are optimized for driving moderate-sized high-side, and larger low-side power MOSFETs. An adaptive dead-time circuit monitors the DL output and prevents the high-side MOSFET from turning on until DL is fully off (below ~1V). Semtech's SmartDriver™ FET drive first pulls DH high with a pull-up resistance of 10Ω (typ.) until LX = 1.5V (typ.). At this point, an additional pull-up device is activated, reducing the resistance to 2Ω (typ.). This negates the need for an external gate or boost resistor. The adaptive dead-time circuit also monitors the phase node, LX, to determine the state of the high side MOSFET, and prevents the low-side MOSFET from turning on until DH is fully off (LX below ~1V). Be sure to have low resistance and low inductance between the DH and DL outputs to the gate of each MOSFET.

Dropout Performance

The output voltage adjust range for continuous-conduction operation is limited by the fixed 550ns (maximum) minimum off-time one-shot. For best dropout performance, use the slowest on-time setting of 200kHz. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on and off times. The IC duty-factor limitation is given by:

$$DUTY = \frac{t_{ON(MIN)}}{t_{ON(MIN)} + t_{OFF(MAX)}}$$

Be sure to include inductor resistance and MOSFET on-state voltage drops when performing worst-case dropout duty-factor calculations.

SC483 System DC Accuracy

Two IC parameters affect system DC accuracy, the error comparator threshold voltage variation and the switching frequency variation with line and load. The error comparator threshold does not drift significantly with supply and temperature. Thus, the error comparator contributes 1% or less to DC system inaccuracy.

Board components and layout also influence DC accuracy. The use of 1% feedback resistors contribute 1%. If tighter DC accuracy is required use 0.1% feedback resistors.

The on pulse in the SC483 is calculated to give a pseudo fixed frequency. Nevertheless, some frequency variation with line and load can be expected. This variation changes the output ripple voltage. Because constant-on regulators regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error. For example, if the feedback resistors are chosen to divide down the output by a factor of five, the valley of the output ripple will be VOUT. For example: if VOUT is 2.5V and the ripple is 50mV with VBAT = 6V, then the measured DC output will be 2.525V. If the ripple increases to 80mV with VBAT = 25V, then the measured DC output will be 2.540V.

The output inductor value may change with current. This will change the output ripple and thus the DC output voltage. It will not change the frequency.

Switching frequency variation with load can be minimized by choosing MOSFETs with lower $R_{DS(ON)}$. High $R_{DS(ON)}$ MOSFETs will cause the switching frequency to increase as the load current increases. This will reduce the ripple and thus the DC output voltage.

Design Procedure

Prior to designing an output and making component selections, it is necessary to determine the input voltage range and the output voltage specifications. For purposes of demonstrating the procedure the output for the schematic in Figure 8 on Page 16 will be designed.

The maximum input voltage ($V_{BAT(MAX)}$) is determined by the highest AC adaptor voltage. The minimum input voltage ($V_{BAT(MIN)}$) is determined by the lowest battery voltage after accounting for voltage drops due to connectors, fuses and battery selector switches. For the purposes of this design example we will use a V_{BAT} range of 8V to 20V and design OUT2. The design for OUT1 employs the same technique.

Four parameters are needed for the output:
1) nominal output voltage, V_{OUT} (we will use 1.2V)
2) static (or DC) tolerance, TOL_{ST} (we will use +/-4%)
3) transient tolerance, TOL_{TR} and size of transient (we will use +/-8% and 6A for purposes of this demonstration).
4) maximum output current, I_{OUT} (we will design for 6A)

Switching frequency determines the trade-off between size and efficiency. Increased frequency increases the switching losses in the MOSFETs, since losses are a function of VIN^2. Knowing the maximum input voltage and budget for MOSFET switches usually dictates where the design ends up. It is recommended that the two outputs are designed to operate at frequencies approximately 25% apart to avoid any possible interaction. It is also recommended that the higher frequency output is the lower output voltage output, since this will tend to have lower output ripple and tighter specifications. The default R_{tON} values of 1MΩ and 715kΩ are suggested as a starting point, but these are not set in stone. The first thing to do is to calculate the on-time, t_{ON}, at $V_{BAT(MIN)}$ and $V_{BAT(MAX)}$, since this depends only upon V_{BAT}, V_{OUT} and R_{tON}.

For V_{OUT} < 3.3V:

$$t_{ON\_VBAT(MIN)} = \left[3.3 \bullet 10^{-12} \bullet \left(R_{tON} + 37 \bullet 10^{3}\right) \bullet \frac{V_{OUT}}{V_{BAT(MIN)}}\right] + 50 \bullet 10^{-9} s$$

and

$$t_{ON\_VBAT(MAX)} = \left[3.3 \bullet 10^{-12} \bullet \left(R_{tON} + 37 \bullet 10^{3}\right) \bullet \frac{V_{OUT}}{V_{BAT(MAX)}}\right] + 50 \bullet 10^{-9} s$$

From these values of t_{ON} we can calculate the nominal switching frequency as follows:

$$f_{SW\_VBAT(MIN)} = \frac{V_{OUT}}{\left(V_{BAT(MIN)} \bullet t_{ON\_VBAT(MIN)}\right)} Hz$$

and

$$f_{SW\_VBAT(MAX)} = \frac{V_{OUT}}{(V_{BAT(MAX)} \bullet t_{ON\_VBAT(MAX)})} Hz$$

t_{ON} is generated by a one-shot comparator that samples V_{BAT} via R_{tON}, converting this to a current. This current is used to charge an internal 3.3pF capacitor to V_{OUT}. The equations above reflect this along with any internal components or delays that influence t_{ON}. For our example we select R_{tON} = 1MΩ:

$t_{ON\_VBAT(MIN)}$ = 563ns and $t_{ON\_VBAT(MAX)}$ = 255ns

$f_{SW\_VBAT(MIN)}$ = 266kHz and $f_{SW\_VBAT(MAX)}$ = 235kHz

Now that we know t_{ON} we can calculate suitable values for the inductor. To do this we select an acceptable inductor ripple current. The calculations below assume 50% of I_{OUT} which will give us a starting place.

$$L_{VBAT(MIN)} = (V_{BAT(MIN)} - V_{OUT}) \bullet \frac{t_{ON\_VBAT(MIN)}}{(0.5 \bullet I_{OUT})} H$$

and

$$L_{VBAT(MAX)} = (V_{BAT(MAX)} - V_{OUT}) \bullet \frac{t_{ON\_VBAT(MAX)}}{(0.5 \bullet I_{OUT})} H$$

For our example:

$L_{VBAT(MIN)}$ = 1.3µH and $L_{VBAT(MAX)}$ = 1.6µH

We will select an inductor value of 2.2µH to reduce the ripple current, which can be calculated as follows:

$$I_{RIPPLE\_VBAT(MIN)} = (V_{BAT(MIN)} - V_{OUT}) \bullet \frac{t_{ON\_VBAT(MIN)}}{L} A_{P-P}$$

and

$$I_{RIPPLE\_VBAT(MAX)} = (V_{BAT(MAX)} - V_{OUT}) \bullet \frac{t_{ON\_VBAT(MAX)}}{L} A_{P-P}$$

For our example:

$I_{RIPPLE\_VBAT(MIN)}$ = 1.74A_{P-P} and $I_{RIPPLE\_VBAT(MAX)}$ = 2.18A_{P-P}

From this we can calculate the minimum inductor current rating for normal operation:

$$I_{INDUCTOR(MIN)} = I_{OUT(MAX)} + \frac{I_{RIPPLE\_VBAT(MAX)}}{2} A_{(MIN)}$$

For our example:

$I_{INDUCTOR(MIN)}$ = 7.1$A_{(MIN)}$

Next we will calculate the maximum output capacitor equivalent series resistance (ESR). This is determined by calculating the remaining static and transient tolerance allowances. Then the maximum ESR is the smaller of the calculated static ESR ($R_{ESR\_ST(MAX)}$) and transient ESR ($R_{ESR\_TR(MAX)}$):

$$R_{ESR\_ST(MAX)} = \frac{(ERR_{ST} - ERR_{DC}) \bullet 2}{I_{RIPPLE\_VBAT(MAX)}} Ohms$$

Where ERR_{ST} is the static output tolerance and ERR_{DC} is the DC error. The DC error will be 1% plus the tolerance of the feedback resistors, thus 2% total for 1% feedback resistors.

For our example:

ERR_{ST} = 48mV and ERR_{DC} = 24mV, therefore

$R_{ESR\_ST(MAX)}$ = 22mΩ

$$R_{ESR\_TR(MAX)} = \frac{(ERR_{TR} - ERR_{DC})}{\left(I_{OUT} + \frac{I_{RIPPLE\_VBAT(MAX)}}{2}\right)} Ohms$$

Where ERR_{TR} is the transient output tolerance. Note that this calculation assumes that the worst case load transient is full load. For half of full load, divide the I_{OUT} term by 2.

For our example:

ERR_{TR} = 96mV and ERR_{DC} = 24mV, therefore

$R_{ESR\_TR(MAX)}$ = 10.2mΩ for a full 6A load transient

We will select a value of 12.5mΩ maximum for our design, which would be achieved by using two 25mΩ output capacitors in parallel. Note that for constant-on converters there is a minimum ESR requirement for stability which can be calculated as follows:

$$R_{ESR(MIN)} = \frac{3}{2 \bullet \pi \bullet C_{OUT} \bullet f_{SW}}$$

This criteria should be checked once the output capacitance has been determined.

Now that we know the output ESR we can calculate the output ripple voltage:

$$V_{RIPPLE\_VBAT(MAX)} = R_{ESR} \bullet I_{RIPPLE\_VBAT(MAX)} V_{P-P}$$

and

$$V_{RIPPLE\_VBAT(MIN)} = R_{ESR} \bullet I_{RIPPLE\_VBAT(MIN)} V_{P-P}$$

For our example:

$V_{RIPPLE\_VBAT(MAX)}$ = 27mV$_{P-P}$ and $V_{RIPPLE\_VBAT(MIN)}$ = 22mV$_{P-P}$

Note that in order for the device to regulate in a controlled manner, the ripple content at the feedback pin, V_{FB}, should be approximately 15mV$_{P-P}$ at minimum V_{BAT}, and worst case no smaller than 10mV$_{P-P}$. If $V_{RIPPLE\_VBAT(MIN)}$ is less than 15mV$_{P-P}$ the above component values should be revisited in order to improve this. Quite often a small capacitor, C_{TOP}, is required in parallel with the top feedback resistor, R_{TOP}, in order to ensure that V_{FB} is large enough. C_{TOP} should not be greater than 100pF. The value of C_{TOP} can be calculated as follows, where R_{BOT} is the bottom feedback resistor. Firstly calculating the value of Z_{TOP} required:

$$Z_{TOP} = \frac{R_{BOT}}{0.015} \bullet \left(V_{RIPPLE\_VBAT(MIN)} - 0.015\right) \text{Ohms}$$

Secondly calculating the value of C_{TOP} required to achieve this:

$$C_{TOP} = \frac{\left(\frac{1}{Z_{TOP}} - \frac{1}{R_{TOP}}\right)}{2 \bullet \pi \bullet f_{SW\_VBAT(MIN)}} F$$

For our example we will use R_{TOP} = 20.0kΩ and R_{BOT} = 14.3kΩ, therefore:

Z_{TOP} = 6.67kΩ and C_{TOP} = 60pF

We will select a value of C_{TOP} = 56pF. Calculating the value of V_{FB} based upon the selected C_{TOP}:

$$V_{FB\_VBAT(MIN)} = V_{RIPPLE\_VBAT(MIN)} \bullet \left(\frac{R_{BOT}}{R_{BOT} + \frac{1}{\frac{1}{R_{TOp}} + 2 \bullet \pi \bullet f_{SW\_VBAT(MIN)} \bullet C_{TOP}}} \right) V_{P-P}$$

For our example:

$V_{FB\_VBAT(MIN)}$ = 14.8mV$_{P-P}$ - good

Next we need to calculate the minimum output capacitance required to ensure that the output voltage does not exceed the transient maximum limit, $POSLIM_{TR}$, starting from the actual static maximum, $V_{OUT\_ST\_POS}$, when a load release occurs:

$$V_{OUT\_ST\_POS} = V_{OUT} + ERR_{DC} \ V$$

For our example:

$V_{OUT\_ST\_POS}$ = 1.224V

$$POSLIM_{TR} = V_{OUT} \bullet TOL_{TR} \ V$$

Where TOL_{TR} is the transient tolerance. For our example:

$POSLIM_{TR}$ = 1.296V

The minimum output capacitance is calculated as follows:

$$C_{OUT(MIN)} = L \bullet \frac{\left(I_{OUT} + \frac{I_{RIPPLE\_VBAT(MAX)}}{2}\right)^2}{\left(POSLIM_{TR}^{\ 2} - V_{OUT\_ST\_POS}^{\ 2}\right)} F$$

This calculation assumes the absolute worst case condition of a full-load to no load step transient occurring when the inductor current is at its highest. The capacitance required for smaller transient steps my be calculated by substituting the desired current for the I_{OUT} term.

For our example:

$C_{OUT(MIN)}$ = 610µF.

We will select 440µF, using two 220µF, 25mΩ capacitors in parallel. For smaller load release overshoot, 660µF may be used.

Next we calculate the RMS input ripple current, which is largest at the minimum battery voltage:

$$I_{IN(RMS)} = \sqrt{V_{OUT} \bullet (V_{BAT(MIN)} - V_{OUT})} \bullet \frac{I_{OUT}}{V_{BAT\_MIN}} A_{RMS}$$

For our example:

$I_{IN(RMS)}$ = 2.14A_{RMS}

Input capacitors should be selected with sufficient ripple current rating for this RMS current, for example a 10µF, 1210 size, 25V ceramic capacitor can handle approximately 3A_{RMS}. Refer to manufacturer's data sheets and derate appropriately.

Finally, we calculate the current limit resistor value. As described in the current limit section, the current limit looks at the "valley current", which is the average output current minus half the ripple current. We use the maximum room temperature specification for MOSFET $R_{DS(ON)}$ at V_{GS} = 4.5V for purposes of this calculation:

$$I_{VALLEY} = I_{OUT} - \frac{I_{RIPPLE\_VBAT(MIN)}}{2} A$$

The ripple at low battery voltage is used because we want to make sure that current limit does not occur under normal operating conditions.

$$R_{ILIM} = (I_{VALLEY} \bullet 1.2) \bullet \frac{R_{DS(ON)} \bullet 1.4}{10 \bullet 10^{-6}} Ohms$$

For our example:

I_{VALLEY} = 5.13A, $R_{DS(ON)}$ = 9mΩ and R_{ILIM} = 7.76kΩ

We select the next lowest 1% resistor value: 7.68kΩ

Thermal Considerations

The junction temperature of the device may be calculated as follows:

$$T_J = T_A + P_D \bullet \theta_{JA} \quad °C$$

Where:
T_A = ambient temperature (°C)
P_D = power dissipation in (W)
θ_{JA} = thermal impedance junction to ambient from absolute maximum ratings (°C/W)

The power dissipation may be calculated as follows:

$$P_D = 2 \bullet (VCCA \bullet I_{VCCA} + VDDP \bullet I_{VDDP}) + V_g \bullet Q_{g1} \bullet f_1 + VBST \bullet 1mA \bullet D_1 + V_g \bullet Q_{g2} \bullet f_2 + VBST \bullet 1mA \bullet D_2 \quad W$$

Where:
VCCA = chip supply voltage (V)
I_{VCCA} = operating current (A)
VDDP = gate drive supply voltage (V)
I_{VDDP} = gate drive operating current (A)
V_g = gate drive voltage, typically 5V (V)
Q_{gx} = FET gate charge, from the FET datasheet (C)
f_x = switching frequency (kHz)
VBST = boost pin voltage during t_{ON} (V)
D_x = duty cycle

Inserting the following values for $VBAT_{(MIN)}$ condition (since this is the worst case condition for power dissipation in the controller) as an example (OUT1 = 1.5V, OUT2 = 1.2V):

T_A = 85°C
θ_{JA} = 84°C/W
VCCA = VDDP = 5V
I_{VCCA} = 1100µA (data sheet maximum)
I_{VDDP} = 150µA (data sheet maximum)
V_g = 5V
Q_{gx} = 60nC
f_1 = 250kHz
f_2 = 300kHz
$VBAT_{(MIN)}$ = 8V
$VBST_{(MIN)}$ = $VBAT_{(MIN)}$+VDDP = 13V
$D_{1(MIN)}$ = 1.5/8 = 0.1875
$D_{2(MIN)}$ = 1.2/8 = 0.15

gives us:

$$P_D = 2 \bullet \left(5 \bullet 1100 \bullet 10^{-6} + 5 \bullet 150 \bullet 10^{-6}\right)$$
$$+ 5 \bullet 60 \bullet 10^{-9} \bullet 250 \bullet 10^{3} + 13 \bullet 1 \bullet 10^{-3} \bullet 0.1875$$
$$+ 5 \bullet 60 \bullet 10^{-9} \bullet 300 \bullet 10^{3} + 13 \bullet 1 \bullet 10^{-3} \bullet 0.15$$
$$= 0.182 \quad W$$

and:

$$T_J = 85 + 0.182 \bullet 84 = 100 \quad °C$$

As can be seen, the heating effects due to internal power dissipation are practically negligible, thus requiring no special consideration thermally during layout.

Layout Guidelines

One (or more) ground planes is/are recommended to minimize the effect of switching noise and copper losses, and maximize heat dissipation. The IC ground references, VSSA1 and VSSA2, should be kept separate from power ground. All components that are referenced to them should connect to them locally at the chip. VSSA1 and VSSA2 should connect to power ground at their respective output capacitors only.

Feedback traces must be kept far away from noise sources such as switching nodes, inductors and gate drives. Route feedback traces with their respective VSSAs as a differential pair from the output capacitor back to the chip. Run them in a “quiet layer” if possible.

Chip decoupling capacitors (VDDP, VCCA) should be located next to the pins and connected directly to them on the same side.

Power sections should connect directly to the ground plane(s) using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed to minimize loops and reduce losses. Make all the connections on one side of the PCB using wide copper filled areas if possible. Do not use “minimum” land patterns for power components. Minimize trace lengths between the gate drivers and the gates of the MOSFETs to reduce parasitic impedances (and MOSFET switching losses), the low-side MOSFET is most critical. Maintain a length to width ratio of <20:1 for gate drive signals. Use multiple vias as required by current handling requirement (and to reduce parasitics) if routed on more than one layer

Current sense connections must always be made using Kelvin connections to ensure an accurate signal.

We will examine the SC483 OUT2 reference design used in the Design Procedure section while explaining the layout guidelines in more detail, using the same generic components for OUT1.

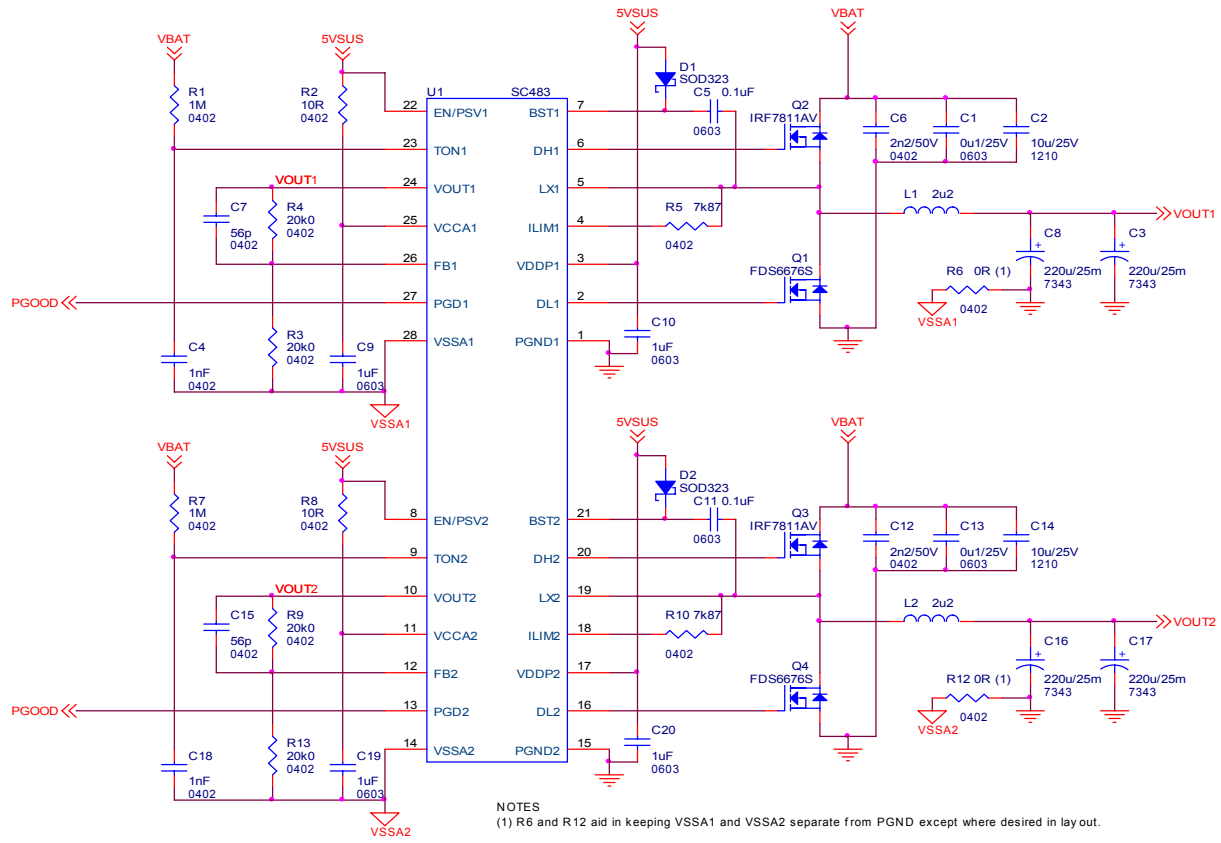


Figure 8: Reference Design and Layout Example

POWER MANAGEMENT

The layout can be considered in two parts, the control section referenced to VSSA1/2 and the power section. Looking at the control section first, locate all components referenced to VSSA1/2 on the schematic and place these components at the chip. Connect VSSA1 and VSSA2 using either a wide (>0.020") trace. Very little current flows in the chip ground therefore large areas of copper are not needed.

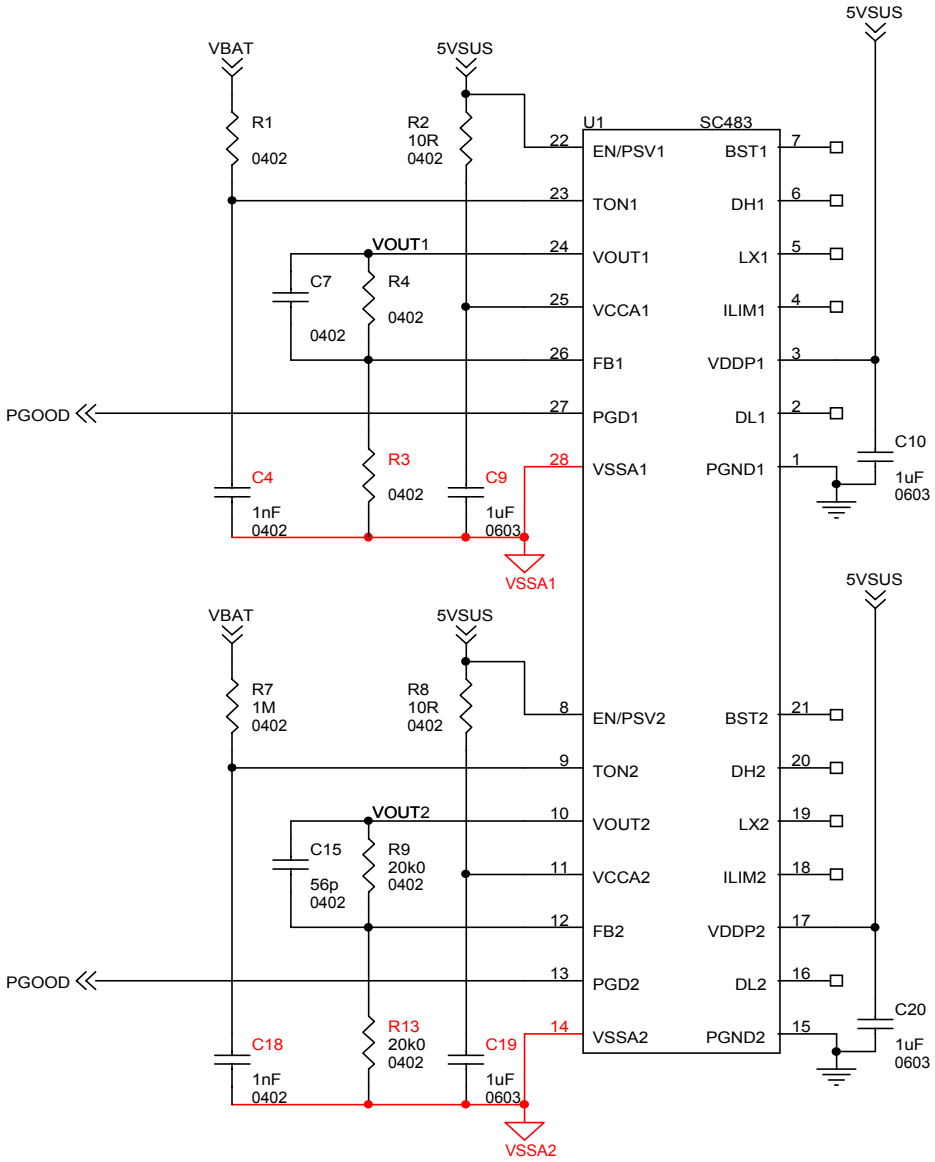


Figure 9: Components Connected to VSSA1 and VSSA2

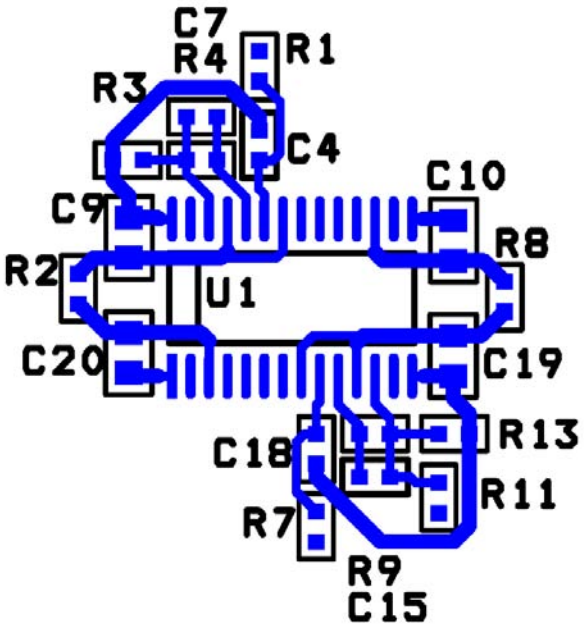


Figure 10: Example VSSA 0.020” Traces

In Figure 10, all components referenced to VSSA1 and VSSA2 have been placed and have been connected using 0.020” traces. Note that there are two separate traces, one for VSSA1 and one for VSSA2. Decoupling capacitors C9 and C19 are as close as possible to their pins, as are VDDP decoupling capacitors C10 and C20. C10 and C20 should connect to the ground plane using two vias each.

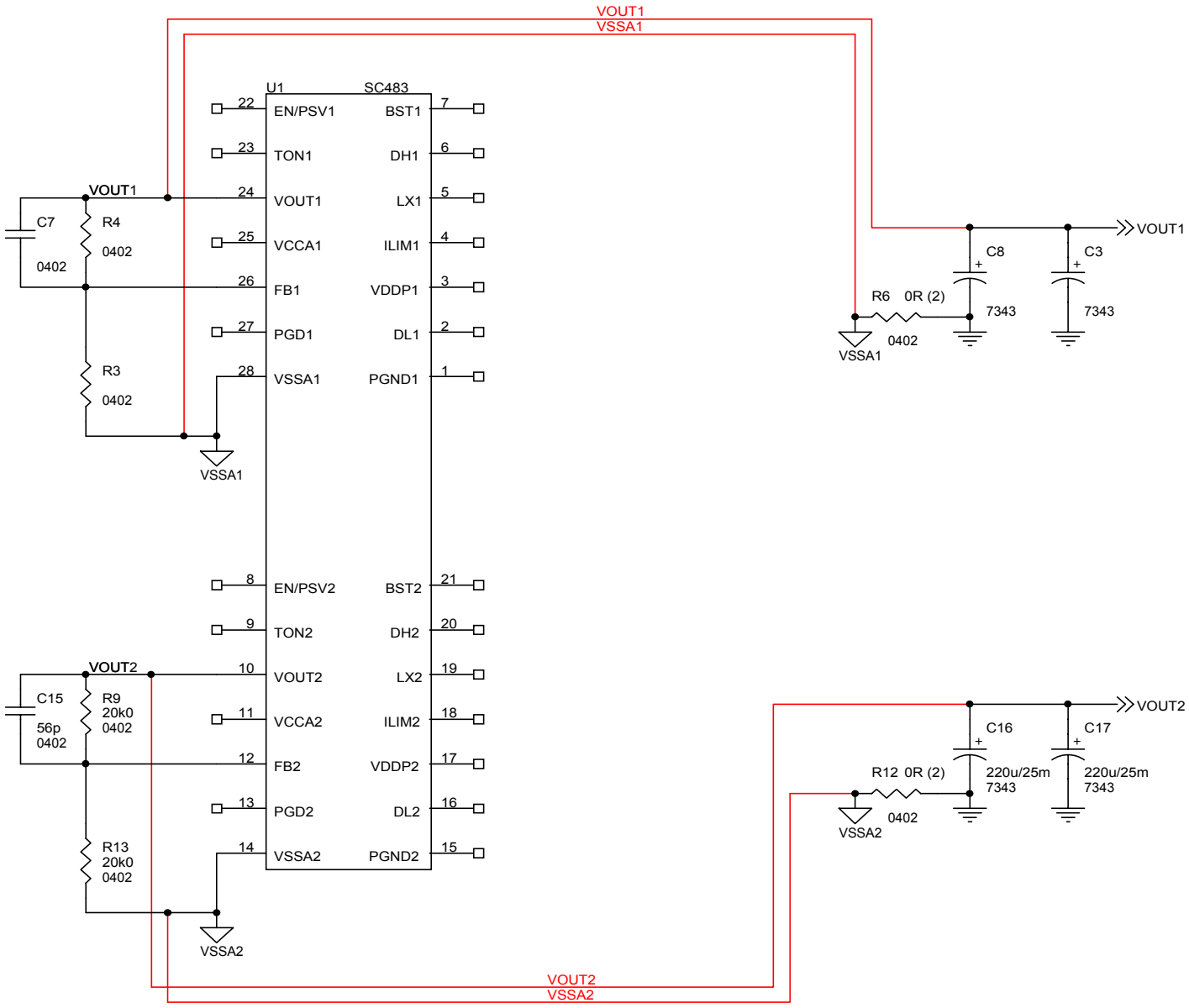


Figure 11: Differential Routing of Feedback and Ground Reference Traces

In Figure 11, VOUT1 and VSSA1 are routed as a differential pair from the output capacitors back to the feedback components and device. Similarly, VOUT2 and VSSA2 are routed as a differential pair from the output capacitors back to the feedback components and device.

Next, looking at the power section, the schematic in Figure 12 below shows the power section and input loop for OUT2:

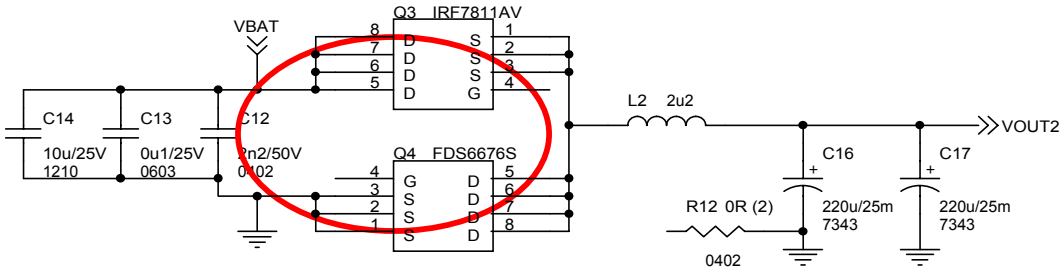


Figure 12: Power Section and Input Loop

The schematic has been redrawn to emphasize the input loop. The highest di/dts occur in the input loops and thus these should be kept as small as possible. The input capacitors should be placed with the highest frequency capacitors closest to the loop to reduce EMI. Use large copper pours to minimize losses and parasitics. Exactly the same philosophy applies to the OUT1 power section and input loop. Figure 13 below shows an example of the layout for the power section using these guidelines.

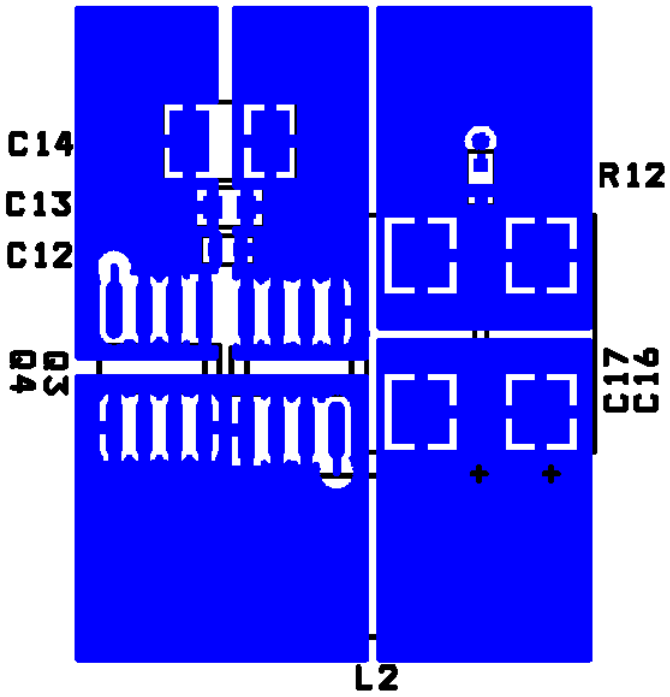


Figure 13: Power Component Placement and Copper Pours

Key points for the power section:
1) there should be a very small input loop, well decoupled.
2) the phase node should be a large copper pour, but compact since this is the noisiest node.
3) input power ground and output power ground should not connect directly, but through the ground planes instead.
4) The two outputs should not share their input capacitors, and these should have separate PWR_SRC and PGND (component-side) copper pours.
5) The two output inductors should not be placed adjacent to each other to avoid crosstalk.
6) Notice in Figure 13 placement of 0Ω resistor at the bottom of the output capacitor to connect to VSSA1/2 for each output.

Connecting the control and power sections should be accomplished as follows (see Figure 14 below):
1) Route VSSA1/2 and their related feedback traces as differential pairs routed in a “quiet” layer away from noise sources.
2) Route DL, DH and LX (low side FET gate drive, high side FET gate drive and phase node) to chip using wide traces with multiple vias if using more than one layer. These connections to be as short as possible for loop minimization, with a length to width ratio less than 20:1 to minimize impedance. DL is the most critical gate drive, with power ground as its return path. LX is the noisiest node in the circuit, switching between PWR_SRC and ground at high frequencies, thus should be kept as short as practical. DH has LX as its return path.
3) BST is also a noisy node and should be kept as short as possible.
4) Connect PGND pins on the chip directly to the VDDP decoupling capacitor and then drop vias directly to the ground plane.
5) Locate the current limit sense resistors between the LX and ILIM pins at the device.

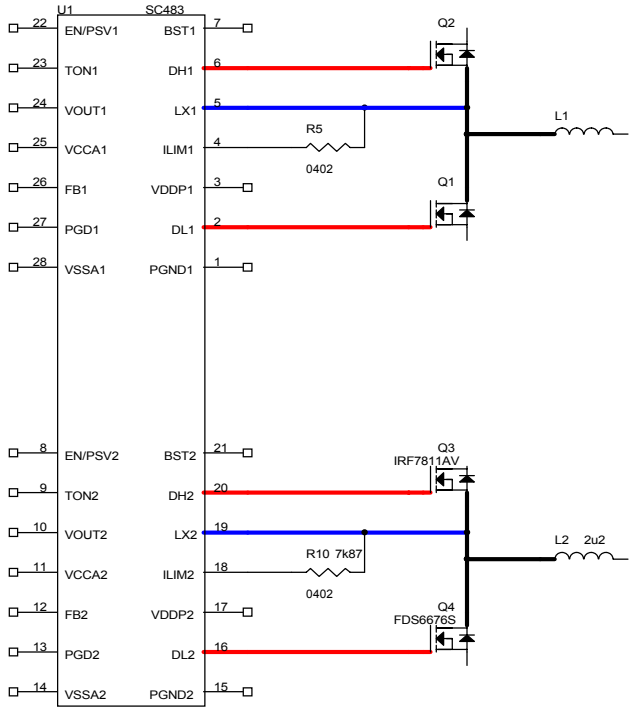
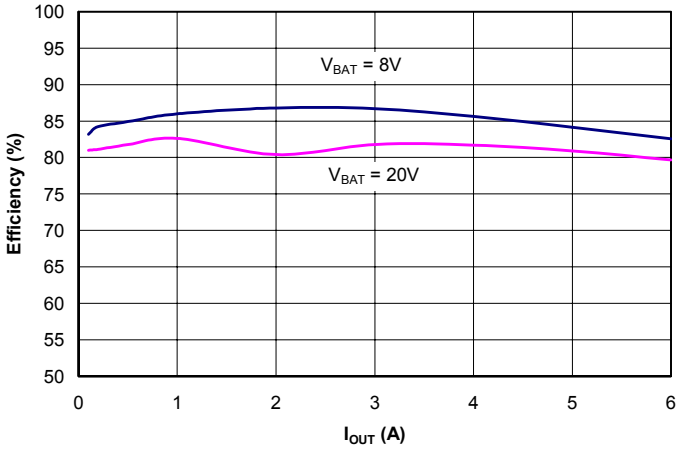


Figure 14: Connecting Control and Power Sections

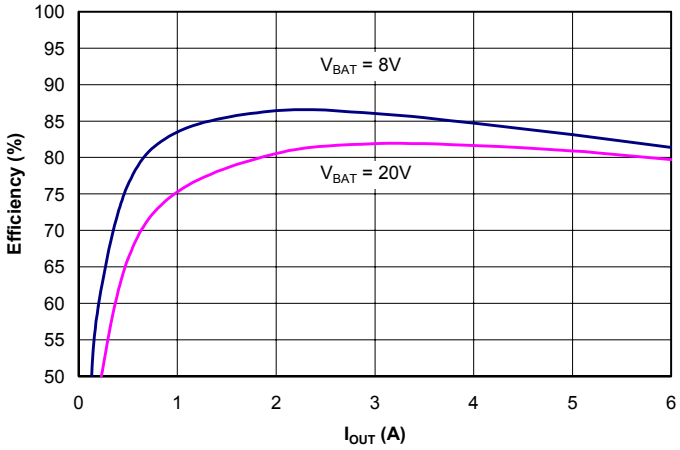
Phase nodes (black) to be copper islands (preferred) or wide copper traces. Gate drive traces (red) and phase node traces (blue) to be wide copper traces (L:W < 20:1) and as short as possible, with DL the most critical.

Typical Characteristics

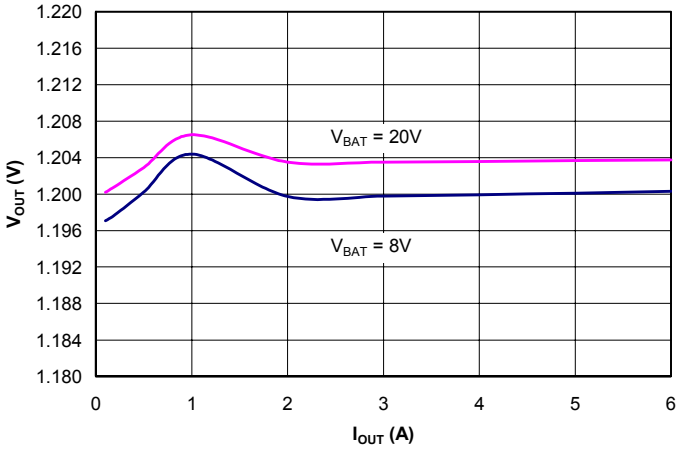
1.2V Efficiency (Power Save Mode) vs. Output Current vs. Input Voltage



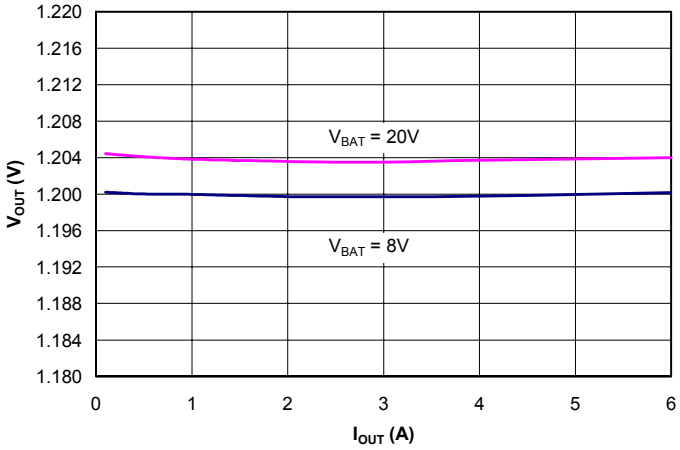
1.2V Efficiency (Continuous Conduction Mode) vs. Output Current vs. Input Voltage



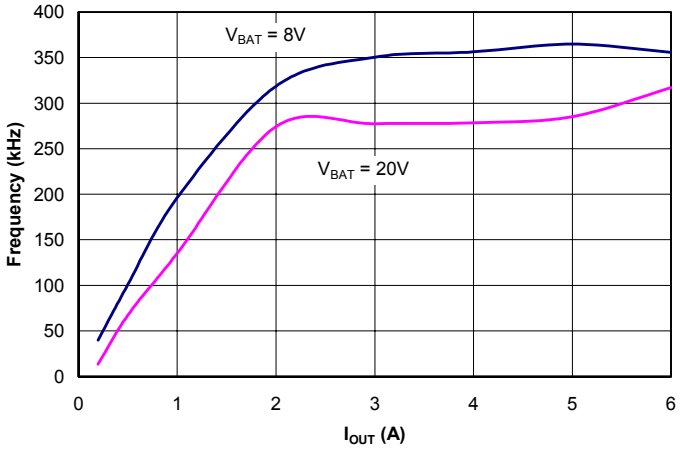
1.2V Output Voltage (Power Save Mode) vs. Output Current vs. Input Voltage



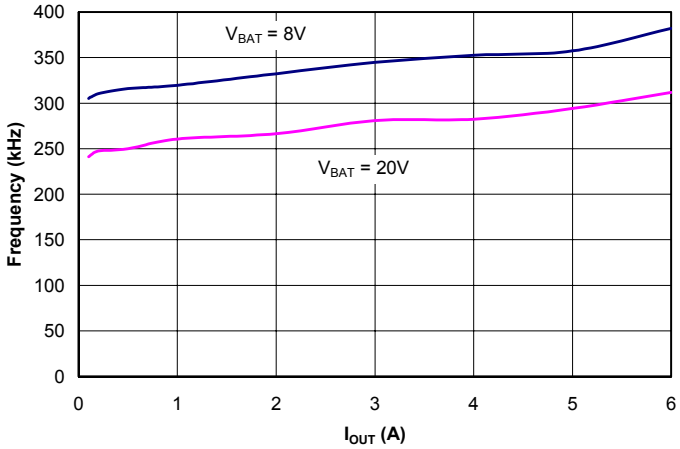
1.2V Output Voltage (Continuous Conduction Mode) vs. Output Current vs. Input Voltage



1.2V Switching Frequency (Power Save Mode) vs. Output Current vs. Input Voltage



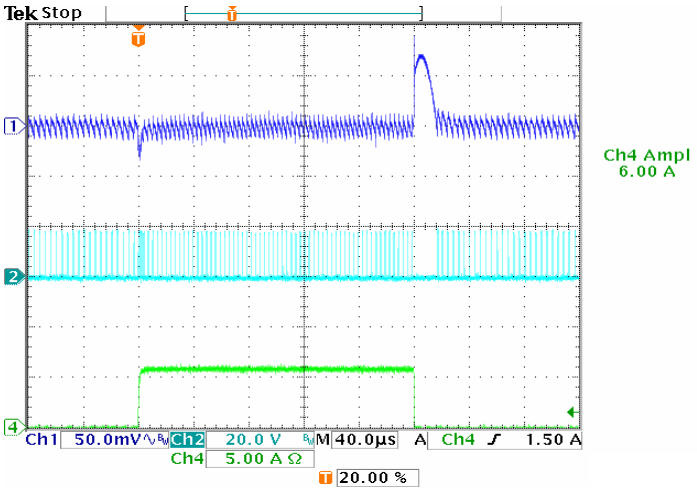
1.2V Switching Frequency (Continuous Conduction Mode) vs. Output Current vs. Input Voltage



Please refer to Figure 8 on Page 16 for test schematic (OUT2)

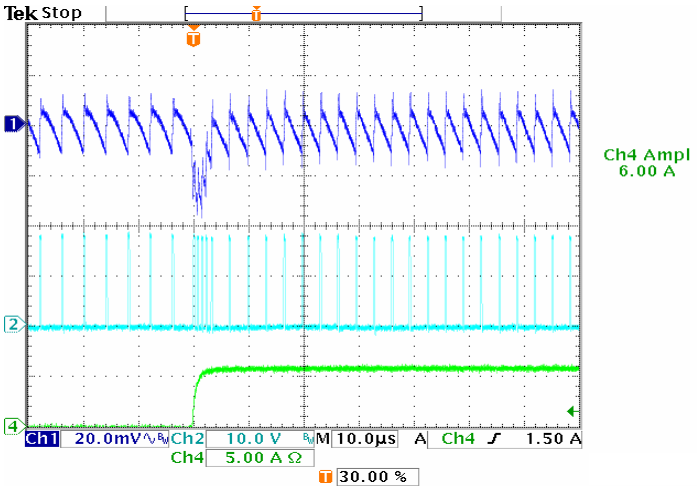
Typical Characteristics (Cont.)

Load Transient Response,
Continuous Conduction Mode, 0A to 6A to 0A



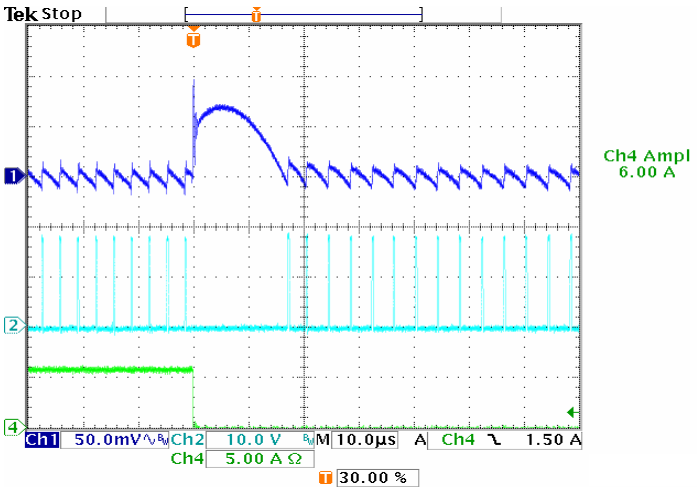
Trace 1: 1.2V, 50mV/div., AC coupled
Trace 2: LX, 20V/div
Trace 3: not connected
Trace 4: load current, 5A/div
Timebase: 40µs/div.

Load Transient Response,
Continuous Conduction Mode, 0A to 6A Zoomed



Trace 1: 1.2V, 20mV/div., AC coupled
Trace 2: LX, 10V/div
Trace 3: not connected
Trace 4: load current, 5A/div
Timebase: 10µs/div.

Load Transient Response,
Continuous Conduction Mode, 6A to 0A Zoomed

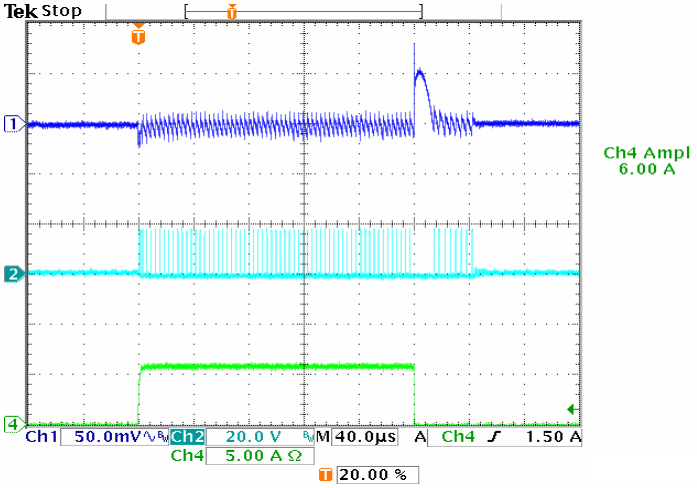


Trace 1: 1.2V, 50mV/div., AC coupled
Trace 2: LX, 10V/div
Trace 3: not connected
Trace 4: load current, 5A/div
Timebase: 10µs/div.

Please refer to Figure 8 on Page 16 for test schematic (OUT2)

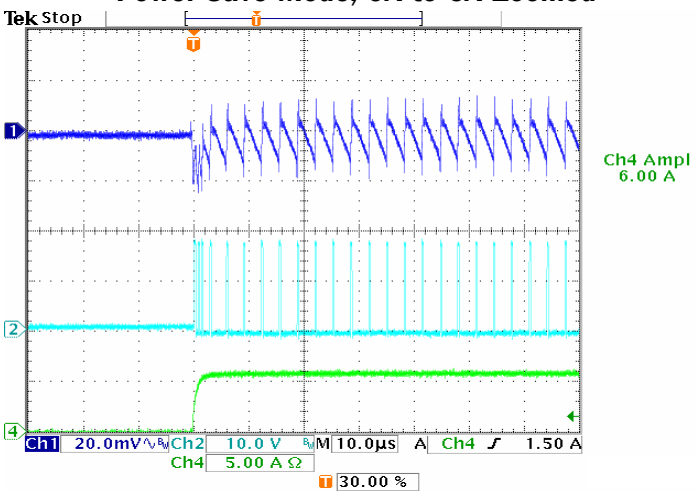
Typical Characteristics (Cont.)

**Load Transient Response,
Power Save Mode, 0A to 6A to 0A**



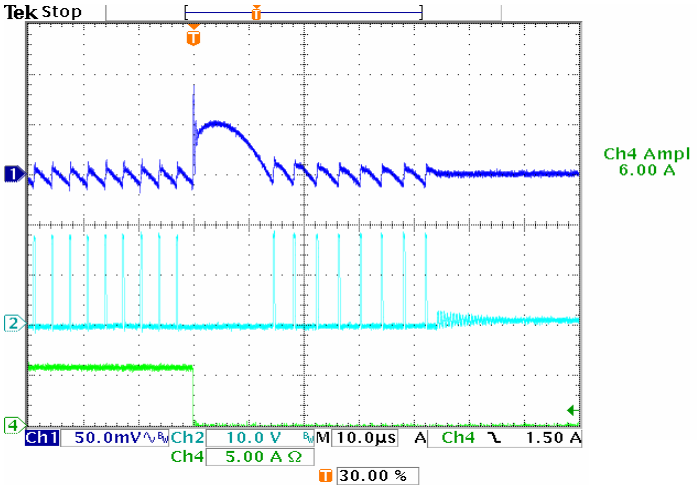
Trace 1: 1.2V, 50mV/div., AC coupled
Trace 2: LX, 20V/div
Trace 3: not connected
Trace 4: load current, 5A/div
Timebase: 40µs/div.

**Load Transient Response,
Power Save Mode, 0A to 6A Zoomed**



Trace 1: 1.2V, 20mV/div., AC coupled
Trace 2: LX, 10V/div
Trace 3: not connected
Trace 4: load current, 5A/div
Timebase: 10µs/div.

**Load Transient Response,
Power Save Mode, 6A to 0A Zoomed**

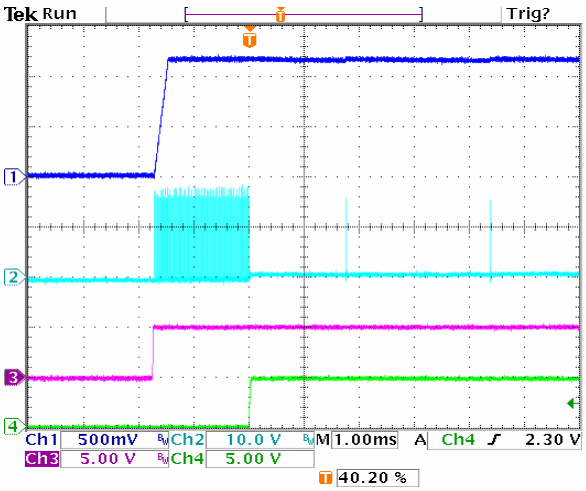


Trace 1: 1.2V, 50mV/div., AC coupled
Trace 2: LX, 10V/div
Trace 3: not connected
Trace 4: load current, 5A/div
Timebase: 10µs/div.

Please refer to Figure 8 on Page 16 for test schematic (OUT2)

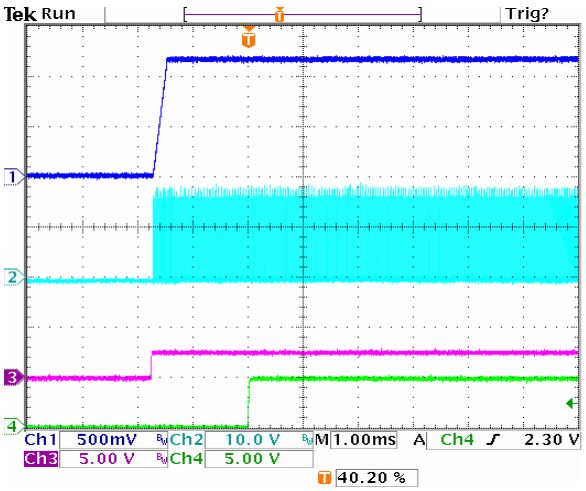
Typical Characteristics (Cont.)

Startup (PSV), EN/PSV Going High



Trace 1: 1.2V, 0.5V/div.
Trace 2: LX, 10V/div
Trace 3: EN/PSV, 5V/div
Trace 4: PGD, 5V/div.
Timebase: 1ms/div.

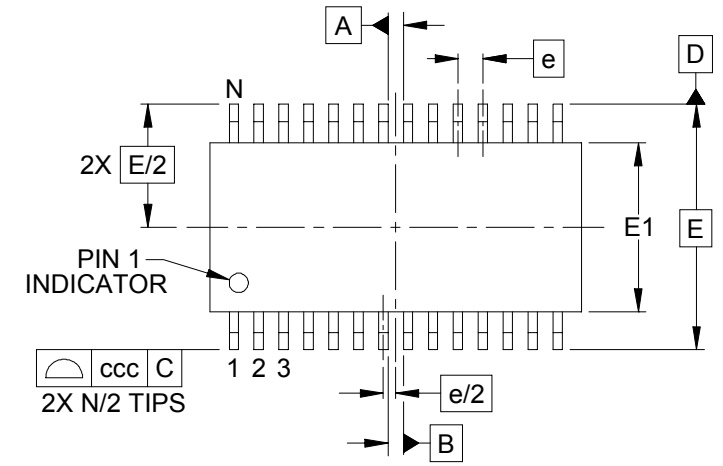
Startup (CCM), EN/PSV 0V to Floating

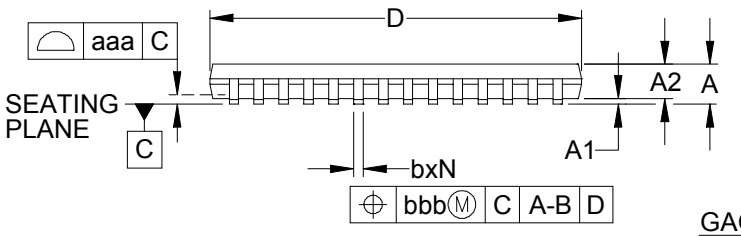


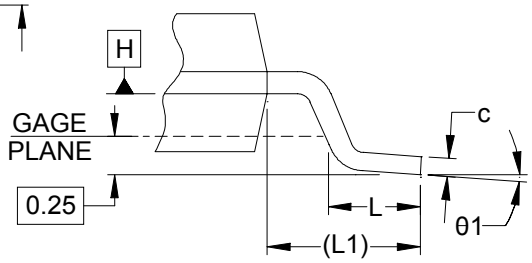
Trace 1: 1.2V, 0.5V/div.
Trace 2: LX, 10V/div
Trace 3: EN/PSV, 5V/div
Trace 4: PGD, 5V/div.
Timebase: 1ms/div.

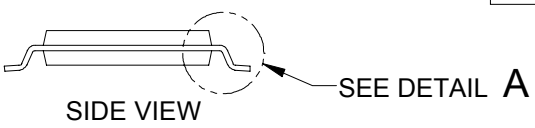
Please refer to Figure 8 on Page 16 for test schematic (OUT2)

Outline Drawing - TSSOP-28







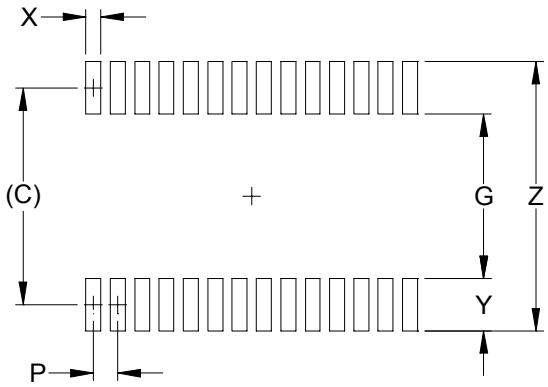


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.047	-	-	1.20
A1	.002	-	.006	0.05	-	0.15
A2	.031	-	.042	0.80	-	1.05
b	.007	-	.012	0.19	-	0.30
c	.003	-	.007	0.09	-	0.20
D	.378	.382	.386	9.60	9.70	9.80
E1	.169	.173	.177	4.30	4.40	4.50
E	.252 BSC			6.40 BSC		
e	.026 BSC			0.65 BSC		
L	.018	.024	.030	0.45	0.60	0.75
L1	(.039)			(1.0)		
N	28			28		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.004			0.10		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-153, VARIATION AE.

Land Pattern - TSSOP-28



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.222)	(5.65)
G	.161	4.10
P	.026	0.65
X	.016	0.40
Y	.061	1.55
Z	.283	7.20

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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