Semiconductor Solutions for High Speed Communications and Fiber Optic Applications

The Infineon Resilient Ring Processor is a packet optimized transport engine designed to enable the first generation of Resilient Packet Rings (RPR) for metropolitan area networks. Its feature-rich design supports spatial reuse protocol (SRP) at speeds up to 10 Gbit/s. It incorporates packet support for both POS and native Ethernet with the flexibility to transport across SONET, DWDM or dark fiber. The Infineon Resilient Ring Processor is uniquely positioned to enable cost-effective resiliency and QoS for growing, high-speed IP networks.

Key Features

- **High speed SRP MAC**
- **Up to OC-192 (10 Gbit/s) throughput**
- **Supports SRP, POS, Native Ethernet**
- **1 MB low-priority transit buffer**
- **32 KB high-priority transit buffer**
- **Giant, runt and short packet filters**
- **Supports IPS and topology discovery**
- **899-pin Hyper BGA package**

Specifications

Modes of Operation

- Dual ring mode
- Wrap mode
- Pass-through mode
- Transparent mode
- Passive and active sniffer modes

Operational Speeds

- OC-192
- OC-48

Packet Formats

- SRP
- Pseudo-SRP
- POS (in transparent mode)
- Native Ethernet

RX/TX Framer

Host Interface

- 64-bits HSTL @200 MHz
- OIF SPI-4 Phase 1 compliant interface
- Giant, runt and short packet filtering with PM counters
- Data and control parity bit checking with PM counters
- Traffic flow monitoring
- Host-side leaky bucket rate limiters - high/low priority
- Data parity fault insertion for system and software test
- Counters for high/low priority unicast/multicast packets and bytes

Lookup / Statistics CAM Functions

- 1024 Double (source, destination or both) address entries
- 1024 Double address counters
- CAM S/W features: read/write/probe/reset individual entries
- 8 coarse multicast address filters accept or reject on match
- Multicast accept/reject capability for individual addresses

Transit Buffer

- Internal source and sink for usage packets
- Internal 1 MB low and 32 KB high priority buffers
- Counters for high/low priority unicast/multicast packets and bytes
- Counters for min, max and average delay in transit buffers

MATE Interface

- XGMII 10 gigabit interface
- 4, 8-bit channels at 312.5 MHz (10.0 Gbit/s total capacity)
- Automatic pass-through/wrap/transparent mode communication
- Requires only 1 standard SERDES for inter-board communication
- Loss of sync detection with performance counters
- CRC detection

Microprocessor Interface

- 16-bit, asynchronous interface, up to 100 MHz
- Multiple interrupt reporting
- Send and receive buffers for IPS and topology packets

Electrical/Mechanical/Thermal

- 1.5/1.8/3.3 V power supplies
- 899-pin Hyper BGA Flip Chip package
- -40 °C to 85 °C operation
- ~5.18 W

Other

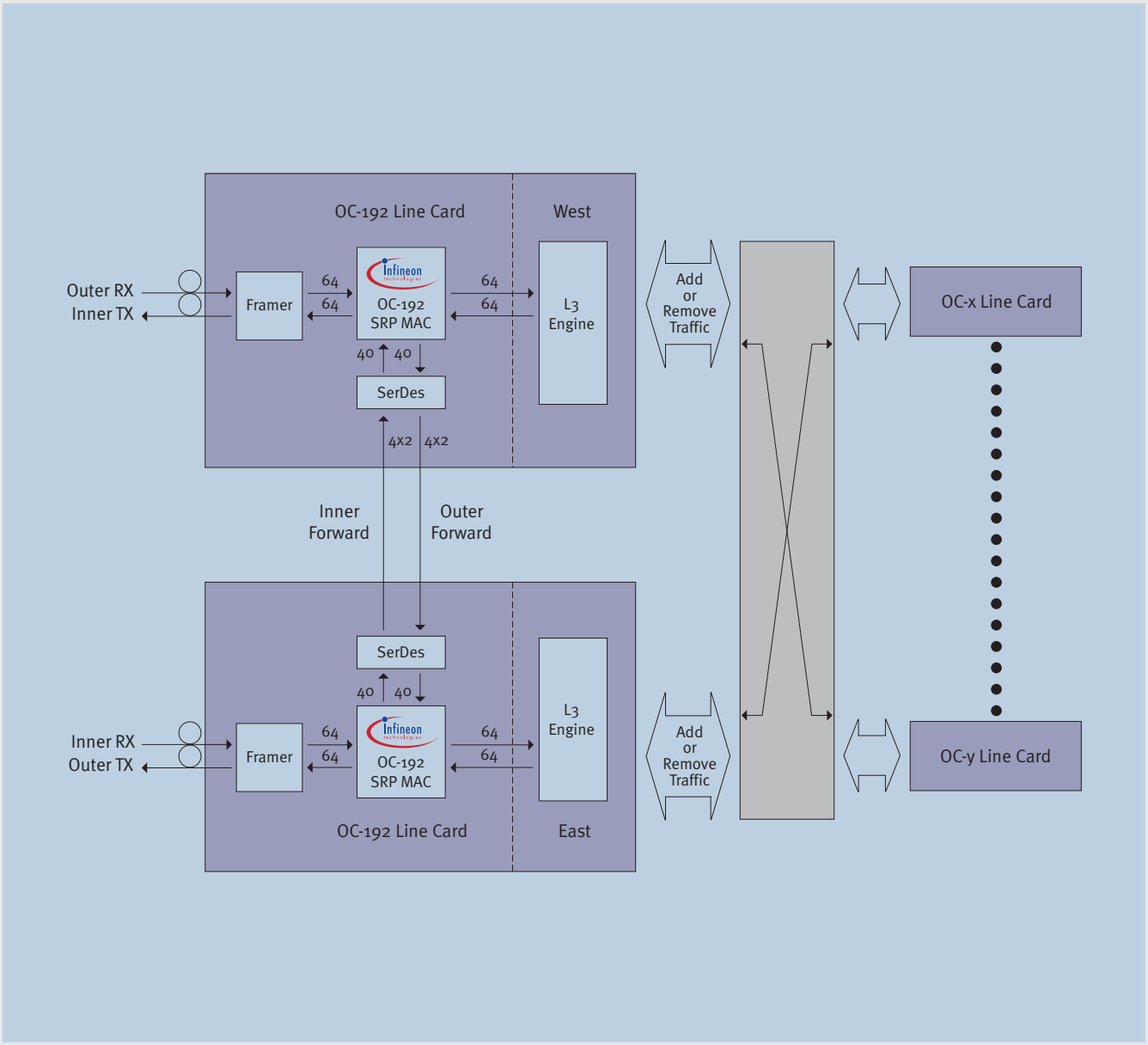
- JTAG Compliant
- 100 MHz or 200 MHz reference clock
- Hard and soft reset
- CRC generation and checking
- Extensive loopback features for testing

Rhea

Resilient Ring Processor OC-48 / OC-192 SRP MAC

Infineon technologies

Never stop thinking.



Block Diagram

How to reach us:
http://www.infineon.com

Infineon Technologies NA Corp.
1730 North First Street
San Jose, CA 95112 USA

Published by
Infineon Technologies AG,
St.-Martin-Strasse 53,
D-81541 München

Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide.

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Ordering No. B168-H8052-X-X-7600
Printed in Germany
PS 05022. R&L

Published by Infineon Technologies AG