To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

PRELIMINARY

Notice:This is not a final specification.
Some parametric limits are subject to change.

M65667SP

PICTURE-IN-PICTURE SIGNAL PROCESSING

DESCRIPTION

The M65667SP is a NTSC PIP (Picture in Picture) signal processing LSI, whose sub and main-picture inputs are composite and Y/C separated signals, respectively. The built-in field memory (96k-bit RAM) ,V-chip data slicer and analog circuitries lead the PIP system low cost and small size.

FEATURES

- Built-in 96k-bit field memory (sub-picture data storage)
- Internal V-chip data slicer (for sub-picture)
- Pin compatible with M65617SP
- Vertical filter for sub-picture (Y signal)
- Single sub-picture (selectable picture size : 1/9 , 1/16)
- Sub-picture processing sepecification (1/9 size / 1/16 size) :
  Quantization bits Y, B-Y, R-Y : 6bits
  Horizontal sampling 171 pixels (Y) , 28.5 pixels (B-Y, R-Y)
  Vertical lines 69/ 52 lines
- Frame (sub-picture) on/off
- Built-in analog circuits :
  Two 8-bit A/D converters (main and sub-picture signals)
  Two 8-bit D/A converters (Y and C sub-picture signals)
  Sync-tip-clump, VCXO, Analog switch ... etc.
- I²C BUS control (parallel/serial control) :
  PIP on/off , Sub-picture size(1/9 or 1/16), Frame on/off (programmable luma level), PIP position (4 corners fixed position), Picture freeze , Y delay adjustment, Chroma level, Tint, Black level, Contrast ... etc.

APPLICATION

NTSC color TV

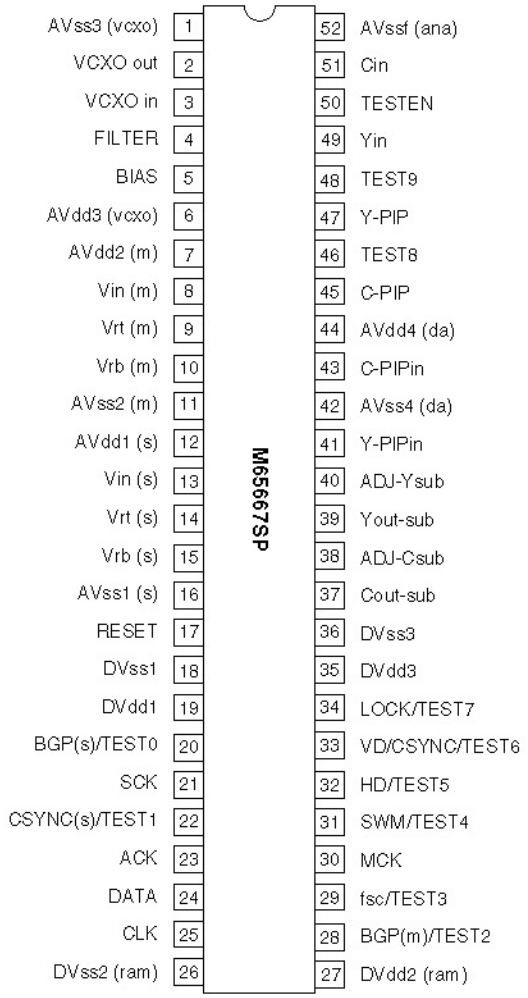
RECOMMENDED OPERATING CONDITION

Supply voltage range.....3.1 to 3.5V
Operating frequency.....14.32 MHz
Operating temperature.....-20 to 75 C
Input voltage (CMOS interface) "H".....VDD 0.7 to VDD V
"L".....0 to VDD 0.3V
Output current (output buffer)..... 4mA (MAX)
Output load capacitance.....20pF (MAX) [1]
Circuit current.....160mA

NOTICE: Connect a 0.1 F or larger capacitor between VDD and Vss pins.

1 : Include pin capacitance (7pF)

PIN CONFIGURATION (TOP VIEW)



Outline 52P4B

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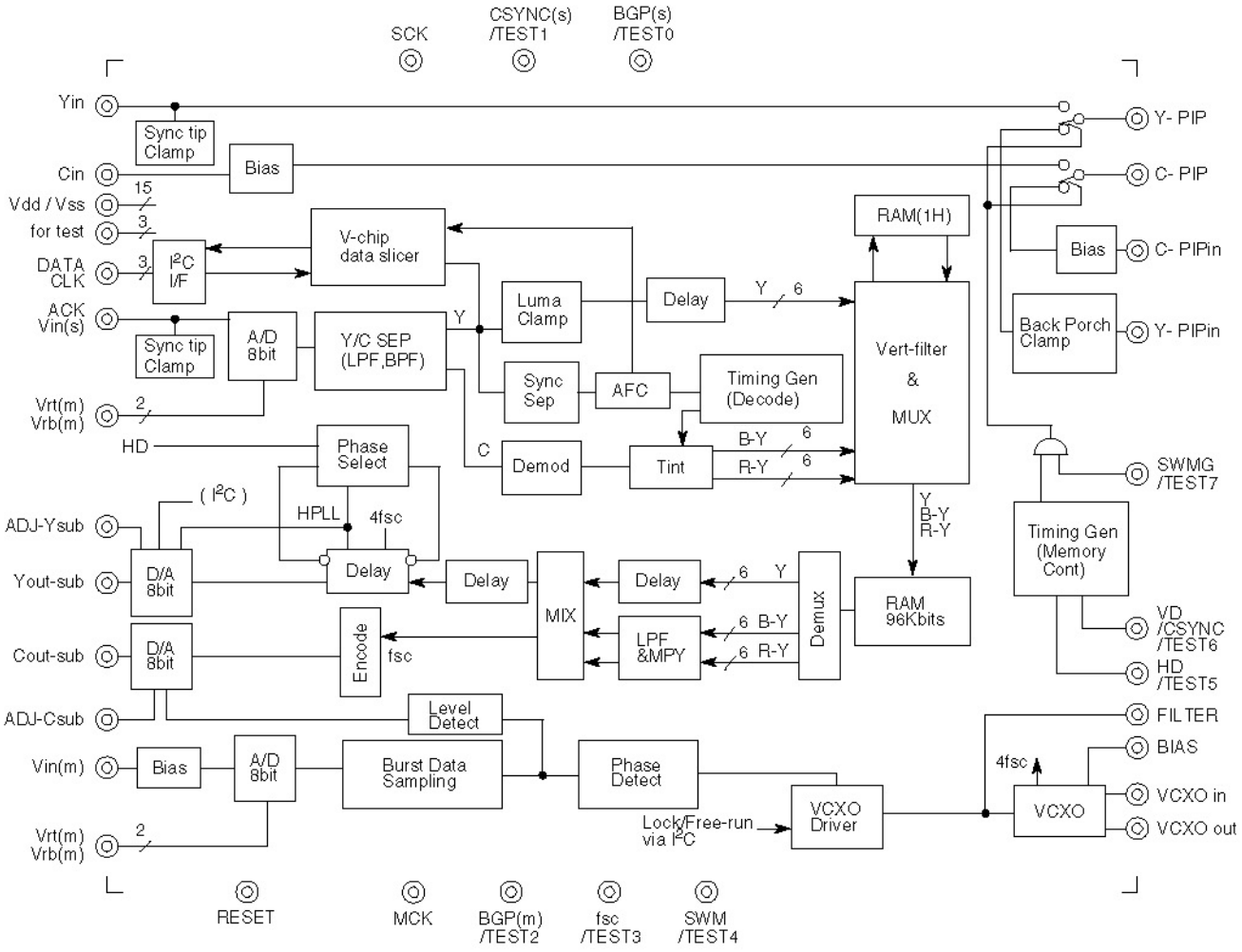
BLOCK DIAGRAM



DESCRIPTION OF PIN

Pin No.	Name	I/O	Function	Remarks
1	AVss3 (VCXO)	GND	Connects to analog GND	
2	VCXO out	O	VCXO output signal	
3	VCXO in	I	VCXO input signal	
4	FILTER	I	Filter	
5	BIAS	O	Bias	
6	AVdd3 (VCXO)	Vdd	Connect to analog power supply	
7	AVdd2 (m)	Vdd	Connect to analog power supply	
8	Vin (m)	I	Chroma signal input (main-picture)	
9	Vrt (m)	O	A/D Vref+ (main-picture)	
10	Vrb (m)	O	A/D Vref- (main-picture)	
11	AVss2 (m)	GND	Connect to analog GND	
12	AVdd1 (s)	Vdd	Connect to analog power supply	
13	Vin (s)	I	Composite video signal input (sub-picture)	
14	Vrt (s)	O	A/D Vref+ (sub-picture)	
15	Vrb (s)	O	A/D Vref- (sub-picture)	
16	AVss1 (s)	GND	Connect to analog GND	
17	RESET	I	Power on reset input signal ("L" reset)	100k to VDD,10 F to GND
18	DVss1	GND	Connect to digital GND	
19	DVdd1	Vdd	Connect to digital power supply	
20	BGP(s)/TEST0	(I/)O	For test	non connect
21	SCK	I	For test (connect to digital GND)	connect to GND
22	CSYNC(s)/TEST1	I(/O)	For test (connect to digital GND)	pull down 15k
23	ACK	O	I²C bus-data/Acknowledge output signal	
24	DATA	I	I²C bus-data input signal	
25	CLK	I	I²C bus-clock input signal	
26	DVss2(ram)	GND	Connect to digital GND	
27	DVdd2(ram)	Vdd	Connect to digital power supply	
28	BGP(m)/TEST2	(I/)O	For test	non connect
29	fsc/TEST3	I(/O)	For test (pull down to digital GND by resistor 15k)	pull down 15k
30	MCK	I	For test (connect to digital GND)	connect to GND
31	SWM/TEST4	(I/)O	For test	non connect
32	HD/TEST5	I(/O)	Horizontal sync input signal (Positive going edge is used)	
33	VD/CSYNC /TEST6	I(/O)	Vertical sync input signal (active "H")	
34	SWMG/TEST7	I(/O)	Enable input signal to display sub picture ("H" enable)	pull up 15k
35	DVdd3	Vdd	Connect to digital power supply	
36	DVss3	GND	Connect to digital GND	
37	Cout-sub	O	D/A output signal (Chroma signal of sub-picture)	
38	ADJ-Csub	I	D/A adjust for chroma signal (sub-picture)	
39	Yout-sub	O	D/A output signal (Luma signal of sub-picture)	
40	ADJ-Ysub	I	D/A adjust for luma signal (sub-picture)	
41	Y-PIPin	I	PIP luma signal re-input	
42	AVss4 (da)	GND	Connects to analog GND	
43	C-PIPin	I	PIP chroma signal re-input	
44	AVdd4 (da)	Vdd	Connect to analog power supply	
45	C-PIP	O	PIP chroma signal output	
46	TEST8	I	For test (connect to analog GND)	pull up 15k
47	Y-PIP	O	PIP luma signal output	
48	TEST9	I	For test (connect to analog GND)	connect to GND
49	Yin	I	Luma input signal (main-picture)	
50	TESTEN	I	For test (connect to analog GND)	connect to GND
51	Cin	I	Chroma input signal (main-picture)	
52	AVssf (ana)	Vss	Connect to analog GND	

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ABSOLUTE MAXIMUM RATINGS (Vss=0V)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
V_{DD3}	Supply voltage (3.3V)	-0.3	4.6	V
V_I	Input voltage	-0.3	V_{DD3}+0.3	V
V_O	Output voltage	-0.3	V_{DD3}+0.3	V
I_O	Output current (1)		I_{OL}=20 I_{OH}=-26	mA
P_d	Power dissipation		1400	mW
T_{opr}	Operating temperature	-20	75	C
T_{stg}	Storage temperature	-50	125	C

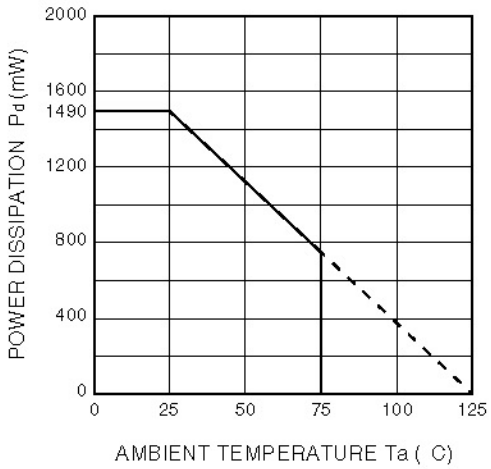
1: Output current per output terminal. But P_d limits all current.

DC CHARACTERISTICS (Ta=25 C, unless otherwise noted, Vss=0V)

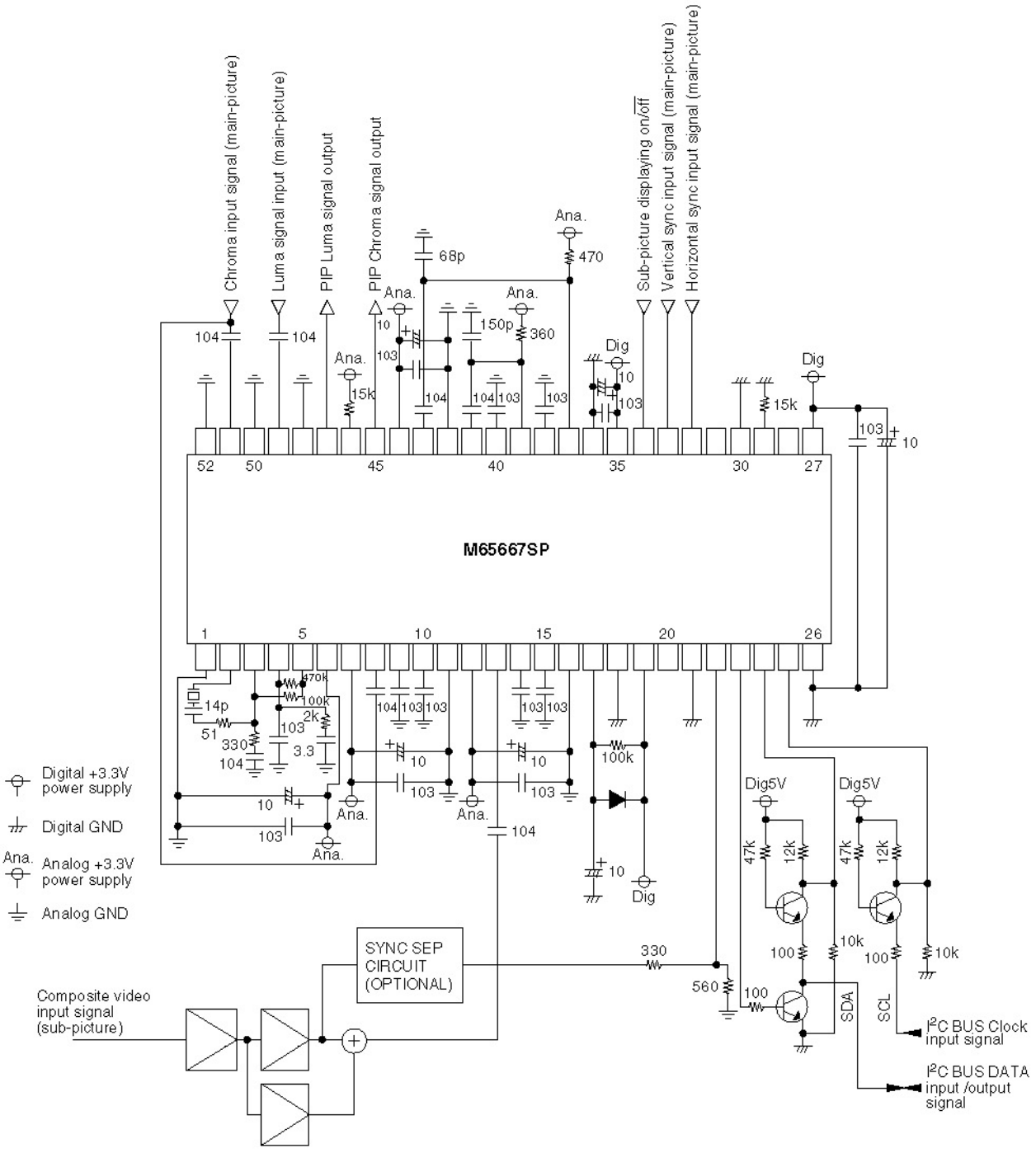
Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{IL}	Input voltage (CMOS interface)	L	V_{DD}=2.7V	0		0.81	V
V_{IH}		H	V_{DD}=3.6V	2.52		3.6	V
V_{T-}	Input voltage schmitt trigger (CMOS interface)	–	V_{DD}=3.3V	0.5		1.65	V
V_{T+}		+		1.4		2.4	V
V_H		Hysteresis		0.3		1.2	V
V_{OL}	Output voltage	L	V_{DD}=3.3V, |Io| <1 A			0.05	V
V_{OH}		H		3.25			V
I_{OL}	Output current	L	V_{DD}=3.0V, V_{OL}=0.4V	4			mA
I_{OH}		H	V_{DD}=3.0V, V_{OH}=2.6V			-4	mA
I_{IH}	Input current	L	V_{DD}=3.6V, V_I=0V	-1		1	A
I_{IL}		H	V_{DD}=3.6V, V_I=3.6V	-1		1	A
I_{OZL}	Output leakage current	L	V_{DD}=3.6V, V_O=0V	-1		1	A
I_{OZH}		H	V_{DD}=3.6V, V_O=3.6V	-1		1	A
C_I	Input pin capacitance		f=1MHz, V_{DD}=0V		7	15	pF
C_O	Output pin capacitance				7	15	pF
C_{IO}	Bidirectional pin capacitance				7	15	pF
I_{DD}	Operating current	3.3V supply				140	mA

TYPICAL CHARACTERISTICS

THERMAL DERATING (MAXIMUM RATING)



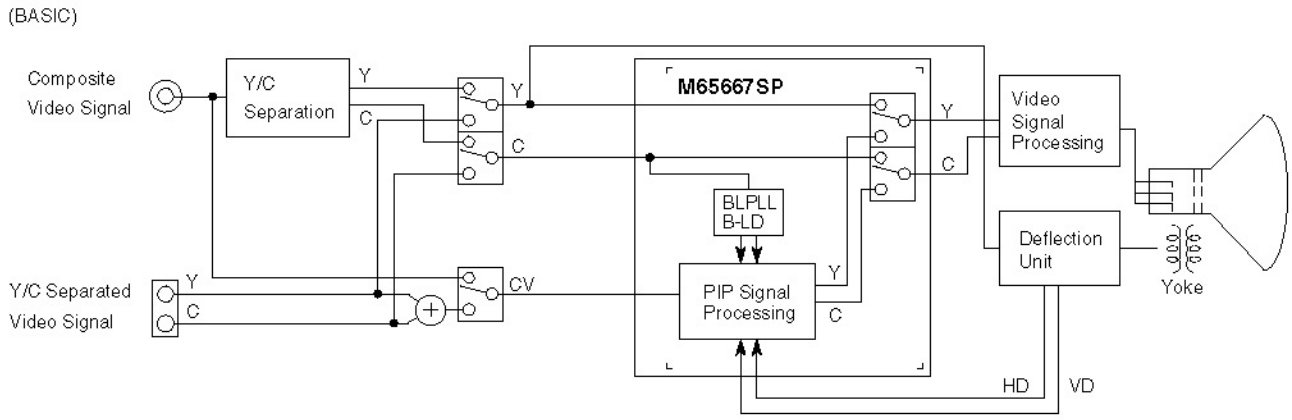
APPLICATION EXAMPLE



Separate Y/C signals by using LC-tank circuit or LPF,BPF for Y/C signals level adjust.
And then mix both signals for sub-picture input video signal.

Units Resistance :
Capacitance : F

PIP TV SYSTEM BLOCK DIAGRAM



(Driving Method and Operating Specification for Serial Interface Data)

(1) Serial data transmission completion and start

A low-to-high transition of the DATA (serial data) line while the CLK (serial clock) is high, that completes the serial transmission and makes the bus free.

A high-to-low transition of the DATA line while the CLK is high, that starts the serial transmission and waits for the following CLK and DATA inputs.

(2) Serial data transmission

The data are transmitted in the most significant bit (MSB) first by one-byte unit on the DATA line successively. One-byte data transmission is completed by 9 clock cycles, the former 8 cycles are for address/data and the latter one is for acknowledge detection. (In reading state, ACK is 'H' under these two conditions ; 1) the coincidence of two address data for the address data transmission, 2) the completion of 8-bit setting data transfer. In writing state, ACK is 'H' with the address coincidence and ACK is 'L' for detecting acknowledge input from the master (micro processor) after sending 8-bit setting data.)

For address/data transmission, DATA must change while CLK is 'L'. (The data change while CLK is 'H' or the simultaneous change of CLK and DATA, that will be a false operation because of undistinguished condition from the completion/start of serial data transfer).

After the beginning of serial data transmission, the total number of data bytes that can be transferred are not limited.

(3) The byte format of data transmission (The sequence of data transmission)

1. The byte format during data setting to M65667SP are shown as follows.

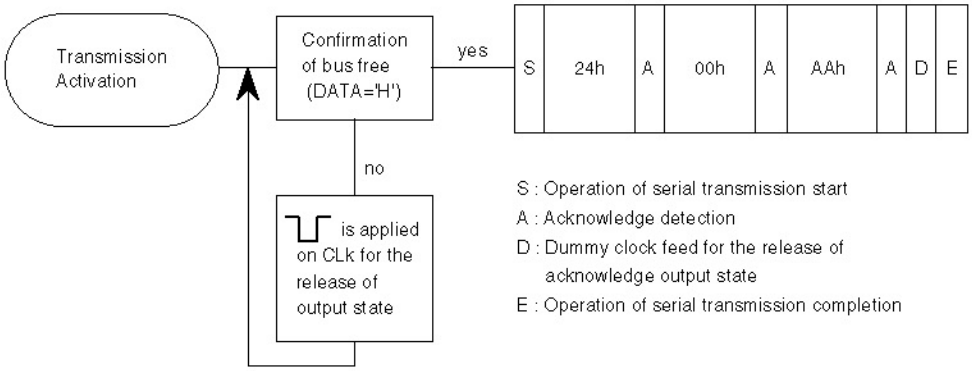
In right after the forming of serial data transmitting state, the slave address 24h (00100100b) is transferred. Afterwards, the internal register address (1 byte) and setting data (by 1 byte unit) are transferred successively. Several bytes of setting data can be handled in the one transmission. In this operation, the setting data are written into the address register whose address is increased one in initially transferred internal register address. (The next address of 7Fh, it returns to 00h).

2. The byte format during data reading from M65667SP are shown as follows.

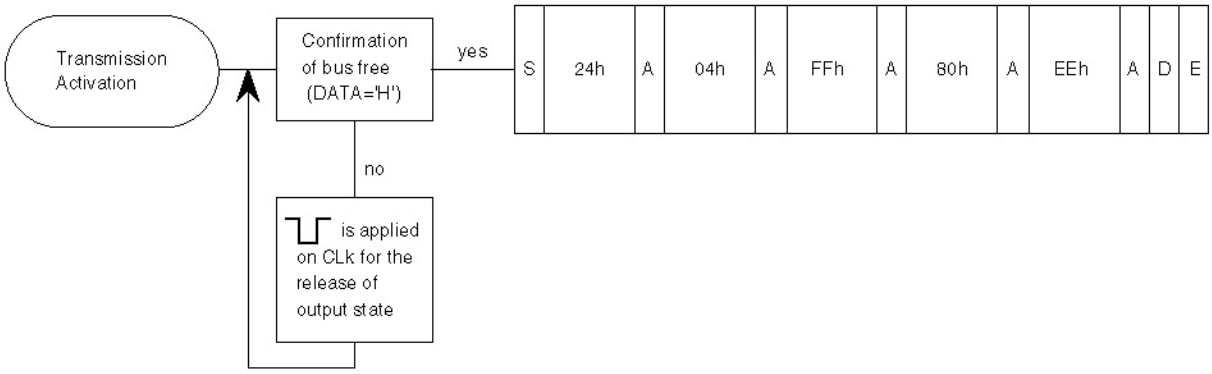
Before data reading from M65667SP, whose internal address need to be set by the data reading/transmitting. After the data reading/transmitting, the operation of "serial data transmission completion and start" (described in (1)) is necessary. Continuously, the slave address 25h (00100101b) is sent, and then the inverted read out data are available on ACK. Several bytes of writing data can be handled in the one transmission, too. In this operation, the setting data also are written into the address register whose address is increased one in initially transferred internal register address. (The next address of 7Fh, it returns to 00h).

(The examples of serial byte transmission format)

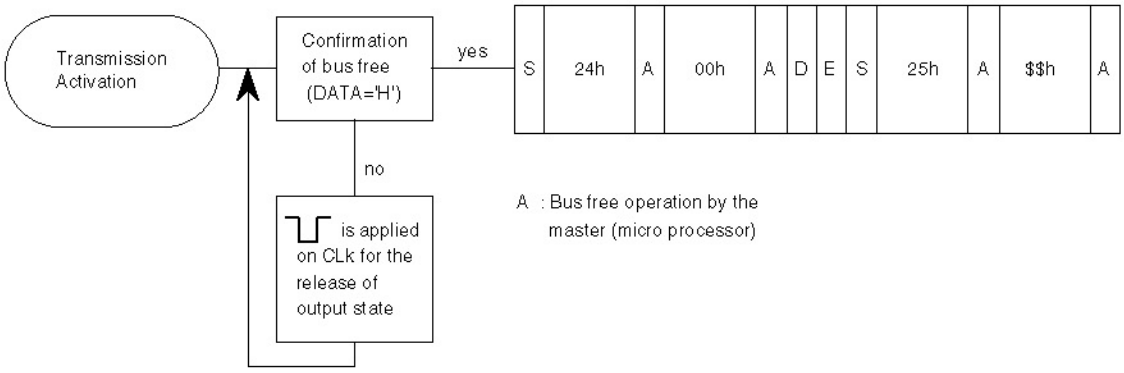
(1) The writing operation of the setting data (AAh) into M65667SP internal address of 00h



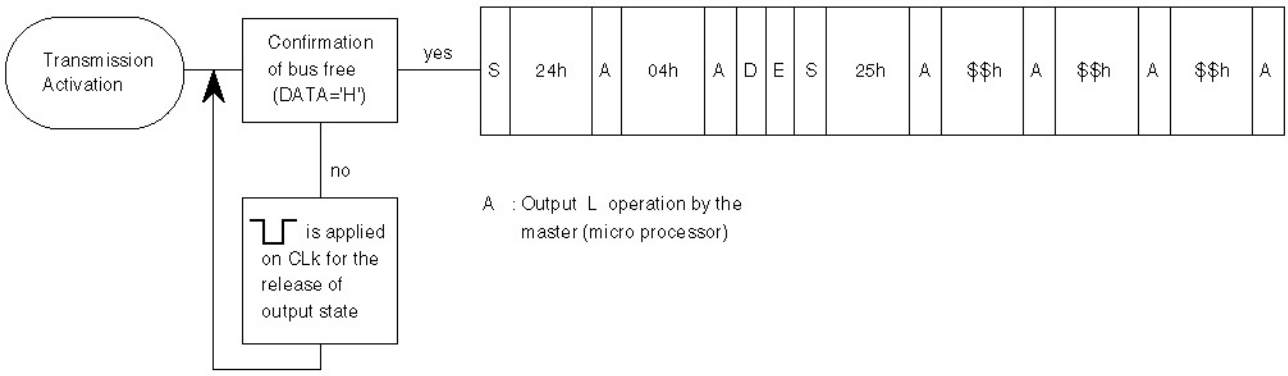
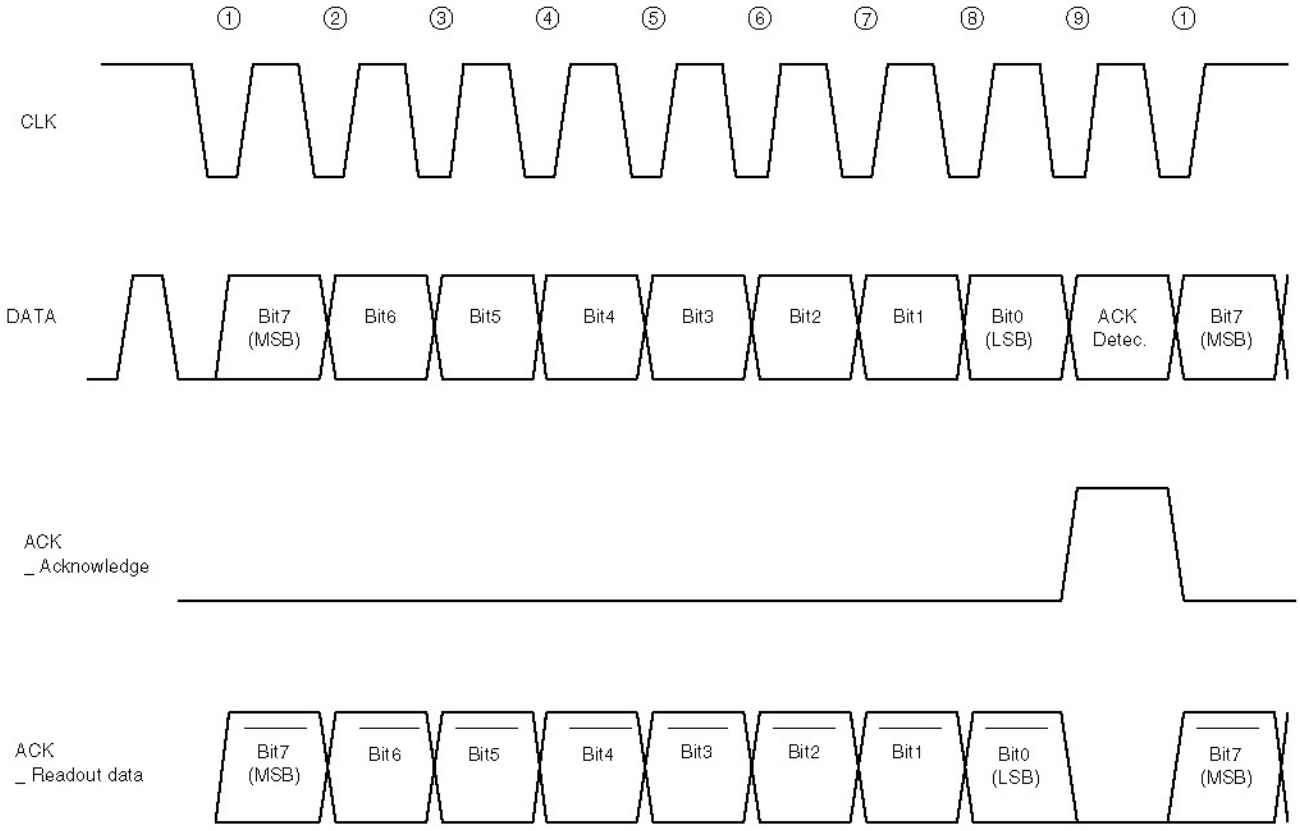
(2) The writing operation of the setting data (FFh, 80h, EEh) into M65667SP internal address of 04h to 06h



(3) The reading operation of the setting data from M65667SP internal address of 00h



(4) The reading operation of the setting data from M65667SP internal address of 04h to 06h



TIMING DIAGRAM