M65665CFP/SP

PICTURE-IN-PICTURE SIGNAL PROCESSING

REJ03F0011-0100Z
Rev.2.00
Sep.04.2003

Description

The M65665CFP/SP is a PIP (Picture in Picture) signal processing LSI, whose sub-picture input is composite signal or component signals(Y/C or Y/U/V) for NTSC.

The built-in field memory (168k-bit RAM) , V-chip data slicer and analog circuitries lead the high quality PIP system low cost and small size.

Features

- Internal V-chip data slicer (for sub-picture)
- Vertical filter for sub-picture (Y signal)
- Base band com filter (2 Line)
- Single sub-picture (selectable picture size : 1/9 , 1/16)
- Sub-picture processing specification (1/9 , 1/16 size) :
  Quantization bits Y, B-Y, R-Y : 7 bits
  Horizontal sampling 229 pixels (Y), 57 pixels (B-Y, R-Y)
  Vertical lines 69/ 52 lines
- Frame (sub-picture) on/off
- Built-in analog circuits :
  Two 8-bit A/D converters (for sub-picture signal)
  Three 8-bit D/A converters (for Y, U and V of sub-picture)
  Auto Slicer(Sync Sep.), Sync-tip-clamp, VCXO, OSD switch, etc..
- I^{l}C BUS control (parallel/serial control) :
  PIP on/off , Frame on/off (programmable luma level),
  Sub-picture size (1/9, 1/16),
  PIP position (free position), Picture freeze ,
  Y delay adjustment, Chroma level, Tint, Black level, Contrast ...etc..

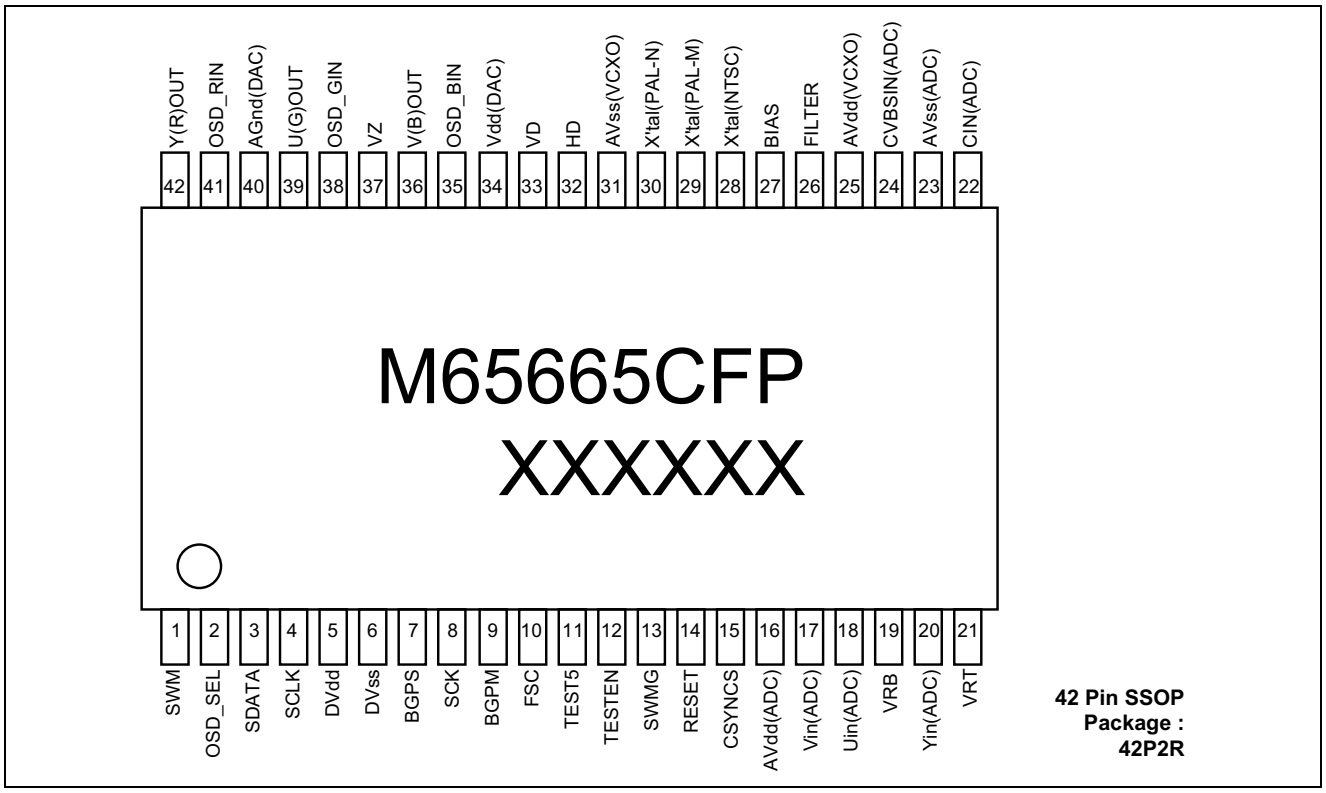
Application

NTSC color TV

Recommended Operating Conditions

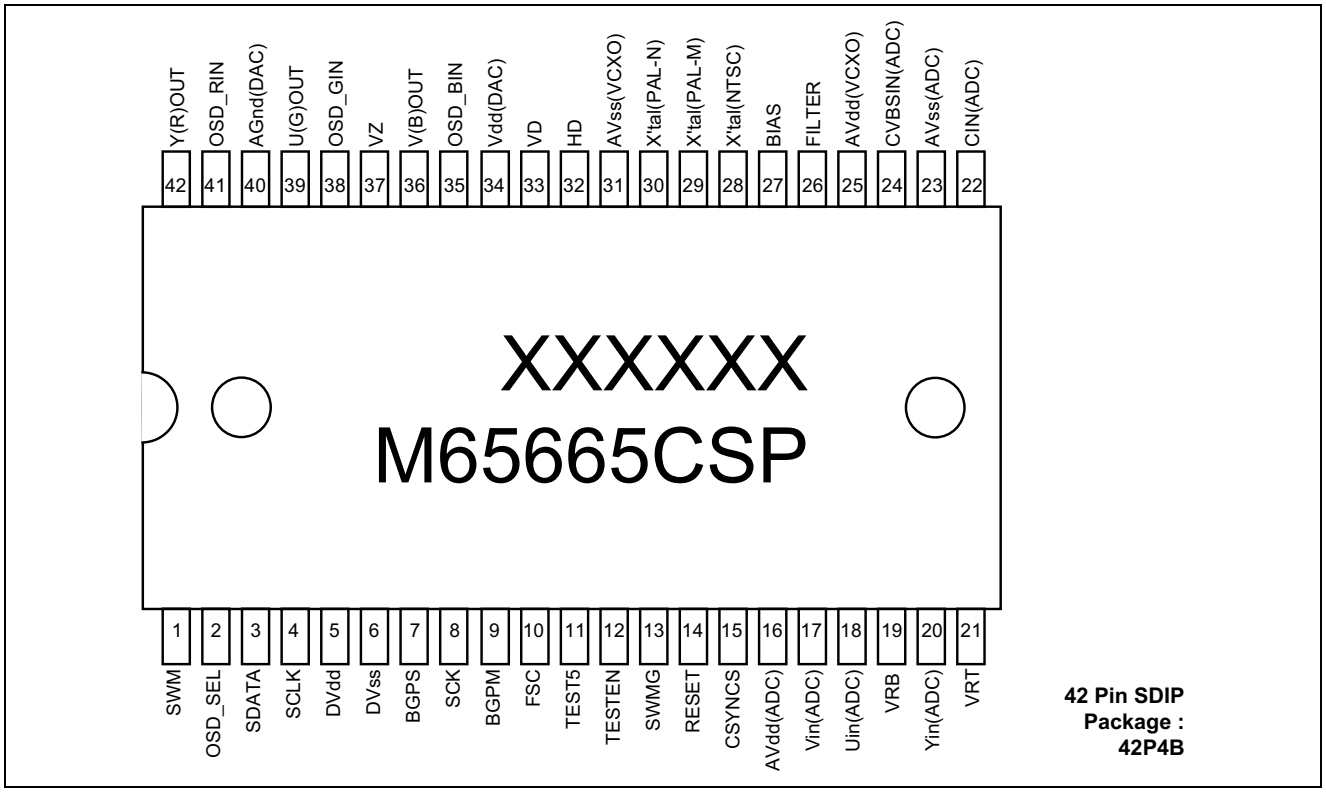
Supply voltage range ---------- 3.2 to 3.5 V
Recommended supply voltage ---------- 3.3 V

Pin Configuration of M65665CFP (Top View)



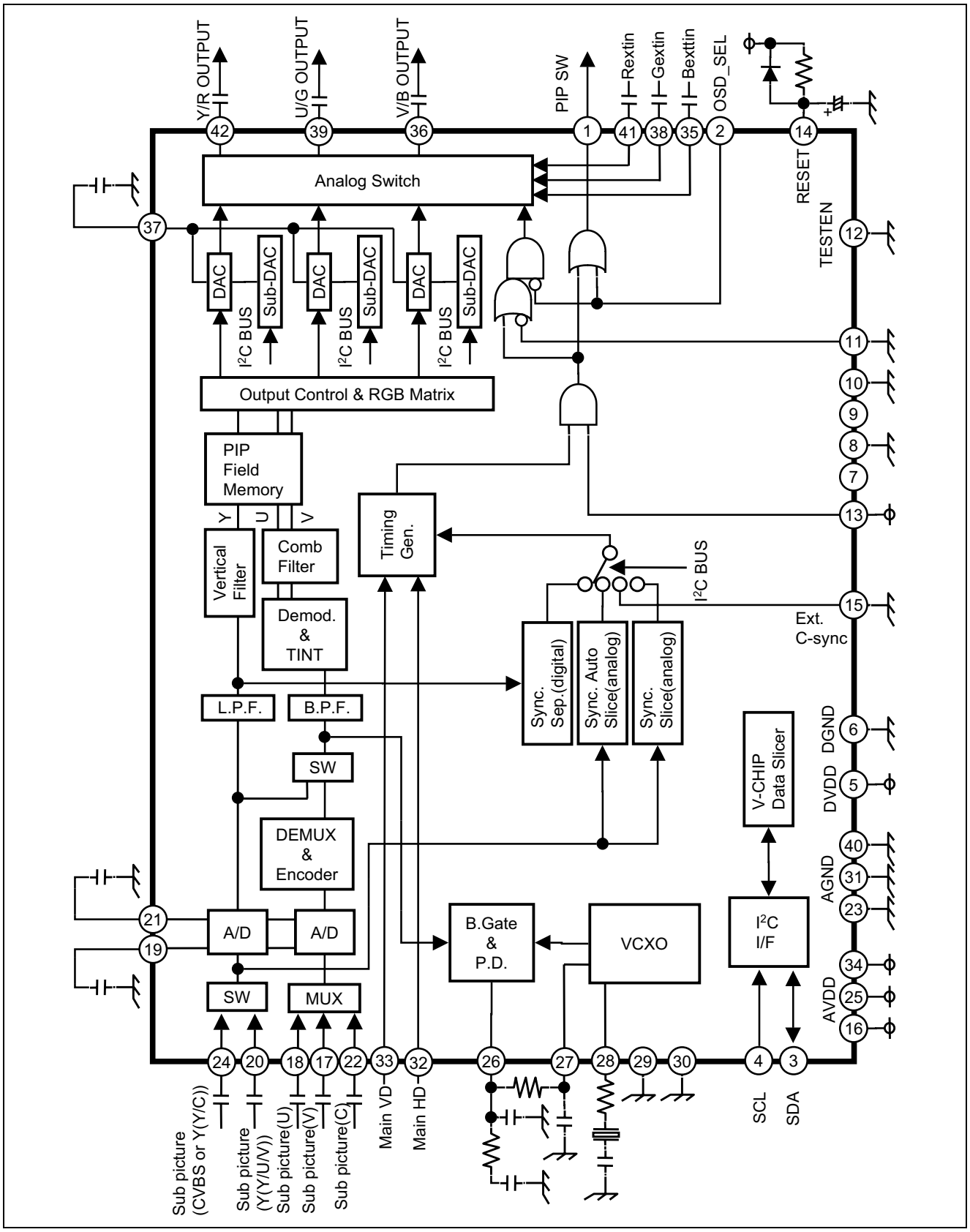
42 Pin SSOP
Package :
42P2R

Pin Configuration of M65665CSP (Top View)



42 Pin SDIP
Package :
42P4B

Block Diagram



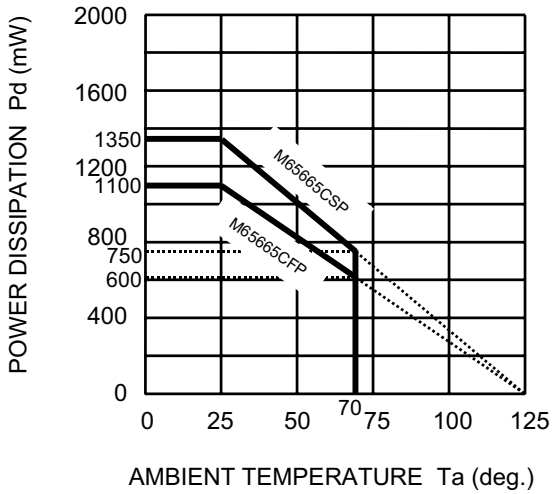
Absolute Maximum Ratings

(Vss=0 V)

Parameter	Symbol	Limits Min.	Limits Max.	Unit	Conditions
Supply voltage (3.3V)	VDD3	–0.3	4.2	V	
Input voltage (except for 5V input)	VI3	–0.3	VDD3+0.3	V	
Input voltage (5V)	VI5	–0.3	5.25	V	
Output voltage	VO	–0.3	VDD3+0.3	V	
Output current (*1)	IO	IOH=–4	IOL=4	mA	
Operating temperature	Topr	–10	70	deg.	
Storage temperature	Tstg	–50	125	deg.	

Note : 1. Output current per output terminal. But Pd limits all current.

THERMAL DERATING (MAXIMUM RATING)



Recommended Operating Conditions

(Ta = 25 °C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply voltage	VDD3	3.2	3.3	3.5	V	
Operating frequency	fopr	—	14.32	—	MHz	
“H” Input voltage (CMOS interface)	VIH	VDD3×0.7	—	VDD3	V	
“L” Input voltage (CMOS interface)	VIL	0	—	VDD3×0.3	V	
Output current (output buffer)	IO	—	—	2	mA	
Output load capacitance	C_{OL}	—	—	20	pF	Include pin capacitance (7pF)

DC Characteristics

(Ta = 25 deg. unless otherwise noted)
(VSS=0V)

Parameter		Symbol	Limits Min.	Typ.	Max.	Unit	Conditions
Input voltage (3.3V CMOS interface)	L	VIL	0	—	0.81	V	VDD=2.7V
	H	VIH	2.52	—	3.6	V	VDD=3.6V
Input current (3.3V CMOS interface)	L	IIL3	–10	—	10	µA	VDD=3.6V,VI=0V
	H	IIH3	–10	—	10	µA	VDD=3.6V,VI=3.6V
Input voltage schmitt (5.0V CMOS interface)	–	VT-	0.8	—	1.65	V	VDD=3.3V
	+	VT+	1.4	—	2.7	V	
	Hysteresis	VH	0.3	—	1.2	V	
Input current (5.0V CMOS interface)	L	IIL5	–100	—	10	µA	VDD=3.6V,VI=0V
	H	IIH5	–10	—	10	µA	VDD=3.6V,VI=3.6V
CMOS output voltage	L	VOL	—	—	0.05	V	VDD=3.3V,|IO|=1µA
	H	VOH	3.25	—	—	V	
CMOS output current	L	IOL	2	—	—	mA	VDD=3.3V,VOL=0.4V
	H	IOH	—	—	–2	mA	VDD=3.3V,VOL=2.6V
Output leakage current	L	IOZL	–10	—	10	µA	VDD=3.6V,VO=0V
	H	IOZH	–10	—	10	µA	VDD=3.6V,VO=3.6V
Input pin capacitance		CI	—	7	15	pF	f=1MHz,VDD=0V
Output pin capacitance		CO	—	7	15	pF	
Bi-directional pin capacitance		CIO	—	7	15	pF	
Operating current	3.3V supply	IDD	—	140	—	mA	

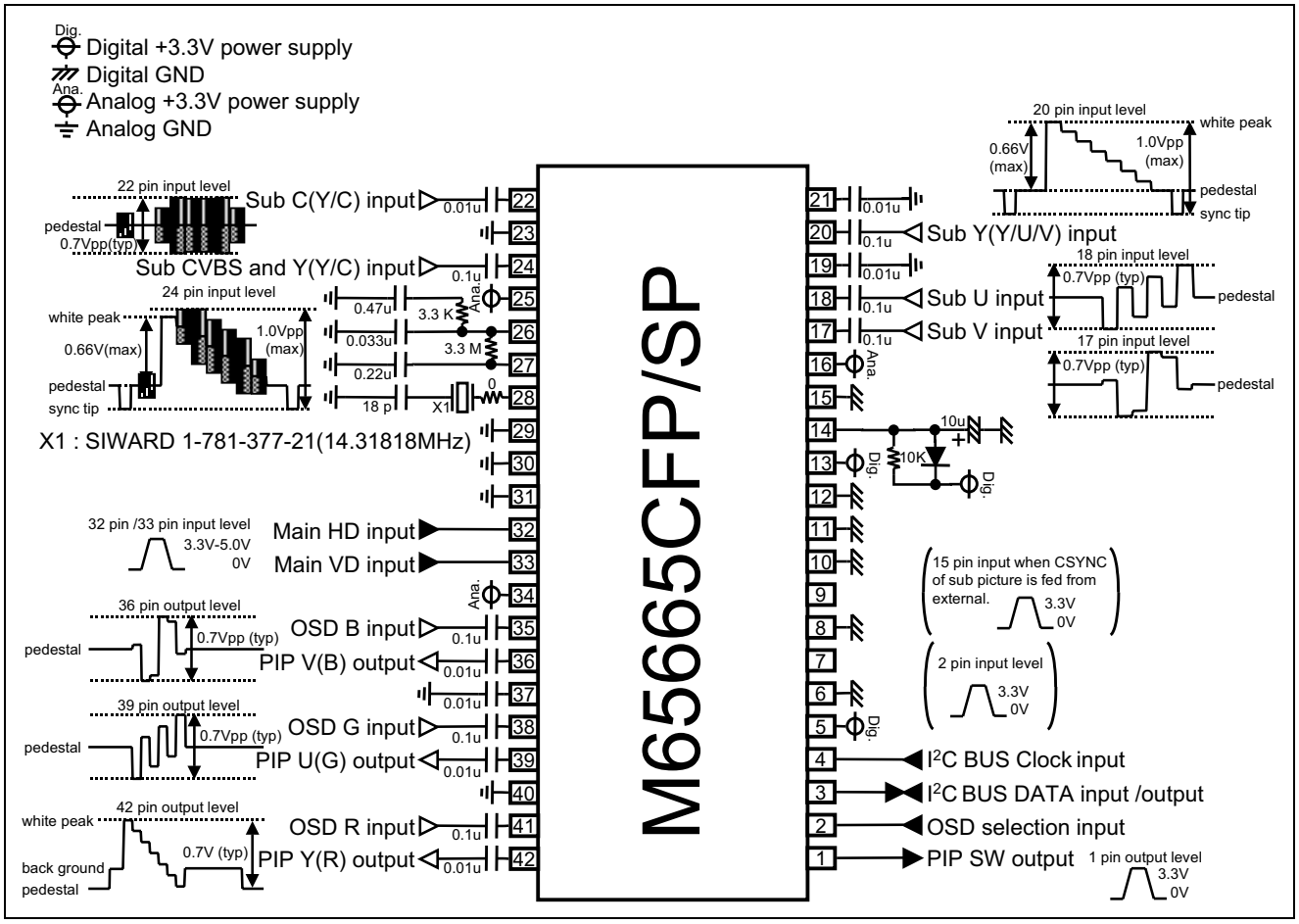
Pin Description

Pin No.	Name	I/O	Function	Remarks
1	SWM	CMOS output	PIP switch output	
2	OSD_SEL	CMOS input	Output OSD select	
3	SDATA	CMOS input/output (5V)*1	IIC SDA input/output	
4	SCLK	CMOS input (5V)*1	IIC SCL input	
5	DVdd	Digital Vdd	VDD for digital part	
6	DVss	Digital Vss	VSS for digital part	
7	BGPS	CMOS output	Test output	
8	SCK	CMOS input	Test input	connect to GND
9	BGPM	CMOS output	Test output	
10	FSC	CMOS input	Test input	connect to GND
11	TEST5	CMOS input	Test input	connect to GND
12	TESTEN	CMOS input	Test input	connect to GND
13	SWMG	CMOS input	PIP switch output enable	connect to VDD
14	RESET	CMOS input	Power on reset input	
15	CSYNCS	CMOS input	Sub picture external c-sync input	
16	AVdd(ADC)	Analog Vdd	Vdd for internal ADC	
17	VIN(ADC)	Analog	Sub picture V input of ADC	
18	UIN(ADC)	Analog	Sub picture U input of ADC	
19	VRB	Analog	Low level reference voltage output of ADC	
20	YIN(ADC)	Analog	Sub picture Y input of ADC	
21	VRT	Analog	High level reference voltage output of ADC	
22	CIN(ADC)	Analog	Sub picture C input of ADC	
23	AVss(ADC)	Analog Vss	VSS for internal ADC	
24	CVBSIN(ADC)	Analog	Sub picture CVBS input of ADC	
25	AVdd(VCXO)	Analog Vdd	Vdd for VCXO	
26	FILTER	Analog	VCXO filter voltage connection	
27	BIAS	Analog	VCXO bias voltage connection	
28	X'tal(NTSC)	Analog	X'tal of NTSC connection	
29	TEST	Analog	TEST	connect to GND
30	TEST	Analog	TEST	connect to GND
31	AVss(VCXO)	Analog Vss	Vss for VCXO	
32	HD	CMOS input (5V)*1	Main picture HD input	
33	VD	CMOS input (5V)*1	Main picture VD input	
34	Vdd(DAC)	Analog Vdd	Vdd for DAC	
35	OSD_BIN	Analog	OSD input of B	
36	V(B)OUT	Analog	Sub picture V or B output	
37	VZ	Analog	Voltage reference output of DAC	
38	OSD_GIN	Analog	OSD input of G	
39	U(G)OUT	Analog	Sub picture U or G output	
40	AVss(DAC)	Analog Vss	Vss for DAC	
41	OSD_RIN	Analog	OSD input of R	
42	Y(R)OUT	Analog	Sub picture Y or R output	

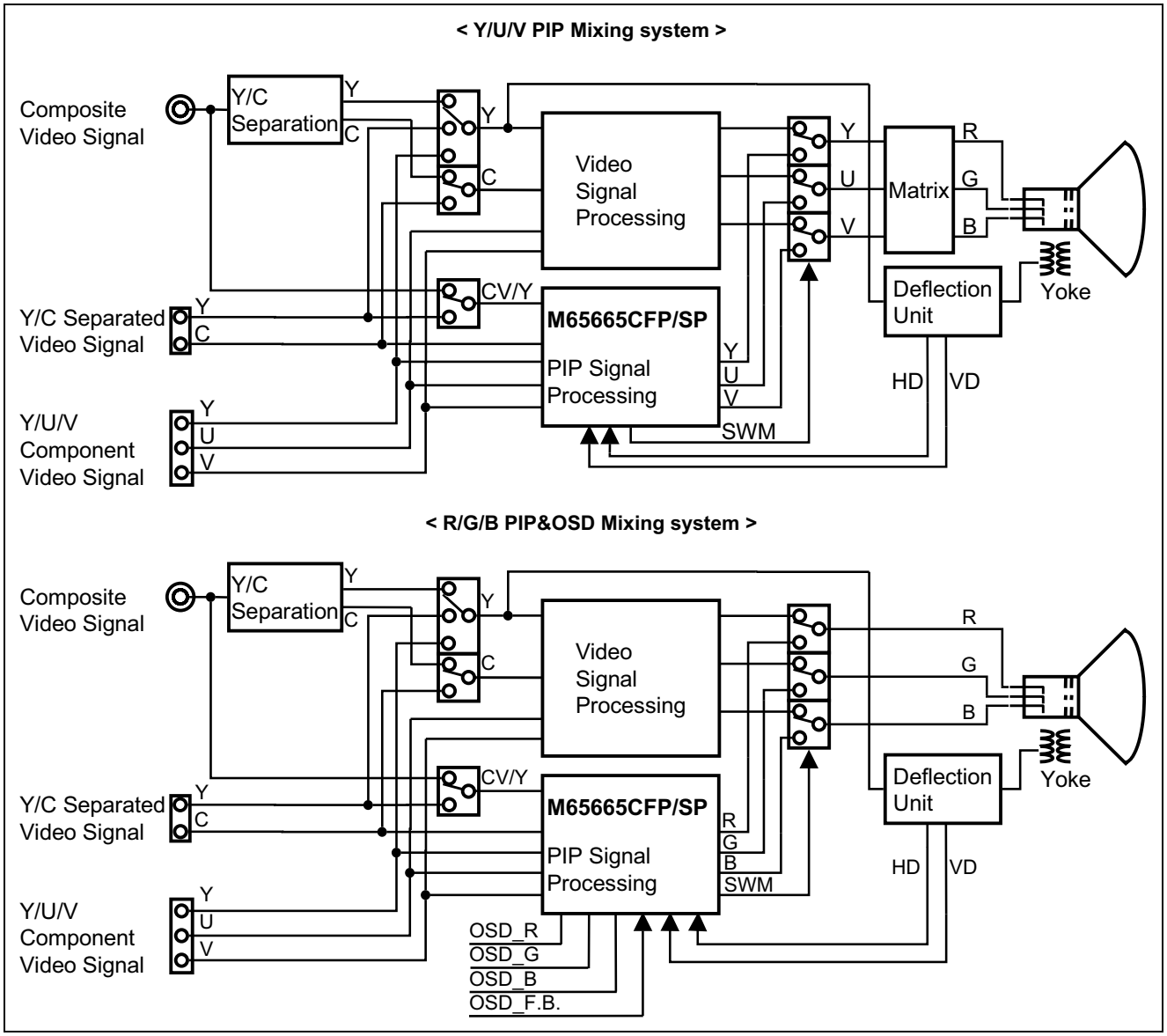
Note : 1. (5V) means 5V I/F tolerant

Basic Application Example

When using any or all of the information contained in this diagrams, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products.



TV System Block Diagram



I²C Register Information

When using any or all of the information contained in this table, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products.

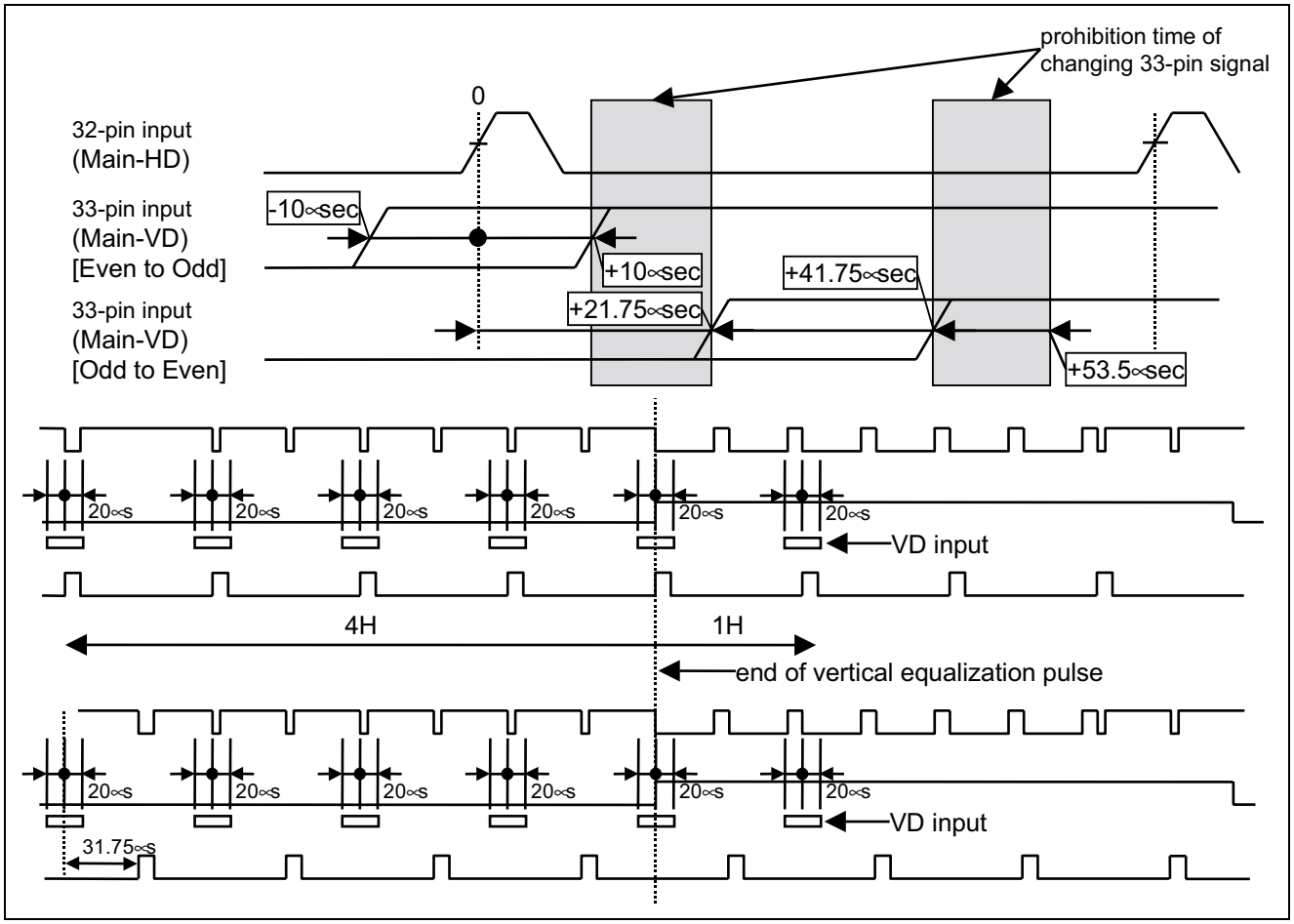
Address	Bit	Symbol	Read/ Write	Reset Value	1/9 Ref. Value	Remarks
00h	<7>	DISP	W/R	0	1h	Sub picture display : [0] off , [1] on
	<6>	SIZE_V	W/R	0	0	Sub picture vertical size : [0] 1/9 , [1] 1/16
	<5>	SIZE_H	W/R	0	0	Sub picture horizontal size : [0] 1/9 , [1] 1/16
	<4>	WEN	W/R	0	1h	Sub picture : [0] Still , [1] Moving
	<3>	BGC	W/R	0	0	Back ground display : [0] off , [1] on
	<2>	BGCS	W/R	0	0	Sub picture mute : [0] off , [1] on
	<1>	FREE_RUN	W/R	0	0	VCXO oscilation : [0] Lock , [1] Free run
	<0>	—	W/R	0	0	For test : 0 set only
01h	<7:0>	VXA<7:0>	W/R	0	20h	Sub picture vertical position
02h	<7:0>	HXA<7:0>	W/R	0	20h	Sub picture horizontal position
03h	<7>	DECODE	W/R	0	0	Sub picture color decoder reset : [1] reset
	<6:0>	CONTRAST<6:0>	W/R	0	32h	Sub picture Y or R DAC output amplitude control
04h	<7>	KILLER	W/R	0	0	Sub picture color killer : [0] enable , [1] disable
	<6:0>	U_DAC<6:0>	W/R	0	32h	Sub picture U or G DAC output amplitude control
05h	<7>	GRC	W/R	0	1h	Frame display : [0] off , [1] on
	<6>	YUVN_RGB_SEL	W/R	0	0	PIP output mode selection : [0] YUV , [1] RGB
	<5:0>	TINT<5:0>	W/R	0	0	Sub picture TINT control
06h	<7:6>	EXT_SC_SEL<1:0>	W/R	0	1h	Sub picture c-sync sep. selection : [0] int. digital , [1] int. auto slice , [2] ext.(18 pin) , [3] int. analog
	<5:4>	DCONT<1:0>	W/R	0	0	Sub picture int. c-sync sep. threshhold setting.
	<3:0>	HT<3:0>	W/R	0	Ah	Sub picture display timing adjust
07h	<7:6>	INPUT_SEL<1:0>	W/R	0	2h	Sub picture input selection : [0] YC , [1] N.A. , [2] CVBS , [3] YUV
	<5:0>	BG_START<5:0>	W/R	0	0Fh	Sub picture Burst Gate Pulse position setting
08h	<7:4>	ADJ<3:0>	W/R	0	4h	Main/Sub switch delay control
	<3:0>	YDL<3:0>	W/R	0	Ah	Sub picture Y/C delay adjust
09h	<7:5>	BGBY<2:0>	W/R	0	0	Back ground U level setting
	<4:0>	Y_OFFSET<4:0>	W/R	0	0Fh	Sub picture Y bright control
0Ah	<7>	VCHIP ONLY	W/R	0	1h	V-chip decode mode : [0] off , [1] on
	<6:4>	BGRY<2:0>	W/R	0	0	Back ground V level setting
	<3:0>	BGY<3:0>	W/R	0	6h	Back ground Y level setting
0Bh	<7:4>	PEDESTV<3:0>	W/R	0	0	Sub picture V pedestal level (2's comp)
	<3:0>	PEDESTU<3:0>	W/R	0	0	Sub picture U pedestal level (2's comp)

Address	Bit	Symbol	Read/ Write	Reset Value	1/9 Ref. Value	Remarks
0Ch	<7>	UV_FILTER_OFF	W/R	0	1h	Sub picture U,V output filter [0] on , [1] off
	<6>	SET_ACC	W/R	0	0	Address 0Dh,0Eh setting mode : [0] fixed value, [1] released to MCU
	<5:4>	—	W/R	0	0	For test : 0 set only
	<3>	SET_SIZE	W/R	0	0	Address 11h<6:0>,12h-14h setting mode : [0] fixed value, [1] released to MCU
	<2>	SET_VCHIP	W/R	0	0	Address 15h-17h setting mode : [0] fixed value, [1] released to MCU
	<1:0>	SYNC_DELAY<1:0>	W/R	0	0	Sub picture sync. delay control
0Dh	<7:4>	YUV_COL<3:0>	W/R	0	0	Sub picture color control parameter when YUV input
	<3>	C_GAIN_SEL	W/R	0	0	Sub picture chroma : [0] X1 , [1] X2
	<2>	WDOF_KILLER_ON	W/R	0	0	Sub picture killer on when burst PLL is unlock : [0] off , [1] on
	<1>	SET_YUV	W/R	0	0	For test : 0 set only
	<0>	CVF	W/R	0	0	Internal chroma comb filter : [0] on , [1] off
0Eh	<7>	BITSEL	W/R	0	0	Sub picture Y clamp time constant : [0] X2 , [1] X1
	<6>	AFCBITSEL	W/R	0	0	Sub picture AFC time constant : [0] X2 , [1] X1
	<5:0>	ACC_LEVEL<5:0>	W/R	0	15h	Sub picture color decoder amplitude
0Fh	<7>	—	W/R	0	0	For test : 0 set only
	<6>	—	W/R	0	0	For test : 0 set only
	<5>	—	W/R	0	0	For test
	<4>	INV_RFF	W/R	0	0	Invert main picture field definition : [0] normal , [1] invert
	<3>	INV_WFF	W/R	0	0	Invert sub picture field definition : [0] normal , [1] invert
	<2>	—	W/R	0	0	For test : 0 set only
	<1>	RFF_FIX	W/R	0	0	Main picture field fix : [0] not fix , [1] fix
	<0>	—	W/R	0	1h	For test

Address	Bit	Symbol	Read/ Write	Reset Value	1/9 Ref. Value	Remarks
10h	<7:6>	NO_BST_LVL<1:0>	W/R	0	0	For test
	<5:4>	BW_DET_LVL<1:0>	W/R	0	0	BW det. threshold setting : [0] off , [1] 16mV , [2] 32mV , [3] 64mV
	<3:0>	—	W/R	0	0	For test
11h	<7>	—	W/R	0	0	For test : 0 set only
	<6:0>	HYA<6:0>	W/R	0	37h	Sub picture horizontal display pixel
12h	<7:0>	VYA<7:0>	W/R	0	44h	Sub picture vertical display line number
13h	<7:2>	HX<5:0>	W/R	0	1Eh	Sub picture horizontal capture position (coarse)
	<1:0>	HP<1:0>	W/R	0	0	Sub picture horizontal capture position (fine)
14h	<7:6>	MVC<1:0>	W/R	0	0	Sub picture c-sync input mask period : [0] 48usec , [1] 44usec , [2] 53usec , [3] off
	<5:0>	VXS<5:0>	W/R	0	29h	Sub picture sample start line
15h	<7>	—	W/R	0	0	For test : 0 set only
	<6>	PLUS	W/R	0	0	For test : 0 set only
	<5>	—	W/R	0	0	For test : 0 set only
	<4:0>	LINE_NUM<4:0>	W/R	0	11h	Data slicer line selection
16h	<7:0>	STB_DLY<7:0>	W/R	0	40h	Data slicer start bit detection parameter
17h	<7:0>	L_LEVEL<7:0>	W/R	0	82h	Data slicer data slice parameter
18h	<7>	EDGE_ON	W/R	0	1h	Frame data independent control : [0] disable , [1] enable
	<6:4>	BGBY_EDGE<2:0>	W/R	0	0	Frame data independent B-Y data setting
	<3:0>	BGY_EDGE<3:0>	W/R	0	Ch	Frame data independent Y data setting
19h	<7:5>	BGRY_EDGE<2:0>	W/R	0	0	Frame data independent R-Y data setting
	<4>	HPFOFF	W/R	0	0	Sub picture Y output HPF : [0] on , [1] off
	<3:0>	FREE_RUN_ADJ<3:0>	W/R	0	0	Frequency adjustment control when free run mode (2's comp)
1Ah	<7:0>	—	W/R	0	0	For test
1Bh	<7:6>	EXPORT<1:0>	W/R	0	0	Ext. port (7 pin) : [0] "0" output , [1] "1" output , [2 or 3] Sub BGP
	<5>	INV_UV	W/R	0	0	Invert U,V output value : [0] normal , [1] invert
	<4>	AFC_OFF	W/R	0	0	Sub picture AFC : [0] on , [1] off
	<3:0>	—	W/R	0	0	For test
1Ch	<7>	PINOE	W/R	0	0	For test
	<6:0>	V_DAC<6:0>	W/R	0	32h	Sub picture V or B DAC output amplitude control
1Dh	<7:0>	PINOE<7:0>	W/R	0	E6h	For test
1Eh	<7:0>	—	W/R	0	0	For test : 0 set only

Address	Bit	Symbol	Read/ Write	Reset Value	1/9 Ref. Value	Remarks
1Fh	<7:6>	—	R			Test use (Read only)
	<5>	—	R			Test use (Read only)
	<4>	SUB_UNLOCK	R			VCXO is : [0] Lock , [1] Unlock (Read only)
	<3>	—	R			Test use (Read only)
	<2>	RDOF	R			Main picture V sync is [0] present , [1] not present (Read only)
	<1>	SUB_BW	R			Sub picture burst is : [0] not present , [1] present (Read only)
	<0>	WDOF	R			Sub picture V sync is [0] present , [1] not present (Read only)
20h	<7>	KILLERSTATUS	R			Sub picture killer status : [0] not active , [1] active (Read only)
	<6>	—	R			Test use (Read only)
	<5>	WDOF	R			Sub picture V sync is [0] present , [1] not present (Read only)
	<4>	EDS_ACK2	R			EDS data flag of even field : [0] no EDS , [1] EDS (Read only)
	<3>	EDS_ACK1	R			EDS data flag of odd field : [0] no EDS , [1] EDS (Read only)
	<2>	SIGNAL_OK	R			Test use (Read only)
	<1>	READ_REQB	R			Read request of even field : [0] no , [1] requesting (Read only)
	<0>	READ_REQA	R			Read request of odd field : [0] no , [1] requesting (Read only)
21h	<7:0>	PDB<15:8>	R			Even field Sliced data upper 8bit (Read only)
22h	<7:0>	PDB<7:0>	R			Even field Sliced data lower 8bit (Read only)
23h	<7:0>	PDA<15:8>	R			Odd field Sliced data upper 8bit (Read only)
24h	<7:0>	PDA<7:0>	R			Odd field Sliced data lower 8bit (Read only)

The relation of input signal 32-pin (Main-HD) and 33-pin (Main-VD) is shown below



Driving Method and Operating Specification for Serial Interface Data

(1) Serial data transmission completion and start

A low-to-high transition of the DATA (serial data) line while the CLK (serial clock) is high, that completes the serial transmission and makes the bus free. A high-to-low transition of the DATA line while the CLK is high, that starts the serial transmission and waits for the following CLK and DATA inputs.

(2) Serial data transmission

The data are transmitted in the most significant bit (MSB) first by one-byte unit on the DATA line successively. One-byte data transmission is completed by 9 clock cycles, the former 8 cycles are for address/data and the latter one is for acknowledge detection. (In writing state, SDATA outputs ‘L' under these two conditions ; 1) the coincidence of two address data for the address data transmission, 2) the completion of 8-bit setting data transfer. In reading state, SDATA outputs ‘L' with the address coincidence and SDATA becomes high-impedance for detecting acknowledge input from the master (micro processor) after sending 8-bit setting data.) For address/data transmission, DATA must change while CLK is 'L'. (The data change while CLK is 'H' or the simultaneous change of CLK and DATA, that will be a false operation because of undistinguished condition from the completion / start of serial data transfer). After the beginning of serial data transmission, the total number of data bytes that can be transferred are not limited.

(3) The byte format of data transmission (The sequence of data transmission)

a. The byte format during data writing to M65665CFP/SP are shown as follows.

In right after the forming of serial data transmitting state, the slave address 24h (00100100b) is transferred. Afterwards, the internal register address (1 byte) and writing data (by 1 byte unit) are transferred successively. Several bytes of

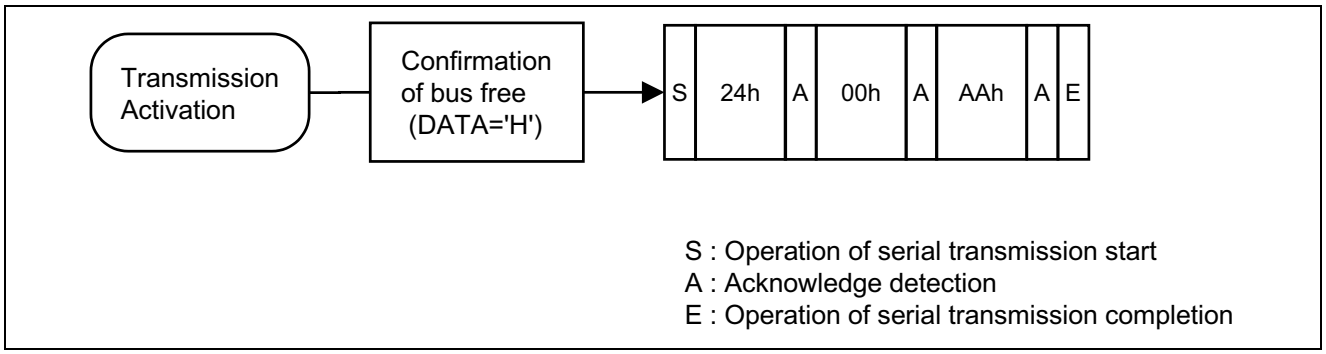
writing data can be handled in the one transmission. In this operation, the setting data are written into the address register whose address is increased one in initially transferred internal register address.

b. The byte format during data reading from M65665CFP/SP are shown as follows.

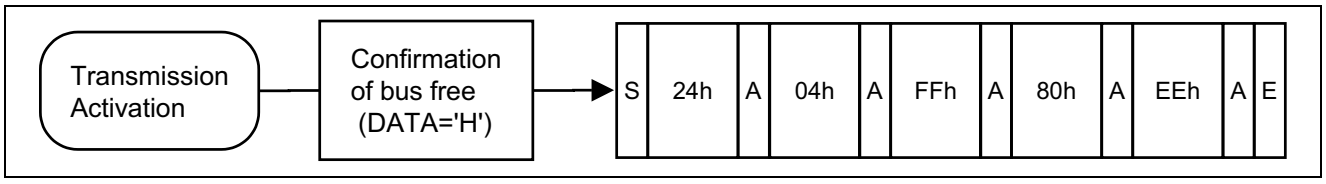
Before data reading from M65665CFP/SP, whose internal address need to be set by the data reading/transmitting. After the data reading/transmitting, the operation of "serial data transmission completion and start" (described in (1)) is necessary. Continuously, the slave address 25h (00100101b) is sent, and then the read out data are available on SDATA as 'L'/'high-impedance' pattern. Several bytes of reading data can be handled in the one transmission, too. In this operation, the setting data also are written into the address register whose address is increased one in initially transferred internal register address.

The examples of serial byte transmission format

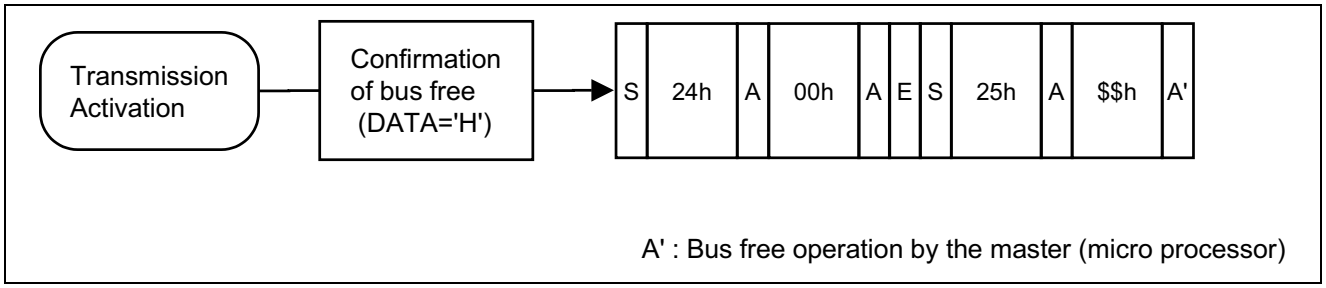
(1) The writing operation of the setting data (AAh) into M65665CFP/SP internal address of 00h



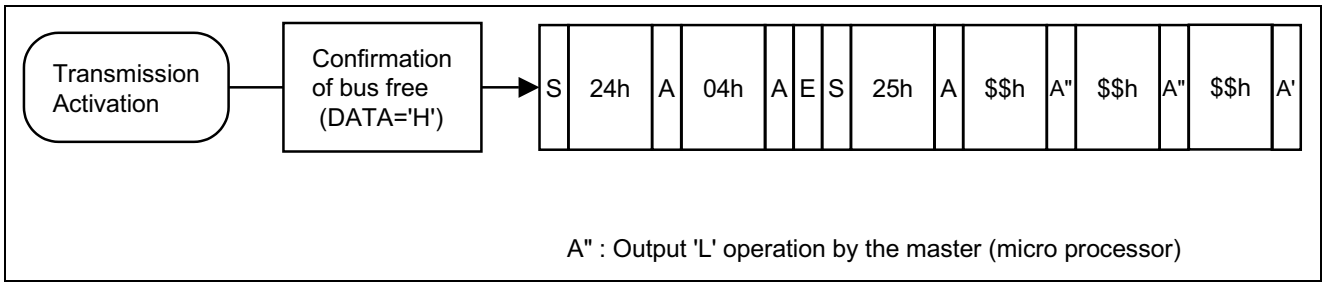
(2) The writing operation of the setting data (FFh, 80h, EEh) into M65665CFP/SP internal address of 04h to 06h



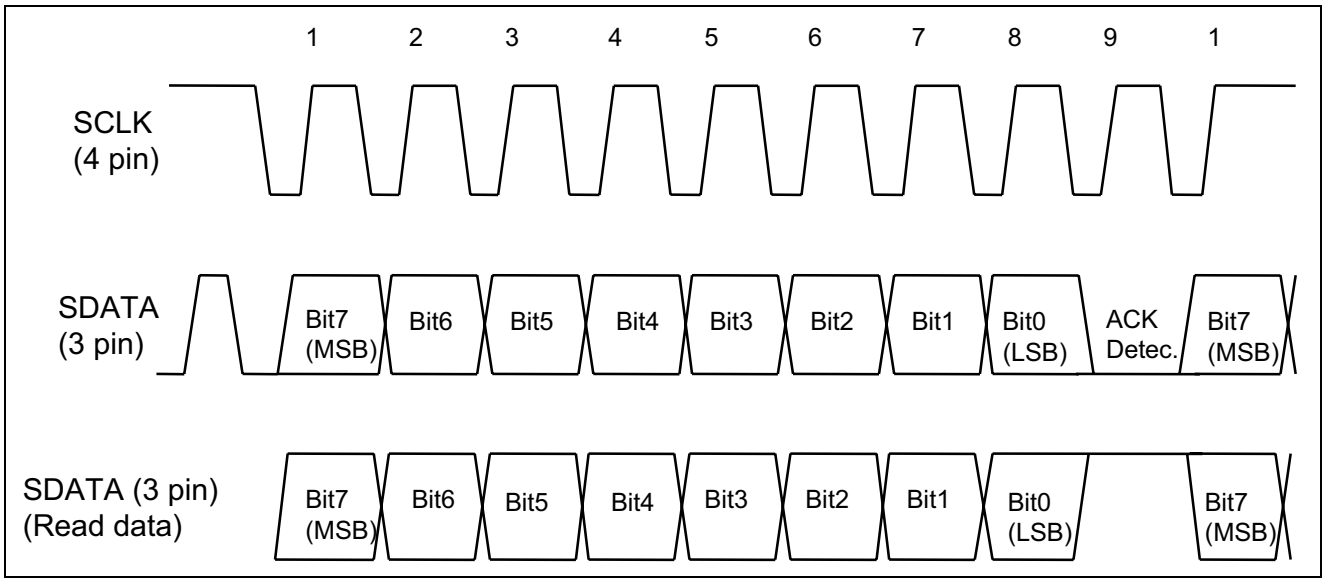
(3) The reading operation of the setting data from M65665CFP/SP internal address of 00h



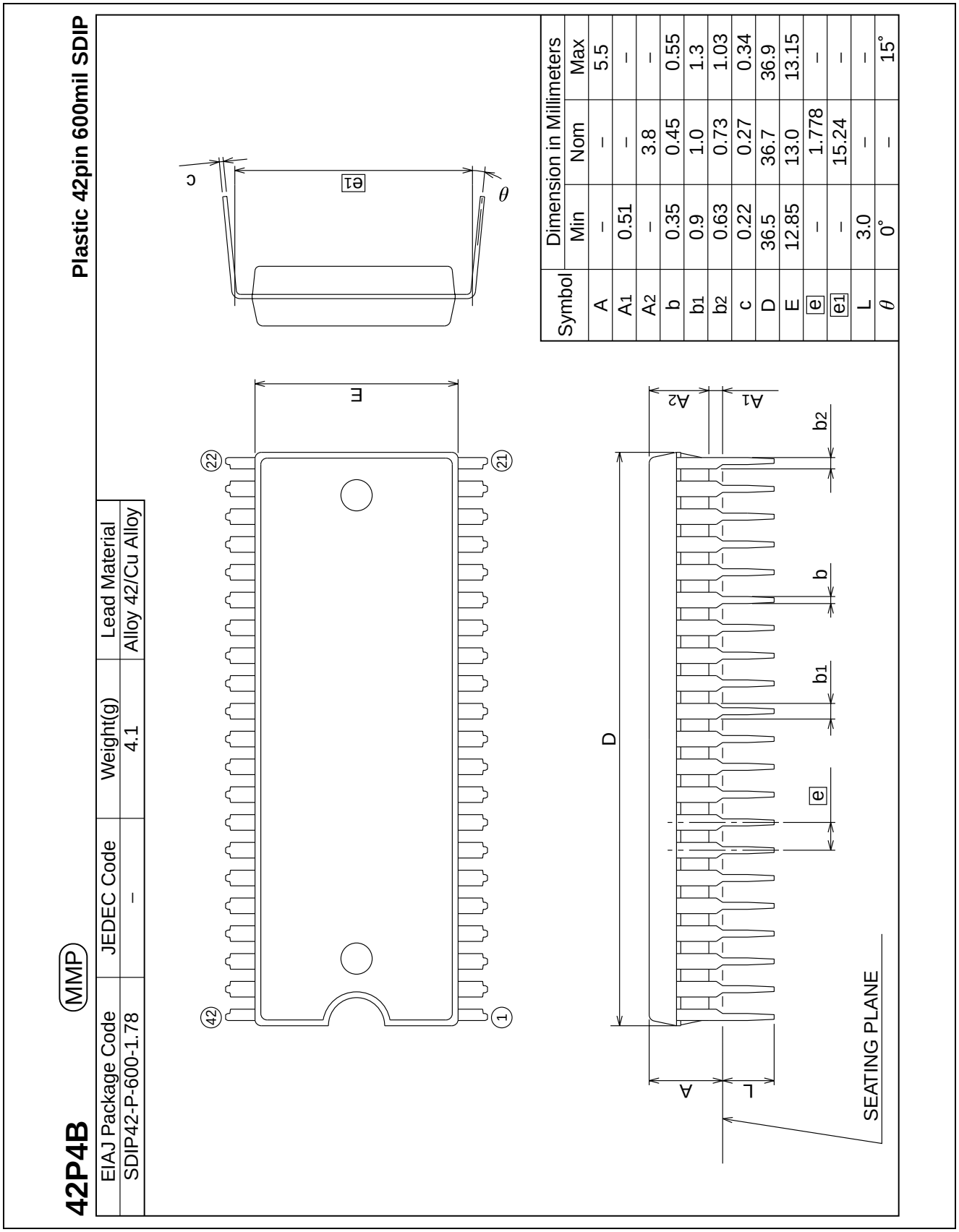
(4) The reading operation of the setting data from M65665CFP/SP internal address of 04h to 06h.

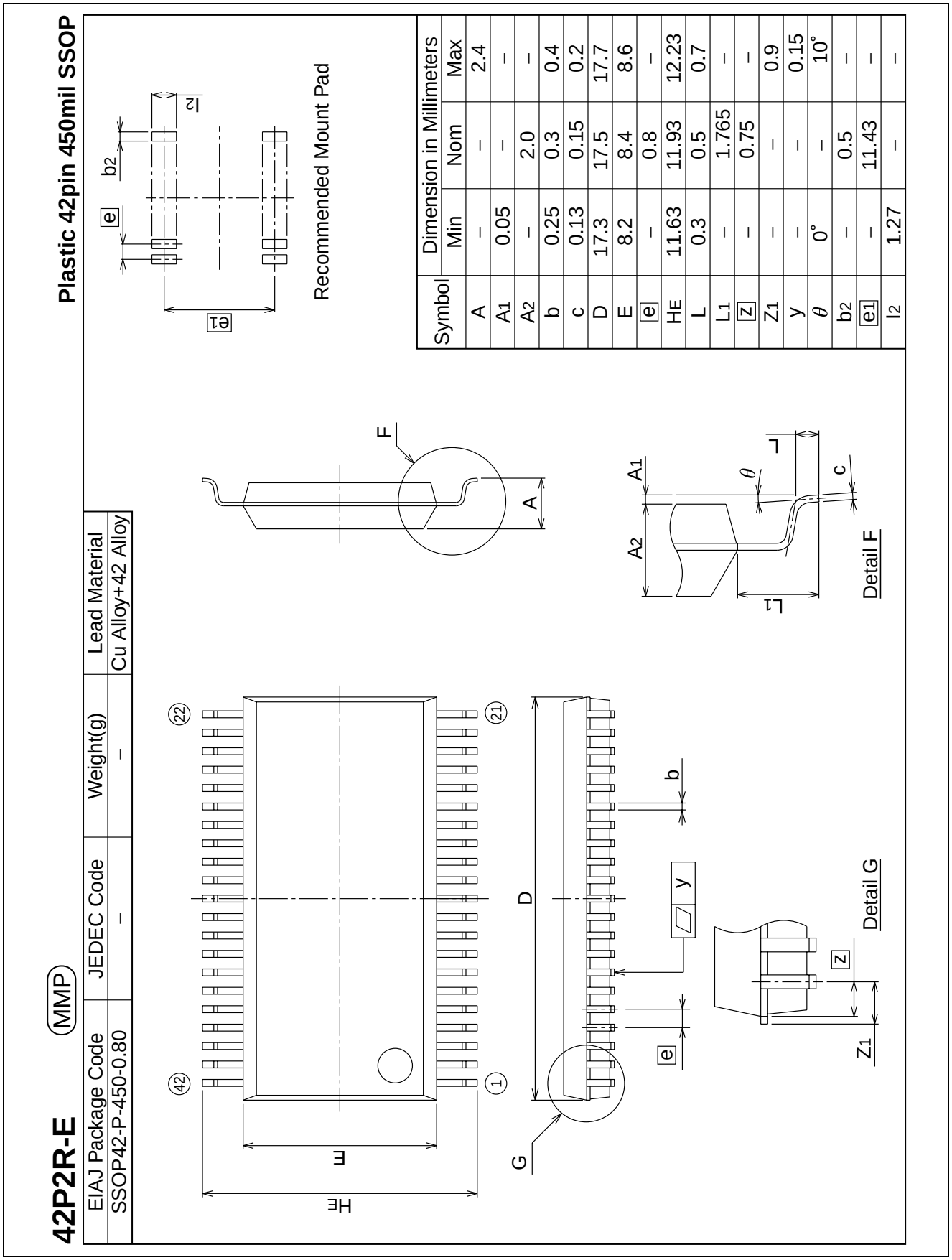


Timing Diagram



Package Dimensions




42P2R-E
MMP
Plastic 42pin 450mil SSOP
EIAJ Package Code
SSOP42-P-450-0.80
JEDEC Code
–
Weight(g)
–
Lead Material
Cu Alloy+42 Alloy
Recommended Mount Pad
Dimension in Millimeters
Symbol
Min
Nom
Max
A – – 2.4
A1 0.05 – –
A2 – 2.0 –
b 0.25 0.3 0.4
c 0.13 0.15 0.2
D 17.3 17.5 17.7
E 8.2 8.4 8.6
e – 0.8 –
HE 11.63 11.93 12.23
L 0.3 0.5 0.7
L1 – 1.765 –
z – 0.75 –
Z1 – – 0.9
y – – 0.15
θ 0° – 10°
b2 – 0.5 –
e1 – 11.43 –
l2 1.27 – –
HE
E
D
G
F
A
A1
A2
θ
L
c
L1
Detail F
b
y
e
z
Z1
Detail G

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Colophon 1.0