When the halt status is released by a reset, the status in effect before entering the halt status (including built-in RAM) is held. The RAM contents may not be held, however, if the HALT instruction is executed within the built-in RAM.

WDMOD (FFD2H)

	7	6	5	4	3	2	1	0
bit Symbol	WDTE	WDTP1	WDTP0	WARM	HALTM1	HALTM0	EXF	DRIVE
Read/Write	R/W	R/W		R/W	R/W		R	R/W
Resetting Value	1	0	0	0	0	0	Undefined	0
Function	1: Enable	WDT Detecting time 00: 2^{14}/fc 01: 2^{16}/fc 10: 2^{18}/fc 11: 2^{20}/fc		Warming up time 0: 2^{14}/fc 1: 2^{16}/fc	Standby mode 00: RUN mode 01: STOP mode 10: IDLE1 mode 11: IDLE2 mode		Invert each time EXX instruction is executed	1: to drive pin in STOP mode.

See "3.10 Watchdog Timer"

See "3.4.4 STOP mode"

Exchange flag
See "3.1.2 Registers"

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Figure 3.4 (1) HALT Mode Set Register

3.4.1 RUN Mode

Figure 3.4 (2) shows the timing for releasing the HALT state by interrupts in the RUN/IDLE 2 mode.

In the RUN mode, the system clock in the MCU continues to operate even after a HALT instruction is executed. Only the CPU stops executing the instruction. Until the HALT state is released, the CPU repeats dummy cycles. In the HALT state, an interrupt request is sampled with the rising edge of the "CLK" signal.

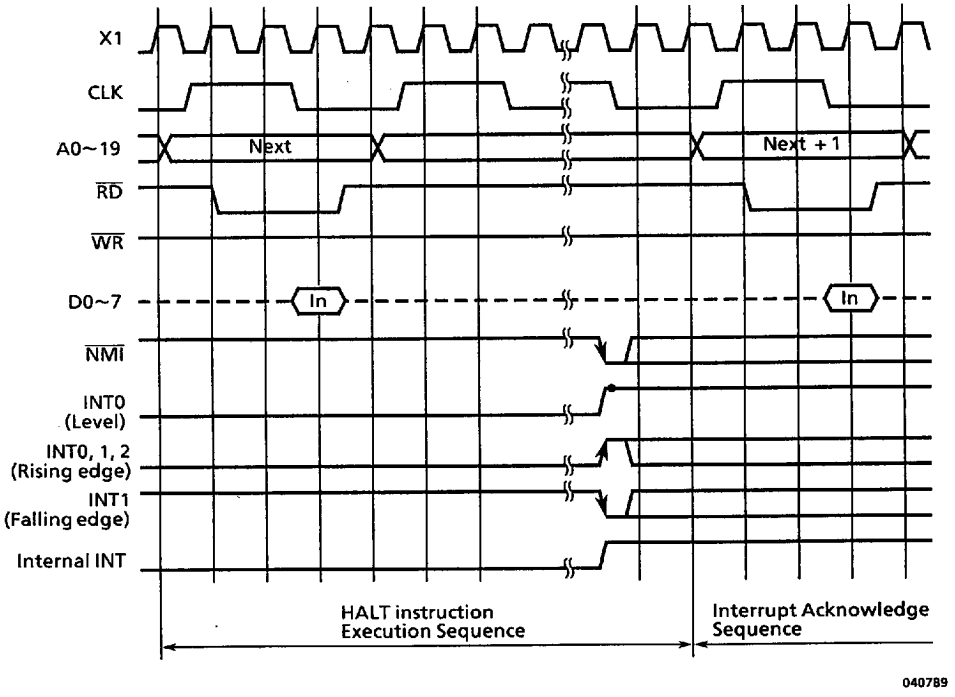

Figure 3.4 (2) Timing Chart for Releasing the HALT State by Interrupts in RUN/IDLE 2 Modes

3.4.2 IDLE 1 Mode

Figure 3.4 (3) illustrates the timing for releasing the HALT state by interrupts in the IDLE 1 mode.

In the IDLE 1 mode, only the internal oscillator and the watchdog timer operate. The system clock in the MCU stops, and the CLK signal is fixed at the "1" level.

In the HALT state, an interrupt request is sampled asynchronously with the system clock, however the HALT release (restart of operation) is performed synchronously with it.

Note : An interrupt requested by the watchdog timer is prohibited through the HALT period in this mode.

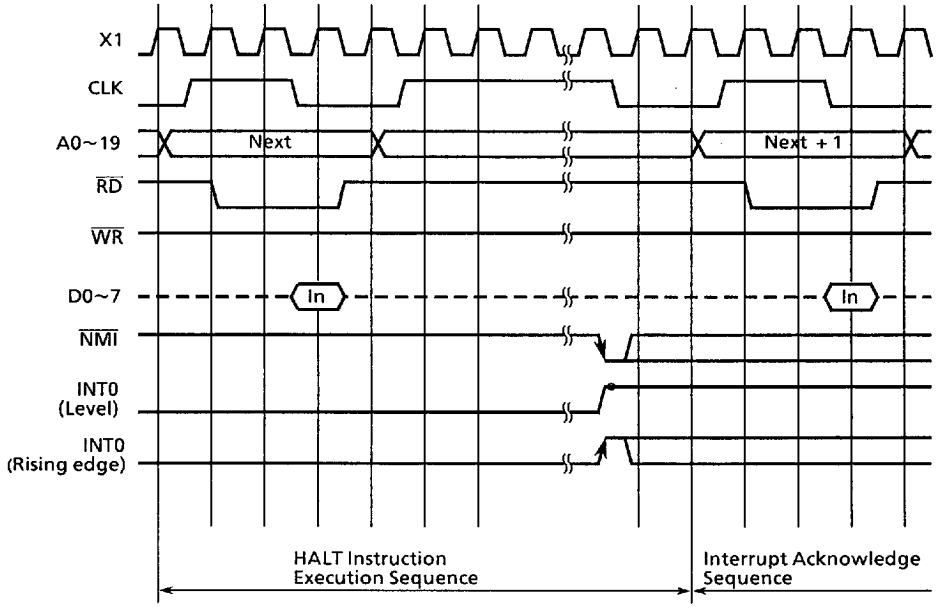

Figure 3.4 (3) Timing Chart of HALT Released by Interrupts in IDLE1 Mode