

# TC9090AN, TC9090AF

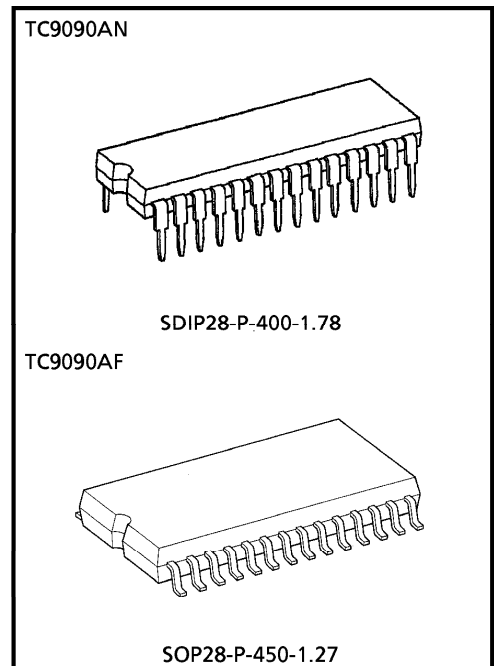
## MULTICOLOR SYSTEM VERSION

## 3-LINE DIGITAL Y / C SEPARATION IC

The TC9090AN and TC9090AF separate luminance (Y) and chrominance (C) signals from a multicolor system composite video signal. It employs the Toshiba logical comb filter to realize high performance Y/C separation at low cost.

### FEATURES

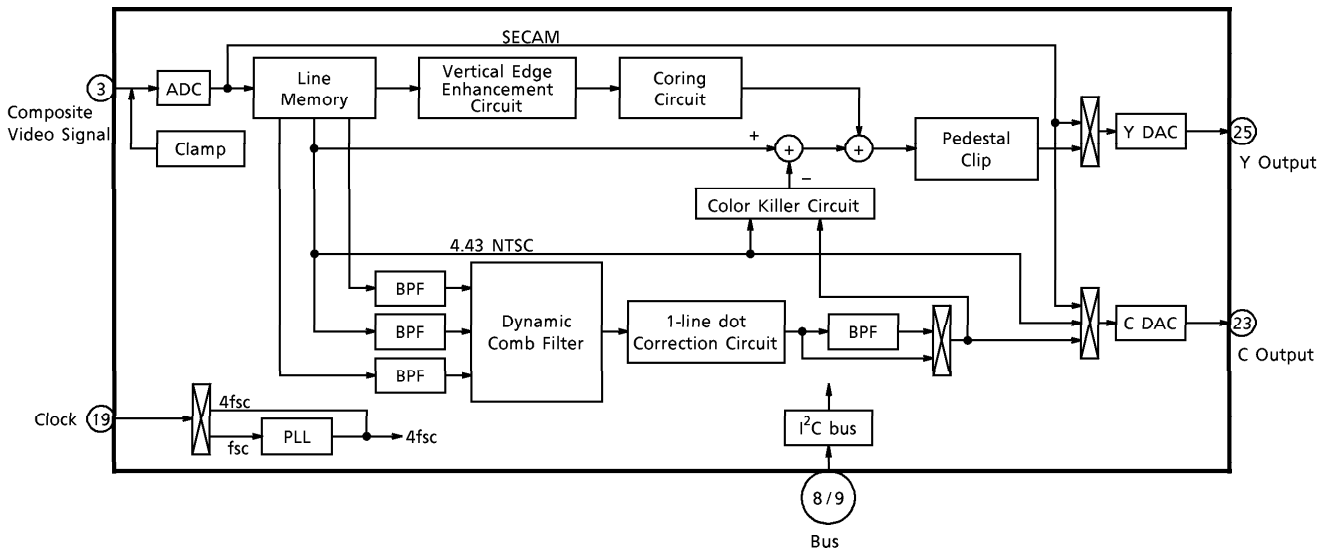
- TV systems : NTSC, PAL, N-PAL, M-PAL, 4.43NTSC
- PLL 4× multiplication circuit
- Sync tip clamping circuit
- Internal 8bit A/D converter
- Internal 8bit D/A converters (2ch)
- 4H line memories
- Dynamic comb filter
- 1-line dot interference correction circuit
- Vertical edge enhancement circuit
- Color killer mode (Y/C separation OFF)
- Chroma output band width selectable
- I<sup>2</sup>C bus control
- SDIP28/SOP28 package
- 5V single power supply



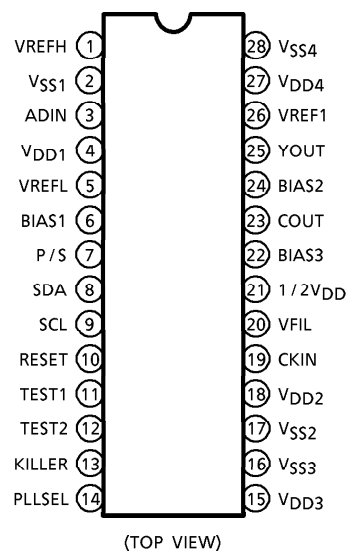
### Weight

|                   |               |
|-------------------|---------------|
| SDIP28-P-400-1.78 | : 1.7g (Typ.) |
| SOP28-P-450-1.27  | : 0.8g (Typ.) |

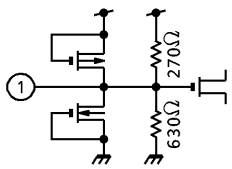
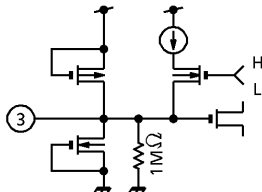
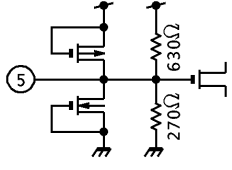
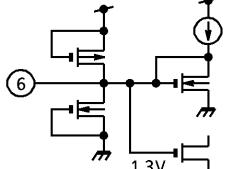
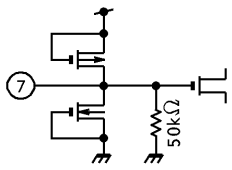
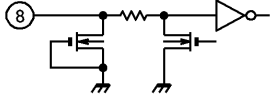
BLOCK DIAGRAM

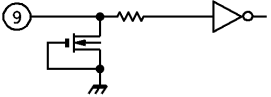
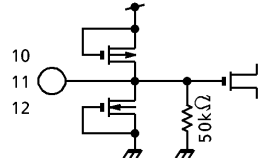
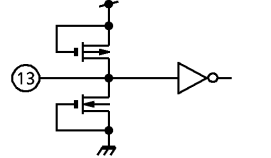
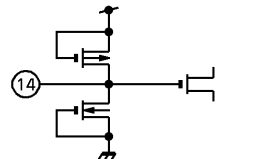
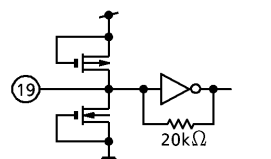
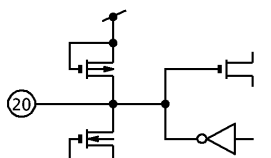


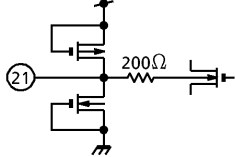
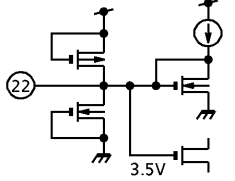
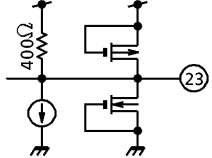
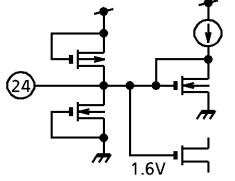
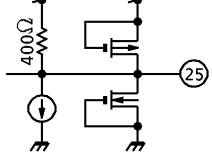
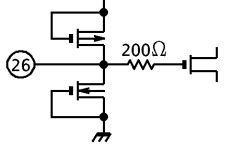
TERMINAL CONNECTION DIAGRAM



## TERMINAL FUNCTION

| PIN No. | PIN NAME    | FUNCTION                                                                                                                                                                      |                                 | I / O | INTERFACE CIRCUIT                                                                     |
|---------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------|-------|---------------------------------------------------------------------------------------|
| 1       | VREFH       | ADC bias higher limit reference voltage. This defaults internally to approximately 3.5V, so this pin should normally be connected to ground through a 0.01 $\mu$ F capacitor. |                                 | I     |    |
| 2       | VSS1        | ADC ground.                                                                                                                                                                   |                                 | —     | —                                                                                     |
| 3       | ADIN        | Composite video signal input.                                                                                                                                                 |                                 | I     |    |
| 4       | VDD1        | ADC Power supply (+ 5V).                                                                                                                                                      |                                 | —     | —                                                                                     |
| 5       | VREFL       | ADC bias lower limit reference voltage. This defaults internally to approximately 1.5V, so this pin should normally be connected to ground through a 0.01 $\mu$ F capacitor.  |                                 | —     |   |
| 6       | BIAS1       | ADC bias voltage. This defaults internally to approximately 1.3V, so this pin should normally be connected to ground through a 0.01 $\mu$ F capacitor.                        |                                 | —     |  |
| 7       | P/S         | Control mode select.<br>L : I <sup>2</sup> C bus control<br>H : Pin control                                                                                                   |                                 | I     |  |
| 8       | SDA (TVSW1) | I <sup>2</sup> C bus                                                                                                                                                          | Data input, acknowledge output. | I / O |  |
|         |             | Pin                                                                                                                                                                           | TV system select.               | I     |                                                                                       |

| PIN No. | PIN NAME      | FUNCTION                                                                                                                |                                                      | I / O | INTERFACE CIRCUIT                                                                     |
|---------|---------------|-------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------|-------|---------------------------------------------------------------------------------------|
| 9       | SCL (TVSW2)   | I <sup>2</sup> C bus                                                                                                    | Clock.                                               | I     |    |
|         |               | Pin                                                                                                                     | TV system select.                                    | I     |                                                                                       |
| 10      | RESET (TVSW3) | I <sup>2</sup> C bus                                                                                                    | Data reset.                                          | I     |    |
|         |               | Pin                                                                                                                     | TV system select.                                    | I     |                                                                                       |
| 11      | TEST1 (VENH0) | I <sup>2</sup> C bus                                                                                                    | Test terminal. Normally connected to digital ground. | —     |                                                                                       |
|         |               | Pin                                                                                                                     | TV system select.                                    | I     |                                                                                       |
| 12      | TEST2 (VENH1) | I <sup>2</sup> C bus                                                                                                    | Test terminal. Normally connected to digital ground. | —     |                                                                                       |
|         |               | Pin                                                                                                                     | Vertical edge enhancement level select.              | I     |                                                                                       |
| 13      | KILLER        | Color killer mode select.<br>L : Color<br>H : Black and white                                                           |                                                      | I     |   |
| 14      | PLLSEL        | PLL circuit select. (Switches input clock frequency.)<br>L : PLL ON, fsc input<br>H : PLL OFF, 4fsc input               |                                                      | I     |  |
| 15      | VDD3          | Power supply for digital components (+5V).                                                                              |                                                      | —     | —                                                                                     |
| 16      | VSS3          | Ground for digital components.                                                                                          |                                                      | —     | —                                                                                     |
| 17      | VSS2          | PLL ground.                                                                                                             |                                                      | —     | —                                                                                     |
| 18      | VDD2          | PLL power supply (+5V).                                                                                                 |                                                      | —     | —                                                                                     |
| 19      | CKIN          | Clock input. After applying a capacitor for DC cut, input a color-burst-synchronized fsc/4fsc clock signal to this pin. |                                                      | I     |  |
| 20      | VFIL          | Connect a VCO filter to this pin.                                                                                       |                                                      | —     |  |

| PIN No. | PIN NAME           | FUNCTION                                                                                                                       | I / O | INTERFACE CIRCUIT                                                                     |
|---------|--------------------|--------------------------------------------------------------------------------------------------------------------------------|-------|---------------------------------------------------------------------------------------|
| 21      | 1/2V <sub>DD</sub> | Bias for line memory. This pin requires 2.5V external bias.                                                                    | I     |    |
| 22      | BIAS3              | Bias for DAC. This defaults internally to 3.5V, so this pin should normally be connected to ground through a 0.01μF capacitor. | —     |    |
| 23      | COUT               | Chrominance signal output.                                                                                                     | O     |   |
| 24      | BIAS2              | Bias for DAC. This defaults internally to 1.6V, so this pin should normally be connected to ground through a 0.01μF capacitor. | I     |  |
| 25      | YOUT               | Luminance signal output.                                                                                                       | O     |  |
| 26      | VREF1              | DAC bias lower-limit reference voltage for. This pin requires 3.0V external bias.                                              | —     |  |
| 27      | V <sub>DD4</sub>   | DAC power supply (+5V).                                                                                                        | —     | —                                                                                     |
| 28      | V <sub>SS4</sub>   | DAC ground.                                                                                                                    | —     | —                                                                                     |

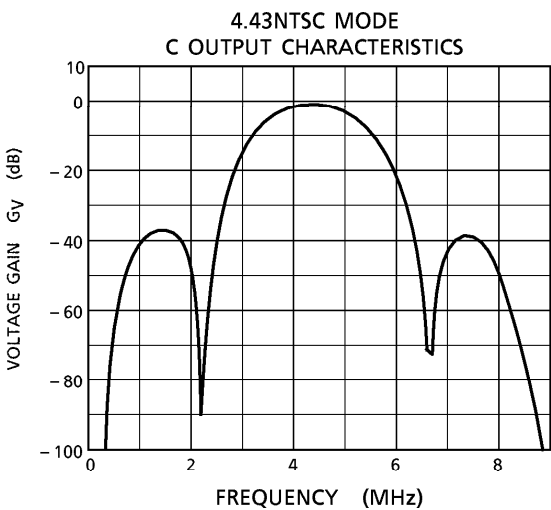
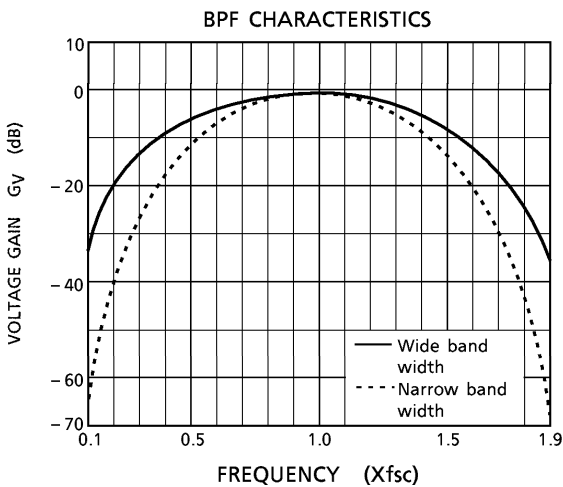
FUNCTION BLOCK DESCRIPTIONS

- 1. Input clamp (CLAMP)  
This block performs sync tip clamping of the composite video signal. It provides a feedback signal for clamping A/D-converted minimum data at Y/C separation to the internal DC bias level.
- 2. A/D converter (ADC)  
This block comprises a high-speed series-parallel 8-bit A/D converter that accepts an input video signal of 1.5V<sub>p-p</sub> (from sync level to 100% white level).
- 3. Line memory  
This block consists of DRAM resident line memory for 1H delay. There are four pairs. The line memories are combined to produce a 3-line composite video signal for each TV system type.

1H delay of the line memory

| TV SYSTEM     | 3.58NTSC | PAL   | N-PAL | M-PAL | 4.43NTSC |
|---------------|----------|-------|-------|-------|----------|
| Delay (clock) | 910      | 1,135 | 917   | 909   | —        |

- 4. Band-pass filter (BPF)  
In this block, with fsc as the center frequency of the BPF, the chrominance signal is extracted from the line-memory-delayed composite video signal. The same logic is used for NTSC, PAL, M-PAL and N-PAL input signals, but the characteristics differ since each TV system uses a different fsc and system clock. Since the BPF for the chrominance signal output can be controlled (ON or OFF), the chrominance output can therefore be switched between a narrow band width and a wide band width. This can be controlled by the I<sup>2</sup>C bus only in I<sup>2</sup>C bus control mode. In pin control mode, the chrominance output is set to a fixed wide band width. Separate BPF logic is used for the 4.43NTSC system type.



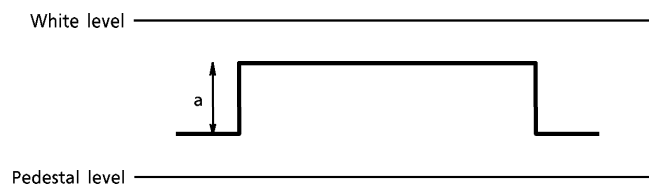
### 5. Dynamic comb filter (DCF)

This block comprises a band-pass filter that extracts the vertical component of the chrominance signal. Using Toshiba original logic, a correlation of the three lines is sought for. The absence of correlation is taken as an indication of a luminance signal, at which time chrominance signal output is suppressed.

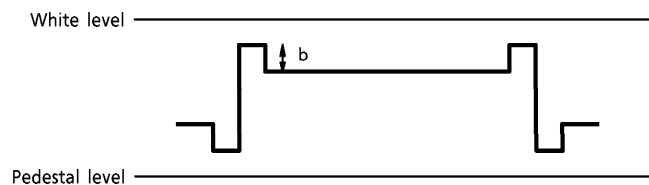
### 6. Vertical edge enhancement circuit (VENH)

This block enhances the uncorrelated components among the three lines of the luminance signal following coring. The luminance signal, obtained by subtracting the chrominance signal from the composite video signal, is added to the vertical edge enhancement component and output through the D/A converter. However, this output signal is limited to the pedestal level (fixed internally) by the pedestal clipping circuit (except for the sync tip level). Eight levels of enhancement (0dB to 1.94dB) can be selected by I<sup>2</sup>C bus control and four levels of enhancement (0dB to 1.49dB) can be selected by pin control. This block can be used with any of the TV system types except SECAM.

#### (i) Input signal with edge component

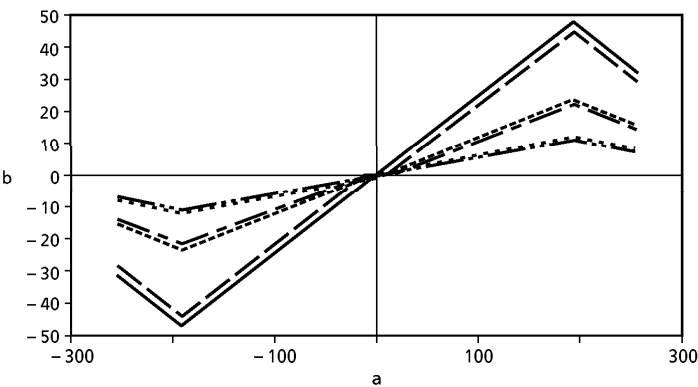


#### (ii) Output signal

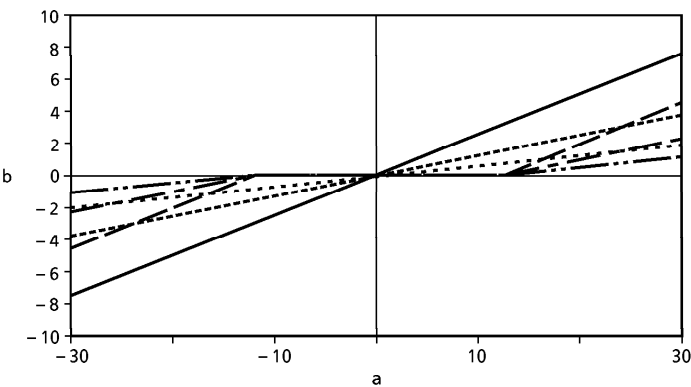


$$\text{Enhance level} = 20 \log \frac{a+b}{a} \text{ (dB)}$$

Vertical edge enhancement characteristic



Vertical edge enhancement characteristic (Zoom)



The relation between a and b.  
a : The difference of the luminance level in part of the edge.  
b : The component of vertical edge enhancement which is add to the luminance signal.  
Both are expressed by digital value.  
(However, this graph only shows adjustable enhance value of the device pin.)

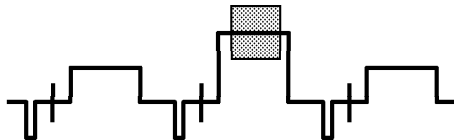
— (A) Enhance Value : 1.49dB  
- - (D) Enhance value : 1.49dB  
..... (B) 1.02dB                      ..... (C) 0.53dB  
- . - (E) 1.02dB                      - . - (F) 0.53dB

A, B, C : Coring=OFF    D, E, F : Coring=ON

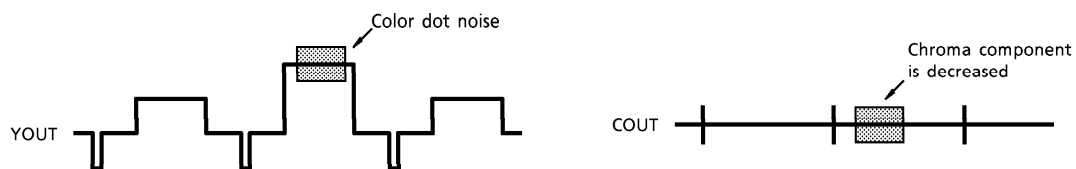
## 7. 1-line dot interference correction

Previously, a 1-line-only chrominance signal was processed as a luminance signal resulting in dot crawl. This circuit prevents this problem by extracting the 1-line dot component and adding it to the DCF output. This function is used with the NTSC system only, and can be set ON or OFF under I<sup>2</sup>C bus control. Under pin control, it is always ON.

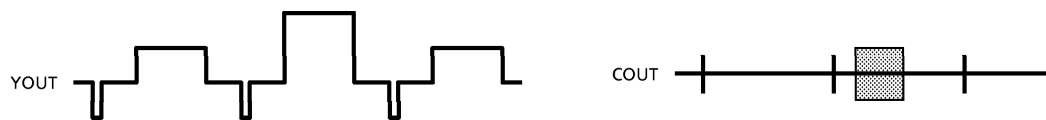
### (i) Input signal



### (ii) 1-line circuit output : OFF



### (iii) 1-line circuit output : ON



## 8. PLL (4× clock signal multiplier)

This block supplies a 4fsc (PLL 4× multiplied) signal for use as system clock. An fsc or 4fsc input clock is selectable under I<sup>2</sup>C bus control. Under pin control, the external clock signal is used, bypassing the PLL circuit.

## 9. Clock and memory timing generator (RTIM)

This block supplies a buffered system clock signal to the other circuit blocks, and also generates a timing signal for the memory blocks.

## 10. D/A converter (DAC)

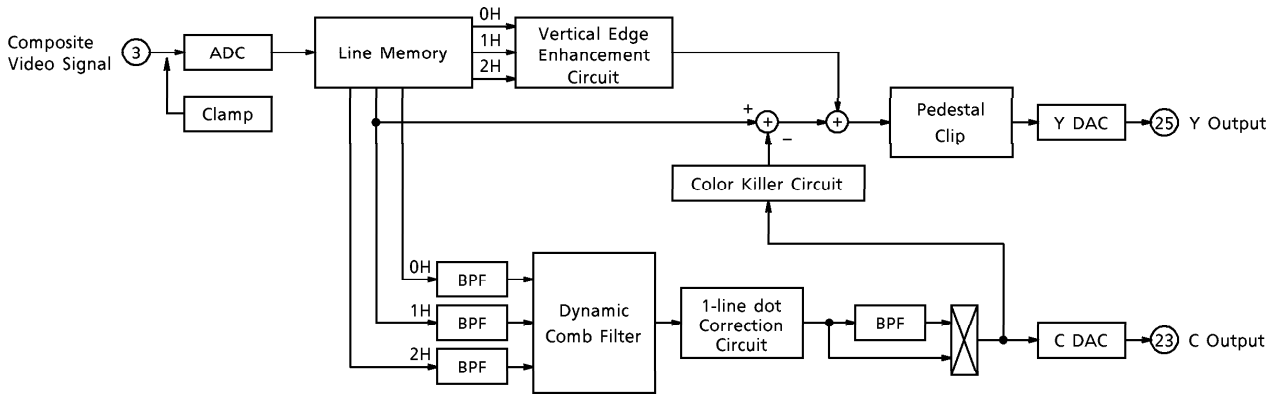
This block comprises a high-speed 8bit D/A converter. It provides Y output at approximately 2.0V<sub>p-p</sub> and burst-level C output at approximately 572mV<sub>p-p</sub>.

SIGNAL FLOW

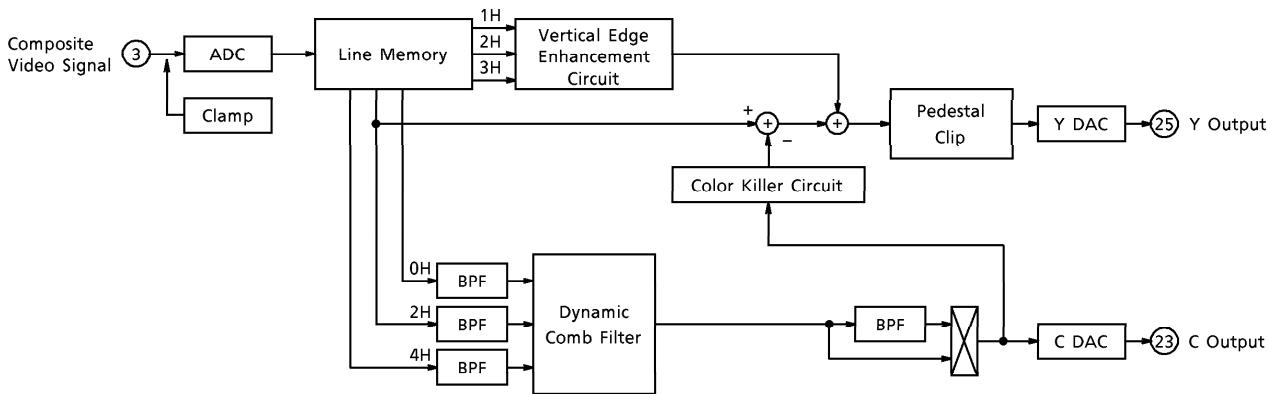
- Signal processing

| TV SYSTEM | METHOD OF Y / C SEPARATION    | VENH CIRCUIT | 1-LINE DOT CORRECTION CIRCUIT |
|-----------|-------------------------------|--------------|-------------------------------|
| NTSC      | 3-line (0H, 1H, 2H)           | ○ ( ± 1H)    | ○                             |
| PAL       | 3-line (0H, 2H, 4H)           | ○ ( ± 1H)    | —                             |
| N-PAL     | 3-line (0H, 2H, 4H)           | ○ ( ± 1H)    | —                             |
| M-PAL     | 3-line (0H, 2H, 4H)           | ○ ( ± 1H)    | —                             |
| 4.43NTSC  | Chroma BPF                    | ○ ( ± 1H)    | —                             |
| SECAM     | Bypass (Input→ADC→DAC→Output) | —            | —                             |

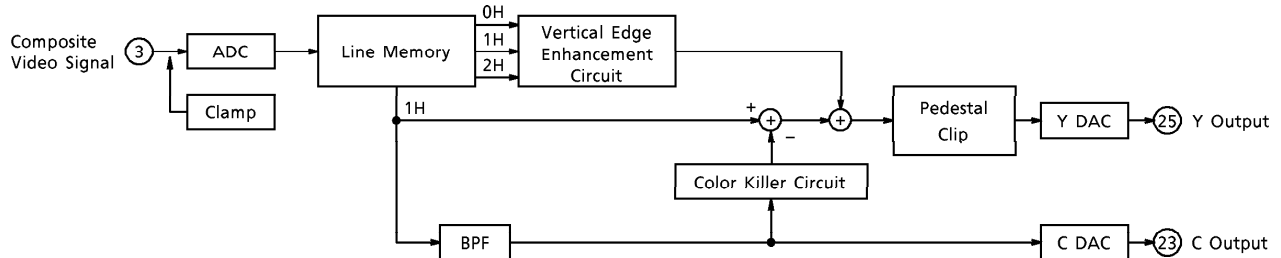
- Signal flow chart
- 1. NTSC system



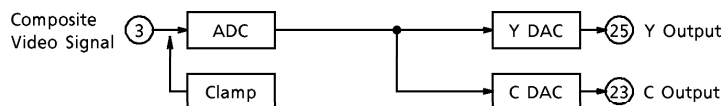
2. PAL, N-PAL, M-PAL systems



### 3. 4.43NTSC system



### 4. SECAM



## FUNCTION CONTROL

There are two ways to control TC9090AN and TC9090AF functions : through the I<sup>2</sup>C bus or through the device pins. The method used is selected with function control selector switch P/S (pin 7).

### • Function table

| FUNCTION                     | SYMBOL | CONTROL          |      | MODE                                                                                      |
|------------------------------|--------|------------------|------|-------------------------------------------------------------------------------------------|
|                              |        | I <sup>2</sup> C | PIN  |                                                                                           |
| TV System Selector           | TVSW   | ○                | ○    | NTSC, PAL, N-PAL, M-PAL 4.43NTSC, SECAM                                                   |
| VENH Level Selector          | VENH   | ○                | ○    | I <sup>2</sup> C bus control : 8 steps (0dB~1.94dB)<br>Pin control : 4 steps (0dB~1.49dB) |
| Color Killer Switch          | KILLER | ○                | ○    | Color, B / W                                                                              |
| Coring Switch                | CORING | ○                | ON   | Coring circuit on, off                                                                    |
| 1-Line Dot Correction Switch | 1LINE  | ○                | ON   | 1-line dot correction circuit on, off                                                     |
| Chroma Band-Width Selector   | CBPF   | ○                | Wide | Wide band width, narrow band width                                                        |
| PLL Selector                 | PLLSEL | ○                | ○    | fsc input, 4fsc input (PLL off)                                                           |

For KILLER and PLLSEL, pin control is also possible even in I<sup>2</sup>C bus control. When you set to "1" or "H" in either control, however, these settings have priority.

Example :

I<sup>2</sup>C bus : 1 Pin : L → I<sup>2</sup>C bus : 1 has priority.

I<sup>2</sup>C bus : 0 Pin : H → Pin : H has priority.

Bus controlled format of TC9090AN and TC9090AF are based on I<sup>2</sup>C bus control format of Philips.

|   |               |  |  |  |  |  |  |   |   |          |  |  |  |  |  |  |  |   |          |  |  |  |  |  |  |  |   |   |
|---|---------------|--|--|--|--|--|--|---|---|----------|--|--|--|--|--|--|--|---|----------|--|--|--|--|--|--|--|---|---|
| S | Slave address |  |  |  |  |  |  | 0 | A | 1st data |  |  |  |  |  |  |  | A | 2nd data |  |  |  |  |  |  |  | A | P |
|   |               |  |  |  |  |  |  |   |   |          |  |  |  |  |  |  |  |   |          |  |  |  |  |  |  |  |   |   |
|   | MSB ↑         |  |  |  |  |  |  |   |   | MSB ↑    |  |  |  |  |  |  |  |   | MSB ↑    |  |  |  |  |  |  |  |   |   |
|   | 7bit          |  |  |  |  |  |  |   |   | 8bit     |  |  |  |  |  |  |  |   | 8bit     |  |  |  |  |  |  |  |   |   |

S : Start Condition  
 P : Stop Condition  
 A : Acknowledge

The diagram illustrates the timing of the Start (S) and Stop (P) conditions in an I2C protocol. The SDA (Serial Data) and SCL (Serial Clock) lines are shown. The Start condition (S) is defined by a high-to-low transition on SDA while SCL is high. The Stop condition (P) is defined by a low-to-high transition on SDA while SCL is high. Both conditions are enclosed in dashed boxes.

The diagram shows three signals over time:

- SDA from master:** Starts high, goes low for a start condition (S), then high for a read operation (1), then low for a write operation (8), and finally high for a stop condition (9).
- SDA from slave:** High impedance during the read operation (1) and low during the write operation (8).
- SCL from slave:** High during the read operation (1) and low during the write operation (8).

| A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/ $\overline{W}$ |
|----|----|----|----|----|----|----|-------------------|
| 1  | 0  | 1  | 1  | 0  | 0  | 1  | 0                 |

Purchase of TOSHIBA I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.

I<sup>2</sup>C BUS CONTROL DATA REGISTERS

Value in tables are default initialization values.

DATA1

| MSB   |       |       |       |       |       |      | LSB    |
|-------|-------|-------|-------|-------|-------|------|--------|
| TVSW1 | TVSW2 | TVSW3 | VENH0 | VENH1 | VENH2 | CBPF | KILLER |
| 0     | 0     | 0     | 0     | 0     | 0     | 0    | 0      |

TVSW1~3 : Selects the TV system.

000 = TEST (not used)

001 = M-PAL

010 = N-PAL

011 = PAL

100 = 4.43NTSC

101 = SECAM

110 = 3.58NTSC

VENH0~2 : Sets level of vertical edge enhancement.

000 = 0dB

001 = 0.27dB

010 = 0.53dB

011 = 0.78dB

100 = 1.02dB

101 = 1.26dB

110 = 1.49dB

111 = 1.94dB

CBPF : Selects the chroma output band width by switching on or off the BPF that follows DCF.

0 = Wide band width

1 = Narrow band width

KILLER : Switches color killer circuit.

0 = Color mode (color killer circuit OFF)

1 = B/W mode (color killer circuit ON)

## DATA2

| MSB           |             |             |  |  |  |  | LSB |
|---------------|-------------|-------------|--|--|--|--|-----|
| 1LINEDOT<br>0 | CORING<br>0 | PLLSEL<br>0 |  |  |  |  |     |

1LINEDOT : Switches 1-line dot correction circuit on or off.

0 = ON

1 = OFF

CORING : Switches coring circuit on or off.

0 = ON

1 = OFF

PLLSEL : Selects input clock frequency.

0 = fsc input, PLL circuit is used

1 = 4fsc input, PLL circuit is bypassed

## PIN CONTROL

| MODE   | ACTION                   | PIN 7<br>P / S | PIN 8<br>SDA<br>(TVSW1) | PIN 9<br>SCL<br>(TVSW2) | PIN 10<br>RESET<br>(TVSW3) | PIN 11<br>TEST1<br>(VENH0) | PIN 12<br>TEST2<br>(VENH1) | PIN 13<br>KILLER | PIN 14<br>PLLSEL |
|--------|--------------------------|----------------|-------------------------|-------------------------|----------------------------|----------------------------|----------------------------|------------------|------------------|
| P / S  | I <sup>2</sup> C Control | L              | —                       | —                       | —                          | —                          | —                          | —                | —                |
|        | Pin Control              | H              | —                       | —                       | —                          | —                          | —                          | —                | —                |
| KILLER | Color                    | —              | —                       | —                       | —                          | —                          | —                          | L                | —                |
|        | B / W                    | —              | —                       | —                       | —                          | —                          | —                          | H                | —                |
| TVSW   | TEST                     | H              | L                       | L                       | L                          | —                          | —                          | —                | —                |
|        | M-PAL                    | H              | L                       | L                       | H                          | —                          | —                          | —                | —                |
|        | N-PAL                    | H              | L                       | H                       | L                          | —                          | —                          | —                | —                |
|        | PAL                      | H              | L                       | H                       | H                          | —                          | —                          | —                | —                |
|        | 4.43NTSC                 | H              | H                       | L                       | L                          | —                          | —                          | —                | —                |
|        | SECAM                    | H              | H                       | L                       | H                          | —                          | —                          | —                | —                |
|        | 3.58NTSC                 | H              | H                       | H                       | L                          | —                          | —                          | —                | —                |
| VENH   | VENH circuit OFF         | H              | —                       | —                       | —                          | L                          | L                          | —                | —                |
|        | VENH level = 0.53dB      | H              | —                       | —                       | —                          | L                          | H                          | —                | —                |
|        | VENH level = 1.02dB      | H              | —                       | —                       | —                          | H                          | L                          | —                | —                |
|        | VENH level = 1.49dB      | H              | —                       | —                       | —                          | H                          | H                          | —                | —                |
| PLLSEL | fsc input                | —              | —                       | —                       | —                          | —                          | —                          | —                | L                |
|        | 4fsc input               | —              | —                       | —                       | —                          | —                          | —                          | —                | H                |

## RATINGS AND CHARACTERISTICS

The following specifications were obtained in part from the test circuit shown on page 19.

## MAXIMUM RATINGS (Ta = 25°C)

| CHARACTERISTIC       | SYMBOL                | RATING                                 | UNIT |
|----------------------|-----------------------|----------------------------------------|------|
| Power Supply Voltage | V <sub>DD</sub>       | V <sub>SS</sub> ~V <sub>SS</sub> + 6.0 | V    |
| Input Voltage        | V <sub>IN</sub>       | -0.3~V <sub>DD</sub> + 0.3             | V    |
| Power Dissipation    | P <sub>D</sub> (Note) | 900                                    | mW   |
|                      |                       | 600                                    |      |
| Storage Temperature  | T <sub>stg</sub>      | -55~125                                | °C   |

(Note) Ta = 75°C

## RECOMMENDED OPERATING CONDITIONS

| CHARACTERISTIC        | SYMBOL           | TEST CONDITION | MIN. | TYP. | MAX.            | UNIT |
|-----------------------|------------------|----------------|------|------|-----------------|------|
| Power Supply Voltage  | V <sub>DD</sub>  | —              | 4.75 | 5.00 | 5.25            | V    |
| Input Voltage         | V <sub>IN</sub>  | —              | 0    | —    | V <sub>DD</sub> | V    |
| Operating Temperature | T <sub>opr</sub> | —              | -10  | —    | 75              | °C   |

## ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (Ta = 25°C, V<sub>DD</sub> = 5V)

| CHARACTERISTIC             |            | SYMBOL           | TEST CIR-<br>CUIT | TEST CONDITION                                                                                                      | MIN. | TYP. | MAX. | UNIT |
|----------------------------|------------|------------------|-------------------|---------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| Power Supply Voltage       |            | V <sub>DD</sub>  | 1                 | CLOCK =<br>4.43361875MHz (PAL)<br><br>VREL1 = 3.0V<br>1 / 2V <sub>DD</sub> = 2.5V<br><br>V <sub>IN</sub> = No input | 4.75 | 5.00 | 5.25 | V    |
| Supply Current             |            | I <sub>DD</sub>  | 1                 |                                                                                                                     | 60   | 80   | 100  | mA   |
| Output Voltage Level       |            | Y <sub>OUT</sub> | 1                 |                                                                                                                     | 2.9  | 3.0  | 3.2  | V    |
|                            |            | C <sub>OUT</sub> |                   |                                                                                                                     | 3.8  | 4.0  | 4.2  |      |
| Pin Voltage Level          |            | VREFL            | 1                 |                                                                                                                     | 1.2  | 1.5  | 1.8  | V    |
|                            |            | VREFH            |                   |                                                                                                                     | 3.2  | 3.5  | 3.8  |      |
|                            |            | ADIN             |                   |                                                                                                                     | 1.3  | 1.6  | 1.9  |      |
|                            |            | BIAS1            |                   |                                                                                                                     | 0.9  | 1.3  | 1.7  |      |
|                            |            | BIAS2            |                   |                                                                                                                     | 1.0  | 1.6  | 2.2  |      |
|                            |            | BIAS3            |                   |                                                                                                                     | 2.5  | 3.5  | 4.5  |      |
|                            |            | VFIL             |                   |                                                                                                                     | 0.9  | 1.8  | 2.5  |      |
|                            |            | CKIN             |                   |                                                                                                                     | 1.8  | 2.4  | 3.0  |      |
| Input Voltage              | High Level | V <sub>IH</sub>  | 1                 |                                                                                                                     | 4    | —    | —    | V    |
|                            | Low Level  | V <sub>IL</sub>  | 1                 | —                                                                                                                   | —    | 1    |      |      |
| ADIN Pin Input Capacitance |            | C <sub>IN</sub>  | 1                 | —                                                                                                                   | 50   | —    | pF   |      |
| Pull-Down Resistance       |            | R <sub>pD</sub>  | 1                 | 25                                                                                                                  | 50   | 100  | kΩ   |      |

## AC CHARACTERISTICS

Y output (Ta = 25°C, V<sub>DD</sub> = 5V, V<sub>REF1</sub> = 3.0V, Input Clock : fsc, 0.4V<sub>p-p</sub>, S1 = 2)

| CHARACTERISTIC     |                      |         | SYMBOL             | TEST CIR-<br>CUIT | TEST CONDITION                                                                                                                                                                                                                                               | MIN.  | TYP.  | MAX.  | UNIT             |
|--------------------|----------------------|---------|--------------------|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|-------|------------------|
| Input Level        |                      |         | V <sub>IN</sub>    | 1                 | —                                                                                                                                                                                                                                                            | —     | 1.5   | 1.6   | V <sub>p-p</sub> |
| Low Frequency Gain |                      |         | GV                 | 1                 | S2 = 2, S3 = 2, S4 = 1, S5 = 2<br>V <sub>IN</sub> = f <sub>H</sub> 1.5V <sub>p-p</sub> V <sub>d</sub> c = 2.5V                                                                                                                                               | − 0.5 | 0.0   | 0.5   | dB               |
| 3.58NTSC           | Frequency Response   | f2 / f1 | FWN <sub>n</sub>   | 1                 | S2 = 2, S3 = 2, S4 = 1, S5 = 2<br>V <sub>IN</sub> = 1.5V <sub>p-p</sub> V <sub>d</sub> c = 2.5V<br><br>Frequency response :<br>Gain (f <sub>n</sub> ) – Gain (f1),<br>(n = 2, 4, 5)<br><br>Comb characteristics :<br>Gain (comb top)<br>– Gain (comb bottom) | − 2.5 | − 2.0 | − 0.9 | dB               |
|                    |                      | f4 / f1 | FWW <sub>n</sub>   |                   |                                                                                                                                                                                                                                                              | − 3.5 | − 2.5 | − 1.6 |                  |
|                    | Comb Characteristics | f2 / f3 | YCOM <sub>n</sub>  |                   |                                                                                                                                                                                                                                                              | 40    | 45    | —     |                  |
| PAL                | Frequency Response   | f2 / f1 | FWN <sub>p</sub>   |                   |                                                                                                                                                                                                                                                              | − 2.5 | − 2.0 | − 0.9 | dB               |
|                    |                      | f4 / f1 | FWW <sub>p</sub>   |                   |                                                                                                                                                                                                                                                              | − 3.5 | − 2.5 | − 1.6 |                  |
|                    | Comb Characteristics | f2 / f3 | YCOM <sub>p</sub>  |                   |                                                                                                                                                                                                                                                              | 40    | 45    | —     |                  |
| N-PAL              | Frequency Response   | f2 / f1 | FWN <sub>np</sub>  |                   |                                                                                                                                                                                                                                                              | − 2.5 | − 2.0 | − 0.9 | dB               |
|                    |                      | f4 / f1 | FWW <sub>np</sub>  |                   |                                                                                                                                                                                                                                                              | − 3.5 | − 2.5 | − 1.6 |                  |
|                    | Comb Characteristics | f2 / f3 | YCOM <sub>np</sub> |                   |                                                                                                                                                                                                                                                              | 40    | 45    | —     |                  |
| M-PAL              | Frequency Response   | f2 / f1 | FWN <sub>mp</sub>  |                   |                                                                                                                                                                                                                                                              | − 2.5 | − 2.0 | − 0.9 | dB               |
|                    |                      | f4 / f1 | FWW <sub>mp</sub>  |                   |                                                                                                                                                                                                                                                              | − 3.5 | − 2.5 | − 1.6 |                  |
|                    | Comb Characteristics | f2 / f3 | YCOM <sub>mp</sub> |                   |                                                                                                                                                                                                                                                              | 40    | 45    | —     |                  |
| 4.43NTSC           | Frequency Response   | f5 / f1 | FWN <sub>4n</sub>  |                   |                                                                                                                                                                                                                                                              | − 3.0 | − 2.5 | − 1.9 | dB               |
|                    |                      | f1 / f2 | FWW <sub>4n</sub>  |                   |                                                                                                                                                                                                                                                              | 40    | 45    | —     |                  |
| Linearity          |                      | Y1 / Y2 | L <sub>s</sub>     | 1                 | S2 = 1, S3 = 1, S4 = 1, S5 = 2<br>V <sub>IN</sub> = 5-step signal<br>1.5V <sub>p-p</sub>                                                                                                                                                                     | 37    | 40    | 43    | %                |
|                    |                      | S / Y2  | L <sub>y</sub>     |                   |                                                                                                                                                                                                                                                              | 57    | 60    | 63    |                  |
| Output Impedance   |                      |         | Z <sub>o</sub>     | 1                 | S2 = 2, S3 = 2, S5 = 2<br>V <sub>IN</sub> = f <sub>H</sub> 1.5V <sub>p-p</sub> V <sub>d</sub> c = 2.5V<br><br>$Z_o = \frac{V_1 - V_2}{V_2} \times 300$<br><br>V1 : S4 = 1, V2 : S4 = 2                                                                       | —     | 400   | —     | Ω                |

| CHARACTERISTIC                             | SYMBOL | TEST CIR-CUIT | TEST CONDITION                                   | MIN. | TYP. | MAX. | UNIT              |
|--------------------------------------------|--------|---------------|--------------------------------------------------|------|------|------|-------------------|
| Clock Leak<br>(4fsc Components)            | Lck    | 1             | S2 = 2, S3 = 2, S4 = 1, S5 = 1<br>VIN = No input | —    | 5.0  | 20   | mV <sub>rms</sub> |
| Fundamental Clock Leak<br>(fsc Components) | Lsc    | 1             | S2 = 2, S3 = 2, S4 = 1, S5 = 1<br>VIN = No input | —    | 1.0  | 2.0  | mV <sub>rms</sub> |

(Note)  $f_1 = f_H$ ,  $f_2 = f_{sc}$ ,  $f_3$  (NTSC) =  $f_{sc} + 1 / 2f_H$ ,  $f_3$  (PAL) =  $f_{sc} + 1 / 4f_H + 25\text{Hz}$ ,  $f_4 = 3 / 4f_{sc}$

|       | 3.58NTSC   | PAL        | N-PAL      | M-PAL      | 4.43NTSC   |
|-------|------------|------------|------------|------------|------------|
| $f_1$ | 15734.26   | 15625.00   | 15625.00   | 15734.26   | 15750.00   |
| $f_2$ | 3579545.00 | 4433618.75 | 3582056.25 | 3575611.49 | 4433618.75 |
| $f_3$ | 3587412.13 | 4437550.00 | 3585987.50 | 3579545.06 | —          |
| $f_4$ | 4772726.67 | 5911491.67 | 4776075.00 | 4767481.99 | —          |
| $f_5$ | —          | —          | —          | —          | 3000000.00 |

Unit : Hz

C output ( $T_a = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ ,  $V_{REF1} = 3.0\text{V}$ , Input Clock : fsc,  $0.4V_{p-p}$ , S1 = 1)

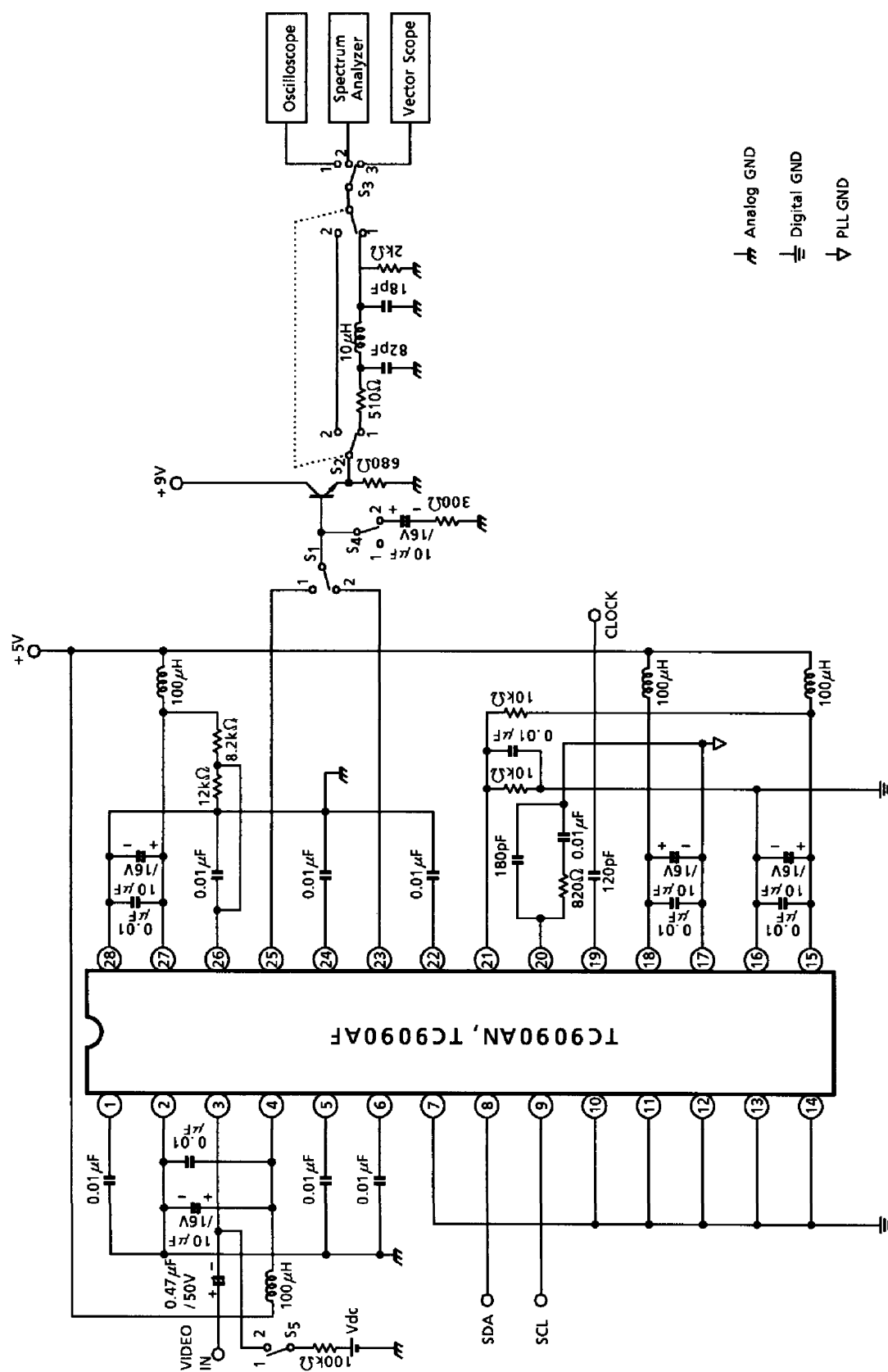
| CHARACTERISTIC |                      |        | SYMBOL            | TEST CIR-CUIT | TEST CONDITION                                                                                     | MIN. | TYP. | MAX. | UNIT |
|----------------|----------------------|--------|-------------------|---------------|----------------------------------------------------------------------------------------------------|------|------|------|------|
| Gain           |                      |        | CV                | 1             | S2 = 2, S3 = 2, S4 = 1, S5 = 1<br>VIN = 430mV <sub>p-p</sub>                                       | -2.0 | -1.5 | -0.6 | dB   |
| 3.58NTSC       | BPF Characteristics  | Wide   | BWCW <sub>n</sub> | 1             | S2 = 2, S3 = 2, S4 = 1, S5 = 2<br>VIN = 1.5V <sub>p-p</sub> Vdc = 2.5V<br>(fsc - 503496Hz) - (fsc) | -0.5 | -0.2 | —    | dB   |
|                |                      | Narrow | BWCN <sub>n</sub> |               |                                                                                                    | -1   | -0.5 | —    |      |
|                | Comb Characteristics |        | CCOM <sub>n</sub> |               | S2 = 2, S3 = 2, S4 = 1, S5 = 2<br>VIN = 430mV <sub>p-p</sub> Vdc = 2.5V                            | 30   | 35   | —    |      |
| PAL            | BPF Characteristics  |        | BW <sub>p</sub>   | 1             | S2 = 2, S3 = 2, S4 = 1, S5 = 2<br>VIN = 1.5V <sub>p-p</sub> Vdc = 2.5V<br>(fsc - 500000Hz) - (fsc) | -0.5 | -0.2 | —    | dB   |
|                | Comb Characteristics |        | CCOM <sub>p</sub> |               | S2 = 2, S3 = 2, S4 = 1, S5 = 2<br>VIN = 430mV <sub>p-p</sub> Vdc = 2.5V                            | 30   | 35   | —    |      |

| CHARACTERISTIC                             |                      | SYMBOL             | TEST CIR-<br>CUIT | TEST CONDITION                                                                                                                                                                            | MIN.  | TYP.  | MAX.  | UNIT              |
|--------------------------------------------|----------------------|--------------------|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|-------|-------------------|
| N-PAL                                      | BPF Characteristics  | BW <sub>np</sub>   | 1                 | S2 = 2, S3 = 2, S4 = 1, S5 = 2<br>V <sub>IN</sub> = 1.5V <sub>p-p</sub> , V <sub>dc</sub> = 2.5V<br>(fsc – 500000Hz) – (fsc)                                                              | – 0.5 | – 0.2 | —     | dB                |
|                                            | Comb Characteristics | CCOM <sub>np</sub> |                   | S2 = 2, S3 = 2, S4 = 1, S5 = 2<br>V <sub>IN</sub> = 430mV <sub>p-p</sub> , V <sub>dc</sub> = 2.5V                                                                                         | 30    | 35    | —     |                   |
| M-PAL                                      | BPF Characteristics  | BW <sub>mp</sub>   | 1                 | S2 = 2, S3 = 2, S4 = 1, S5 = 2<br>V <sub>IN</sub> = 1.5V <sub>p-p</sub> , V <sub>dc</sub> = 2.5V<br>(fsc – 503496Hz) – (fsc)                                                              | – 0.5 | – 0.2 | —     | dB                |
|                                            | Comb Characteristics | CCOM <sub>mp</sub> |                   | S2 = 2, S3 = 2, S4 = 1, S5 = 2<br>V <sub>IN</sub> = 430mV <sub>p-p</sub> , V <sub>dc</sub> = 2.5V                                                                                         | 30    | 35    | —     |                   |
| 4.43NTSC                                   | BPF Characteristics  | BWN <sub>4n</sub>  | 1                 | S2 = 2, S3 = 2, S4 = 1, S5 = 2<br>V <sub>IN</sub> = 1.5V <sub>p-p</sub> , V <sub>dc</sub> = 2.5V<br>(fsc – F) – (fsc)<br>BWN <sub>4n</sub> : F = 500kHz<br>BWW <sub>4n</sub> : F = 1.5MHz | – 3.0 | – 1.9 | – 1.5 | dB                |
|                                            |                      | BWW <sub>4n</sub>  |                   |                                                                                                                                                                                           | – 20  | – 16  | – 13  |                   |
| Differential Gain                          |                      | DG                 | 1                 | S2 = 2, S3 = 3, S4 = 1, S5 = 1<br>V <sub>IN</sub> = 5-step signal<br>Y = 140IRE                                                                                                           | 0     | 2     | 5     | %                 |
| Differential Phase                         |                      | DP                 | 1                 | C = 40IRE<br>DG =<br>(Comax – Comin) / Comax                                                                                                                                              | 0     | 2     | 5     | °                 |
| Output Impedance                           |                      | Zo                 | 1                 | S2 = 2, S3 = 2, S5 = 2<br>V <sub>IN</sub> = f <sub>H</sub> 1.5V <sub>p-p</sub> , V <sub>dc</sub> = 2.5V<br>$Z_o = \frac{V_1 - V_2}{V_2} \times 300$<br>V1 : S4 = 1, V2 : S4 = 2           | —     | 400   | —     | Ω                 |
| Clock Leak<br>(4fsc Components)            |                      | Lck                | 1                 | S2 = 2, S3 = 2, S4 = 1, S5 = 1<br>V <sub>IN</sub> = No input                                                                                                                              | —     | 5.0   | 20    | mV <sub>rms</sub> |
| Fundamental Clock Leak<br>(fsc Components) |                      | Lsc                | 1                 | S2 = 2, S3 = 2, S4 = 1, S5 = 1<br>V <sub>IN</sub> = No input                                                                                                                              | —     | 0.3   | 1     | mV <sub>rms</sub> |

## PLL CIRCUIT CHARACTERISTICS

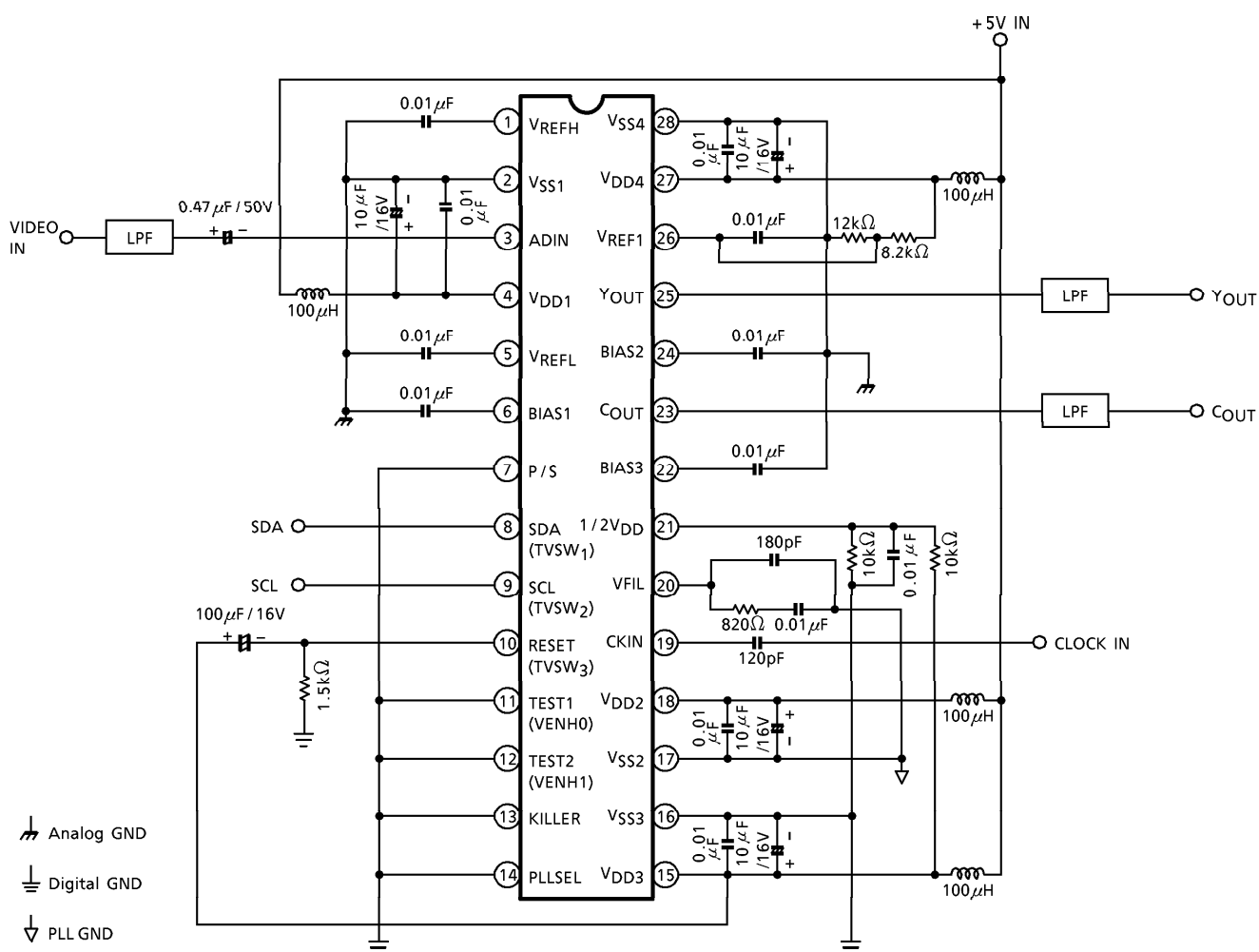
| CHARACTERISTIC                      | SYMBOL | TEST CIR-CUIT | TEST CONDITION | MIN. | TYP. | MAX. | UNIT      |
|-------------------------------------|--------|---------------|----------------|------|------|------|-----------|
| Pull-In Frequency Range             | fck    | 1             | —              | 3.57 | —    | 4.44 | MHz       |
| Input Amplitude<br>(fsc Components) | Vck    | 1             | —              | 0.3  | 0.4  | —    | $V_{p-p}$ |

## TEST CIRCUIT 1



TC9090AN/AF - 19

## APPLICATION CIRCUIT

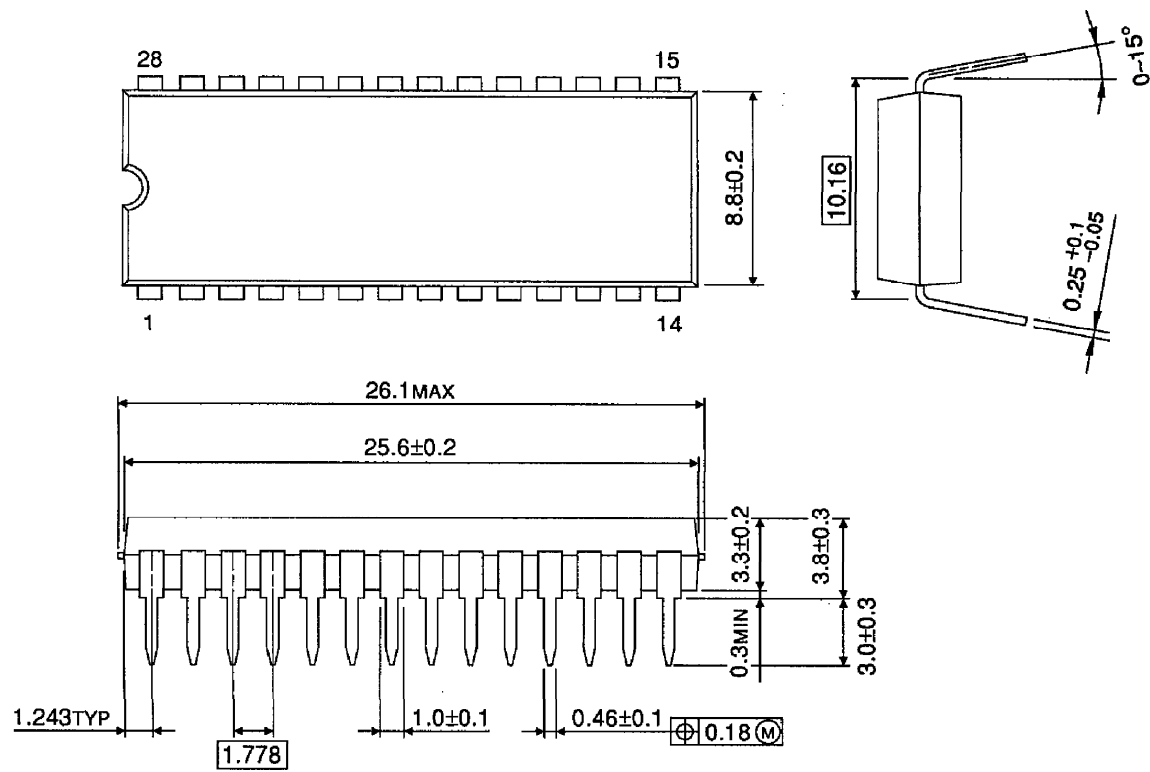


(Note) About PCB design :

To reduce input/output signal noise, isolate the analog, digital and PLL circuits from one another.

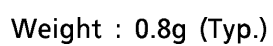
PACKAGE DIMENSIONS  
SDIP28-P-400-1.78

Unit : mm



Weight : 1.7g (Typ.)

## Unit : mm



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000707EBA

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