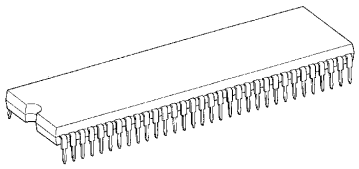
TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB1212N, TB1212F

SINGLE CHIP NICAM SYSTEM

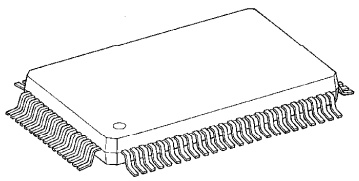
The TB1212N and TB1212F are single chip processor for NICAM (Near Instananeous Conpand Audio. Multiplex) System. This is to get a PCM sound signal from QPSK modulated signal and to get an analog sound signal selected between said PCM sound signal and FM sound signal.
Functionally, QPSK demodulation, sound data decoding, sound channel selection, Digital filter, DAC, and so on are integrated into one chip.

TB1212N



SDIP64-P-750-1.78

TB1212F



QFP80-P-1420-0.80A

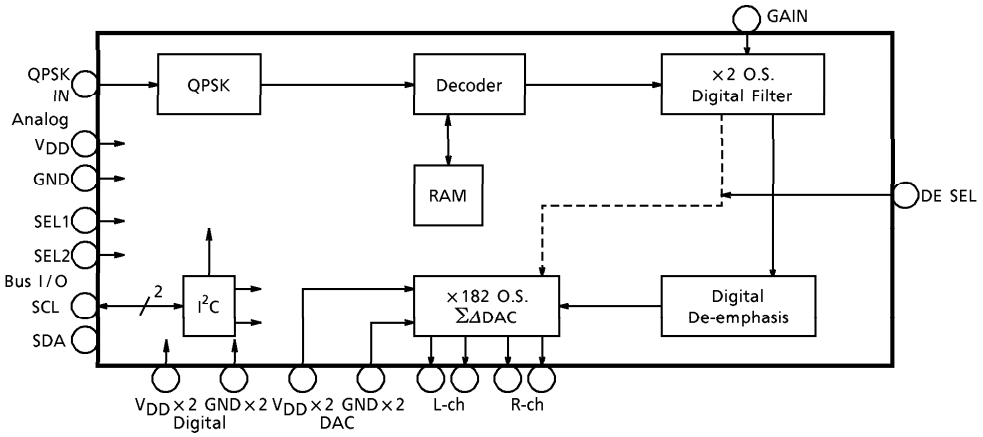
Weight
SDIP64-P-750-1.78 : 8.85g (Typ.)
QFP80-P-1420-0.80A : 1.6g (Typ.)

FEATURES

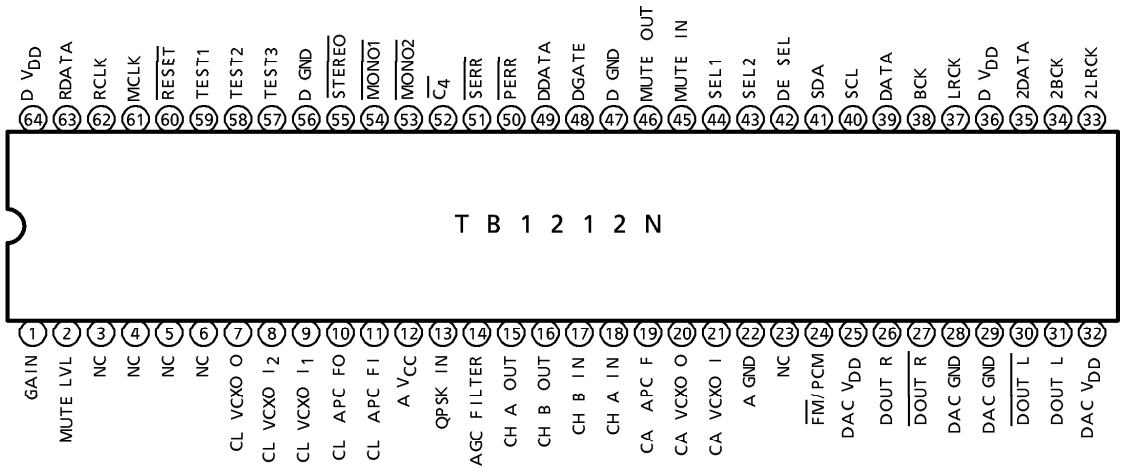
- AGC Circuit
- Phase Synchronous Demodulation by Base Band Select PLL
- Frame Sync. Detection. (FAW Sync., C_0 Sync.)
- De-scramble. (PN code reduction)
- Control data majority-decision detection
- De-interleave.
- Range bit majority-decision detection
- Control information bit majority-decision detection
- Parity detection and error correction
- 10→14bit expansion
- Digital Muting Circuit (Variable Mute Level)
- I^2C bus interface
- Built in RAM (3.5Kbit)

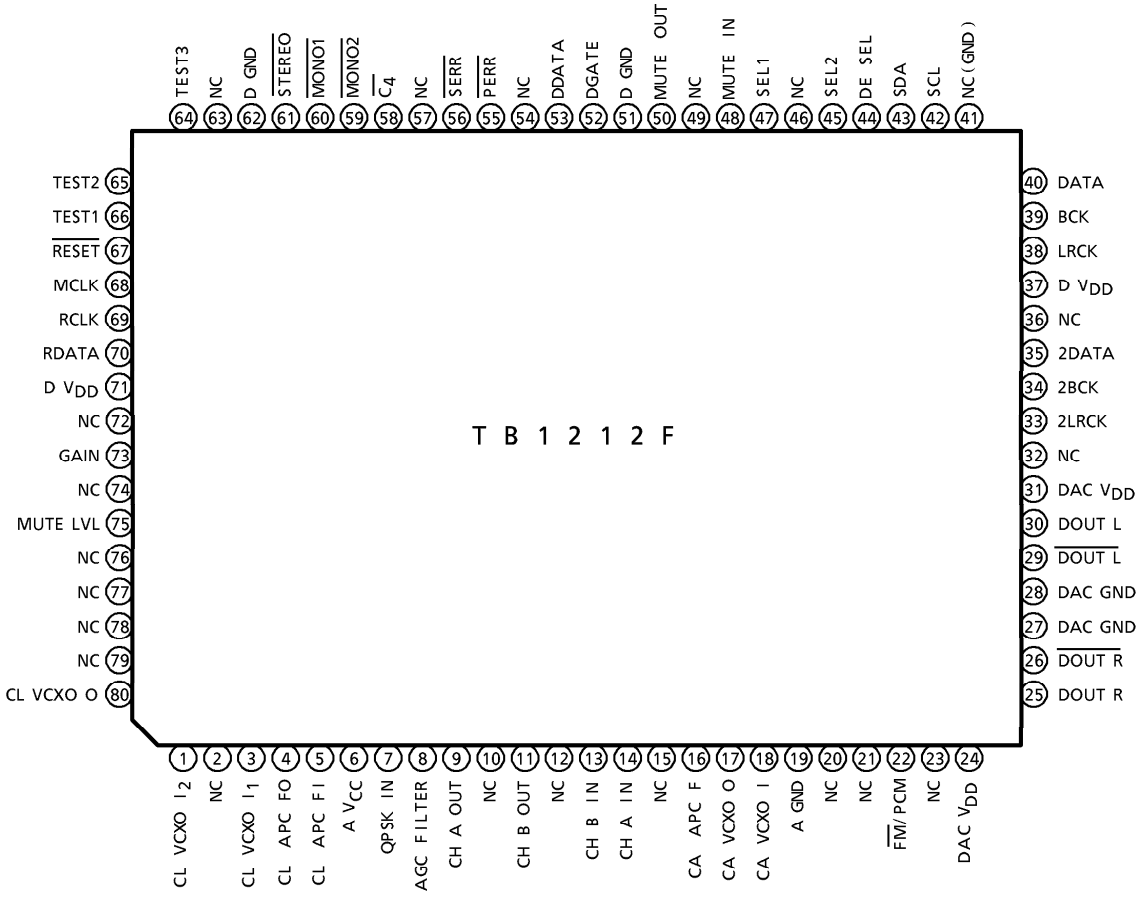
- 2 times over sampling digital filter
- Switchable Digital De-emphasis (CCITT Recommendation J.17)
- 182 times over sampling ΣΔDAC
- 5V power Supply

BLOCK DIAGRAM



TERMINAL CONNECTION DIAGRAM





TERMINAL FUNCTION (64 PIN SHRINK DIP)

PIN No.	PIN NAME	I/O	FUNCTION
1	GAIN	I	GAIN −6dB / −3.5dB Select SW (L : −6dB, H : −3.5dB)
2	MUTE LVL	I	MUTE level control
3	N.C	—	—
4	N.C	—	—
5	N.C	—	—
6	N.C	—	—
7	CL VCXO O	O	Data Clock VCXO output
8	CL VCXO I_2	I	Data Clock VCXO input 2
9	CL VCXO I_1	I	Data Clock VCXO input 1
10	CL APC FO	O	Data Clock APC filter output
11	CL APC FI	I	Data Clock APC filter input
12	A V_{CC}	—	Analog V_{CC} 5V ± 10%
13	QPSK IN	I	QPSK signal input
14	AGC FILTER	O	AGC filter output
15	CH A OUT	O	Channel A detection output
16	CH B OUT	O	Channel B detection output
17	CH B IN	I	Channel B detection input
18	CH A IN	I	Channel A detection input
19	CA APC F	O	Carrier APC filter output
20	CA VCXO O	O	Carrier VCXO output
21	CA VCXO I	I	Carrier VCXO input
22	A GND	—	Analog GND
23	N.C	—	—
24	$\overline{FM}$ / PCM	O	FM / PCM select (H : FM, L : PCM)
25	DAC V_{DD}	—	DAC power supply 5V ± 10%
26	DOUT R	O	PCM sound Digital data output R (Positive)
27	$\overline{DOUT\ R}$	O	PCM sound Digital data output R (Negative)
28	DAC GND	—	DAC GND
29	DAC GND	—	DAC GND
30	DOUT L	O	PCM sound Digital data output L (Positive)
31	$\overline{DOUT\ L}$	O	PCM sound Digital data output L (Negative)
32	DAC V_{DD}	—	DAC power supply 5V ± 10%
33	2LRCK	O	LR clock output for DAC (×2 over sampling)
34	2BCK	O	Bit clock output for DAC (×2 over sampling)
35	2DATA	O	DATA output for DAC (×2 over sampling)
36	D V_{DD}	—	Digital V_{DD} 5V ± 10%
37	LRCK	O	LR clock output for DAC
38	BCK	O	Bit clock output for DAC
39	DATA	O	DATA output for DAC
40	SCL	I	SCL input for I^2C bus control

PIN No.	PIN NAME	I/O	FUNCTION
41	SDA	I/O	SCL input for I^2C bus control
42	DE SEL	I	Digital De-emphasis control (L : use, H : No use)
43	SEL2	I	PCM Audio output selection signal input
44	SEL1	I	PCM Audio output selection signal input
45	MUTE IN	I	Digital Mute signal input
46	MUTE OUT	O	Digital Mute signal output
47	D GND	—	Digital GND
48	D GATE	O	Gate signal for data output
49	D DATA	O	Data output
50	$\overline{PERR}$	O	Parity error output
51	$\overline{SERR}$	O	Sync error output
52	$\overline{C_4}$	O	Mode display signal output : C_4
53	$\overline{MONO2}$	O	Mode display signal output : Monaural 2
54	$\overline{MONO1}$	O	Mode display signal output : Monaural 1
55	$\overline{STEREO}$	O	Mode display signal output : Stereo
56	D GND	—	Digital GND
57	TEST3	I	Test terminal (to be grounded to D.GND)
58	TEST2	I	Test terminal (to be grounded to D.GND)
59	TEST1	I	Test terminal (to be grounded to D.GND)
60	$\overline{RESET}$	I	RESET input
61	MCLK	O	Clock output 2 (5.824MHz)
62	RCLK	O	Clock output 1 (728MHz)
63	RDATA	O	Bit Stream data output
64	D V_{DD}	—	Digital V_{DD} 5V ± 10%

TERMINAL FUNCTION (80 PIN FP)

PIN No.	PIN NAME	I / O	FUNCTION
1	C_L VCXO I_2	I	Data Clock VCXO input 2
2	N.C	—	—
3	C_L VCXO I_1	I	Data Clock VCXO input 1
4	C_L APC FO	O	Data Clock APC filter output
5	C_L APC FI	I	Data Clock APC filter input
6	A V_{CC}	—	Analog V_{CC} 5V ± 10%
7	QPSK IN	I	QPSK signal input
8	AGC FILTER	O	AGC filter output
9	CH A OUT	O	Channel A detection output
10	N.C	—	—
11	CH B OUT	O	Channel B detection output
12	N.C	—	—
13	CH B IN	I	Channel B detection input
14	CH A IN	I	Channel A detection input
15	N.C	—	—
16	CA APC F	O	Carrier APC filter output
17	CA VCXO O	O	Carrier VCXO output
18	CA VCXO I	I	Carrier VCXO input
19	A GND	—	Analog GND
20	N.C	—	—
21	N.C	—	—
22	$\overline{FM}$ / PCM	O	FM / PCM select (H : PCM, L : FM)
23	N.C	—	—
24	DAC V_{DD}	—	DAC power supply 5V ± 10%
25	DOUT R	O	PCM sound Digital data output R (Positive)
26	$\overline{DOUT\ R}$	O	PCM sound Digital data output R (Negative)
27	DAC GND	—	DAC GND
28	DAC GND	—	DAC GND
29	DOUT L	O	PCM sound Digital data output L (Positive)
30	$\overline{DOUT\ L}$	O	PCM sound Digital data output L (Negative)
31	DAC V_{DD}	—	DAC power supply 5V ± 10%
32	N.C	—	—
33	2LRCK	O	LR clock output for DAC (×2 over sampling)
34	2BCK	O	Bit clock output for DAC (×2 over sampling)
35	2DATA	O	DATA output for DAC (×2 over sampling)
36	N.C	—	—
37	D V_{DD}	—	Digital V_{DD} 5V ± 10%
38	LRCK	O	LR clock output for DAC
39	BCK	O	Bit clock output for DAC
40	DATA	O	DATA output for DAC

PIN No.	PIN NAME	I/O	FUNCTION
41	N.C (GND)	—	—
42	SCL	I	SCL input for I^2C bus control
43	SDA	I/O	SDA input/output for I^2C bus control
44	DE SEL	I	Digital De-emphasis control (L : use, H : No use)
45	SEL2	I	PCM Audio output selection signal input
46	N.C	—	—
47	SEL1	I	PCM Audio output selection signal input
48	MUTE IN	I	Digital Mute signal input
49	N.C	—	—
50	MUTE OUT	O	Digital Mute signal output
51	D GND	—	Digital GND
52	D GATE	O	Gate signal for data output
53	D DATA	O	Data output
54	N.C	O	—
55	$\overline{PERR}$	O	Parity error output
56	$\overline{SERR}$	O	Sync error output
57	N.C	—	—
58	$\overline{C_4}$	O	Mode display signal output : C_4
59	$\overline{MONO2}$	O	Mode display signal output : Monaural 2
60	$\overline{MONO1}$	O	Mode display signal output : Monaural 1
61	$\overline{STEREO}$	O	Mode display signal output : Stereo
62	D GND	—	Digital GND
63	N.C	—	—
64	TEST3	I	Test terminal (to be grounded to D.GND)
65	TEST2	I	Test terminal (to be grounded to D.GND)
66	TEST1	I	Test terminal (to be grounded to D.GND)
67	$\overline{RESET}$	I	RESET input
68	MCLK	O	Clock output 2 (5.824MHz)
69	RCLK	O	Clock output 1 (728MHz)
70	RDATA	O	Bit Stream data output
71	D V_{DD}	—	Digital V_{DD} 5V ± 10%
72	N.C	—	—
73	GAIN	I	GAIN −6dB / −3.5dB Select SW (L : −6dB, H : −3.5dB)
74	N.C	—	—
75	MUTE LVL	I	MUTE level control
76	N.C	—	—
77	N.C	—	—
78	N.C	—	—
79	N.C	—	—
80	C_L VCXO O	O	Data Clock VCXO output

FUNCTION

(1) Outline explain

1. QPSK demodulation stage

   This stage is to get PCM digital data stream from the QPSK signal. An AGC for input signal, VCXO for Carrier and Clock, differential operation, and P / S conversion functions are included. VCXO frequency is 6.552MHz for U.K, and 5.85MHz for Scandinavia. Clock VCXO is 11.648MHz (16 times of 728kHz).

2. PCM decoding stage

   This stage is to get digital sound data from QPSK demodulated digital data stream and apply the data to digital filter. Sound signal decoding, receiving mode display, and sound output selection function are included. De-interleave with SRAM of around 3.5Kbit for frames is built ın.

3. Digital filtering stage

   This is the 2 times over sampling digital filter. (49 order shift adder type) with pass band ripple of less than ±0.1dB, and attenuation less than −40dB.

4. Digital de-emphasis stage

   This is digital de-emphasis circuit meets to CCITT recommendation J.17 with gain error of less than ±0.25dB. DE SEL of I^2C bus (address B4HEX, sub address 1) or DE SEL (pin 44) setting to "H" make this circuit invalided.
   The DESEL is result of OR logic between the terminal of DE SEL (pin 44) and DE SEL of I^2C bus (address B4HEX, sub address 1). So, pin 44 is to be connected to D-GND in case of I^2C bus Control. Or, since the register of I^2C is to be initialized to "L" by Reset, SCL, SDA (pin 42, 43) are to be connected to D-V_{DD} in case of terminal SEL1, SEL2 Control.

5. ΣΔDAC stage

   182 times sampling ΣΔDAC is adopted. This is equivalent to more than 14bit performance. Complementally output is adopted to improve the sound quality (Distortion Characteristics) and requires an external adder circuit consist of 'op-amp', which is used also as LPF.

(2) Explanation for each block

1. AGC

   Pin 7 QPSK signal level fluctuation is to be controlled.

2. Carrier PLL of 6.552MHz

   Control voltage is generated by baseband switching. 90° phase shifter for Det. Phase generating is built in. Signal from AGC circuit is to be detected by 2 detector of 90° phase shifted each, and applied to CH A OUT (Pin 9), CH B OUT (Pin 11) through LPF. These output from pin 9 and pin 11 are coupled with capacitance (DC Cut), applied to CH A IN (Pin 14) and CH B IN (Pin 13). Phase difference of these inputs is detected with analog SW to establish the control loop for the PLL.

3. Clock PLL

   Clock PLL circuit for 11.648MHz, which is 16 times of 728k.

4. Data re-generation circuit

   Data and Clock (5.824MHz, 728kHz Synchronized to Data are generated by differential operation and Pararell to serial conversion. With "H" for O-BS of I^2C resister (address B4HEX, Sub-address 1), Data and Clock (5.824MHz, 728kHz synchronized to Data) can be monitored each by RDATA (Pin 70), MCLK (Pin 68), and RCLK (Pin 62).

5. Sync. circuit

   This stage detects the 8bit sync pattern (FAW-Frame Alignment Word) from QPSK signal from the data re-generation Circuit. And the 'Frame' of 728bits is defined utilizing the 'FAW'. ('FAW'-sync established.) The continuity of the sync pattern is checked. The 'FAW-sync' protection performed with forward 2 frames and backward 6 frames. That is to say the 'FAW-sync' is established in case of synchronization over 2 continuous frames, and is to be canceled in case of a synchronization over 6 continuous frames. After FAW established, the 'C_0-Frame' of 16 frames is defined utilizing the 'C_0 Bit' of the 'Control Bit'. (C_0-synchronization.) And the 'C_0-sync' protection is performed with forward 2 'C_0-Frames' and backward 4 'C_0-Frames'. The $\overline{\text{SERR}}$ (Pin 56) is to be "L" level in case of a synchronized state (as to 'FAW sync' and 'C_0 sync').

6. Descramble circuit

   Built-in PN Code generator works synchronously with the frame by the Frame Sunk Pulse from the sync circuit, and the PN Code of the QPSK demodulated signal is to be rejected.

7. Timing generator

   Generate the various timing signal synchronous with the Frame Sync Pulse from the Sync Circuit.

   Control Bit is detected with the majority-decision over 16 frames (1 C_0 Frame). So, the data is to be refreshed by every 16 frames. And the detected control bit is decoded to be lead to the C_4 (Pin 58), $\overline{\text{MONO2}}$ (Pin 59), $\overline{\text{MONO1}}$ (Pin 60), and $\overline{\text{STEREO}}$ (Pin 61) output.

8. Control Bit Detection Circuit

   Control Bit is detected with the majority-decision over 16 frames (1 C_0 Frame). So, the data is to be refreshed by every 16 frames. And the detected control bit is decoded to be lead to the $\overline{C_4}$ (Pin 58), $\overline{\text{MONO2}}$ (Pin 59), $\overline{\text{MONO1}}$ (Pin 60), and $\overline{\text{STEREO}}$ (Pin 61) output.

9. Address generator, RAM I/O controller

   The de-scrambled signal from the De-scramble Circuit is to be de-interleaved, that is to say the de-scrambled and interleaved signal from the De-scramble Circuit is to be written into the RAM, de-interleaved, and read out from the RAM, and these are to be performed under the Address and timing generated from this Address Generator, RAM I/O Controller. And the 'Write timing', 'Read Timing' for Range Bit Detection, and 'Read timing' for data output to DAC are the time shared. The data thus de-interleaved is to be applied to the processor for scale or error, but also is to be generated as it is from the 'DDATA' (Pin 53) with the timing of the DGATE' (Pin 52) considering the data output in case of the DATA Mode.

10. Range bit detector

    The 'Range Bit' and 'Control Information Bit' multiplied to the 'Parity Bit' are detected by the Majority-decision detection.

11. Parity detector

    The 'Range Bit' and the 'Control Information Bit' multiplied to the 'Parity Bit' are removed with these detected 'Range Bit' and the 'Control Information Bit'. After that, the parity is checked, and the $\overline{\text{PERR}}$ (Pin 55) is to be "L" level in case of error.

12. 10→14bit expander

    10bit data is expanded to 14bit data subject to the 'Range Bit'. Adding the "00" to this 14bit data as the lowest 2bit, the data is to be regarded as total 16bit data.

13. Error correction circuit

    The error found by the Parity Detector is to be corrected by the Average compensation, and the previous value compensation. Former is against discrete error, latter is against a continuous error.

14. Output selector

This stage is to control the output for digital filter subject to control bit C_1, C_2, C_3. from NICAM data stream and SEL1, SEL2. Here, the SEL1, SEL2 are result of OR logic between the terminal of SEL1, SEL2 (Pin 47, 45) and bit for SEL1, SEL2 of I^2C bus (address "B4H", subaddress "0"). So, Pin 47, 45 are to be grounded in case of I^2C bus Control. Or, since the register of I^2C is to be initialized to "L" by Re-set, SCL, SDA (Pin 42, 43) are to be connected to D-V_{DD} in case of terminal SEL1, SEL2 Control.
In case of C_1, C_2, C_3 = 0, 0, 0, that is stereo, the output is controlled to stereo sound for L-ch and R-ch. In case of C_1, C_2, C_3 = 1, 0, 0 that is mono + Data, the output is controlled to monaural sound for both of L-ch and R-ch.
In case of C_1, C_2, C_3 = 0, 1, 0 that is mono 2ch, the output is subject to SEL1, SEL2. Ref to output selection table.
Additionally, in case of SEL1, SEL2 = 1, 1, the digital sound output is forced to be muted.
Selected digital sound signal can be monitored when "H" = 0DI of I^2C (address B4H, sub-address 1).

Terminal "DATA" (Pin 40) : Data
Terminal "LRCLK" (Pin 38) : LR Clock
Terminal "BCK" (Pin 39) : Bit Clock
Synchronized to Data

15. Muting circuit

MUTE OUT (Pin 50) becomes "H" when ;

- Sync Error Occurs.
- Parity Error exceed the criteria in a counting period (around 0.5s).

MUTE OUT due to sync error has 7 frames delay as same as the Sync Error output.
The MUTE activated when parity bit error rate in 512 frames exceeds 1 / 8 (MUTE LVL = 0) or 1 / 16 (MUTE LVL = 1), and released when the error rate decreases to less than 1 / 16 (MUTE LVL = 0) or 1 / 32 (MUTE LVL = 1).
The digital mute function is realized by connecting MUTE OUT (pin 50) and MUTE IN (pin 48). MUTE IN (pin 48) should be grounded ("L") when the digital mute is not required.
This Muting circuit is mute level changeable type. And controlled by the terminal of MUTE LVL (Pin 75) or bit for MUTE LVL (address B4HEX, subaddress 1). The MUTE LVL is result of OR logic between the terminal of MUTE LVL (pin 75) and bit for MUTE LVL of I^2C bus (address B4HEX, subaddress 1). So, pin 75 is to be connected to D-GND in case of I^2C bus control. Or, since register of I^2C is to be initialized to "L" by RESET, SCL, SDA (pin 42, 43) are to be connected to D-V_{DD} in case of terminal MUTE LVL control.

16. I^2C bus control circuit

Read out of Control bit, output selection, mode setting can be executed through I^2C bus interface. Data is transmitted by selecting the register subject to 8bit address and 3bit sub address in data. Synchronously to SCL Clock, data is transferred through SDA.
The register is to be initialized to 00H by "L" input to RESET (pin 67).
Stored once, information is kept stored in the register up to next writing.
Analog output select signal is controlled by FM / PCM (L : FM, H : PCM) OF I^2C bus (address B4HEX, sub address 0). Analog output select signal, put out from FM / PCM (pin 24) is same signal asset by I^2C and control FM / NICAM (pin 23) of TA2047F.

☆ It is required to initialize with RESET (pin 67) of "L" level for start operation. (After power supply)

17. Digital filter circuit

Digital sound signal from the output selection circuit is applied to this stage to be processed by 2 times over sampling digital filtering. Filter has 49th order, shifts data and apples the serial summing, realize the performance of pass band ripple less than ±0.1dB, attenuation less than −40dB.
This digital filter circuit is gain changeable type. And controlled by the terminal of GAIN (pin 73) or bit for GAIN (address B4HEX, subaddress 1). The GAIN is result of OR logic between the terminal of GAIN (pin 73) and bit for GAIN of I^2C bus (address B4HEX, sub address 2). So, pin 1 is to be connected to D-GND in case of I^2C bus control. Or, since register of I^2C is to be initialized to "L" by RESET, SCL, SDA (pin 42, 43) are to be connected to D-V_{DD} in case of terminal GAIN control.
Real output level is maximum level of digital filter in case of control to −3.5dB. And −6dB from maximum output level in case of control to −6dB. When control to −3.5dB, ΣΔDAC has 3.5dB attuenation so not to be overflow, and when control to −6dB ΣΔDAC has no attunation.

18. Digital De-emphasis Circuit

2 times over sampled digital sound signal is processed by CCITT Recommendation J.17 digital de-emphasis. The gain error is less than ±0.25dB. This digital de-emphasis is killed by "H" = DESEL. Here DESEL is result of OR logic between the terminal of DE SEL (pin 44) and bit for DE SEL of I^2C bus (address B4HEX, sub address 1). So 44pin is to be connected to D-GND in case of I^2C bus control. Or, since the register of I^2C is to be initialized to "L" by RESET, SCL, SDA (pin 42, 43) are to be connected to D-V_{DD} in case of terminal DESEL control.

Digital de-emphasised digital sound signal can be monitored when with "H" = O-D_2 of I^2C bus (address B4HEX, sub address 1), O-D_2 of sub address "1".

Terminal "2DATA" (pin 35) : DATA
Terminal "2LRCK" (pin 33) : LR clock
Terminal "2BCK" (pin 34) : bit clock
Synchronized to Data

19. ΣΔDAC

2 times over sampled digital sound signal is interpolated (7 times) and times sampling (13 times) to be 182 times sampled. That is, 1bit ΣΔDAC output of 182 is to be available, which is equivalent to the performance of more than 14bit multi bit type DAC.

To improve distortion characteristics, complementary outputs are applied to DOUTR, $\overline{\text{DOUTR}}$, $\overline{\text{DOUTL}}$, DOUTL (pin 25, 26, 29, 30 each). These are converted to analog signal with external summing circuit TA2047F.

Table. 1 Sound output and display output subject to control bit and sound selection

MODE	CONTROL BIT				SOUND SELECTION		DISPLAY OUTPUT				SOUND OUTPUT	
	C_1	C_2	C_3	C_4	SEL1	SEL2	$\overline{\text{STEREO}}$	$\overline{\text{MONO1}}$	$\overline{\text{MONO2}}$	$\overline{C_4}$	L	R
STEREO	0	0	0	0 / 1	×	×	0	1	1	1 / 0	L	R
					1	1	1	1	1	1	—	—
MONO 2CH	0	1	0	0 / 1	0	0	1	0	0	1 / 0	M1	M1
					0	1	1	0	0	1 / 0	M2	M2
					1	0	1	0	0	1 / 0	M1	M2
					1	1	1	1	1	1	—	—
MONO + DATA	1	0	0	0 / 1	×	×	1	0	1	1 / 0	M	M
					1	1	1	1	1	1	—	—
DATA	1	1	0	0 / 1	×	×	1	1	1	1	—	—
OTHERS	×	×	1	0 / 1	×	×	1	1	1	1	—	—

× ; means "don't care", — ; means "mute"
M1, M ; Data of ODD Frame, M2 ; Data of Even Frame
(Note) SEL1 and SEL2 are result of "OR-Logic" between the terminal of SEL1, SEL2 (pin 47, 45) and bit for SEL1, SEL2 of I^2C bus register.

I²C BUS REGISTER

Address B4HEX (Write register)

MSB							LSB
0	0	0	0	$\overline{FM}$ / PCM	ERMUTE	SEL2	SEL1

$\overline{FM}$ / PCM : FM / PCM select 0→FM, 1→PCM

☆ Analog output select signal is controlled by $\overline{FM}$ / PCM (L : FM, H : PCM) of I²C bus (address B4HEX, sub address 0). Analog output select signal, put out from $\overline{FM}$ / PCM (pin 22) is same signal as set by I²C and control FM / NICAM (pin 23) of TA2047F.

ERMUTE : Digital mute ON / OFF control

0→ON, 1→OFF

SEL1, 2 : Digital sound selection (for mono 2 channel)

00→mono 1 01→mono 2

10→mono 1 / mono 2 11→mute

☆ In case of received signal is mono 2 channel, output signal to digital filter is controlled by the terminal of SEL1, SEL2 (pin 47, 45) or bit for SEL1, SEL2 (address B4HEX, sub address 0). The SEL1, SEL2 are result of OR logic between the terminal of SEL1, SEL2 (pin 47, 45) and bit for SEL1, SEL2 of I²C bus (address B4HEX, sub address 0). So, pin 47 45 are to be connected to D-GND in case of I²C bus control. Or, since register of I²C is to be initialized to "L" by reset, SCL, SDA (pin 42, 43) are to be connected to D-V_{DD} in case of terminal MUTE LVL control.

Address B4HEX (Write register)

MSB							LSB
0	0	1	MUTE LVL	DESEL	O-BS	O-D_1	O-D_2

MUTE LVL : Mute level control

0→ MUTE output becomes "H" when the parity bit error rate exceeds 1 / 8 in 512 frames, and released when the error rate decreases to less than 1 / 16.

1→ MUTE output becomes "H" when the parity bit error rate exceeds 1 / 16 in 512 frames, and released when the error rate decreases to less than 1 / 32.

☆ This muting circuit is mute level changeable type. And controlled by the terminal of MUTE LVL (pin 75) or bit for MUTE LVL (address B4HEX, subaddress 1). The MUTE LVL is result of OR logic between the terminal of MUTE LVL (pin 75) and bit for MUTE LVL of I²C bus (address B4HEX, sub address 1). So, pin 75 is to be connected to D-GND in case of I²C bus control. Or, since register of I²C is to be initialized to "L" by RESET, SCL, SDA (pin 42, 43) are to be connected to D-V_{DD} in case of terminal MUTE LVL control.

DESEL : De-emphasis utility control

0→use, 1→No use

☆ This digital de-emphasis circuit is switchable type. DE SEL of I^2C Bus (address B4HEX, sub address 1) or DE SEL (pin 44) setting to "H" make this circuit invalied.
The DESEL is result of OR logic between the terminal of DE SEL (pin 44) and DE SEL of I^2C Bus (address B4HEX, sub address 1). So, pin 44 is to be connected to D-GND in case of I^2C Bus control. Or, since the register of I^2C is to be initialized to "L" by reset, SCL, SDA (pin 42, 43) are to be connected to D-V_{DD} in case of terminal SEL1, SEL2 control.
In case of digital de-emphasis is off, it is required to use analog de-emphasis by LPF IC, TA2047F. (c.f. Example of application circuit (1), (2))

Test terminal output control
0→Fix to "L", 1→Signal output

0-BS : MCLK, RCLK, RDATA
0-D1 : LRCK, BCK, DATA
0-D2 : 2LRCK, 2BCK, 2DATA

Address B4HEX (Write register)

MSB							LSB
0	1	0	GAIN	SFSEL	I-BS	I-D_1	I-D_2

GAIN : Gain control
0→ – 6dB 1→ – 3.5dB

☆ This digital filter circuit is gain changeable type. And controlled by the terminal of GAIN (pin 73) or bit for GAIN (address B4HEX, subaddress 1). The GAIN is result of OR logic between the terminal of GAIN (pin 73) and bit for GAIN of I^2C bus (address B4HEX, sub address 2). So, pin 1 is to be connected to D-GND in case of I^2C bus control. Or, since register of I^2C is to be initialized to "L" by RESET, SCL, SDA (pin 42, 43) are to be connected to D-V_{DD} in case of terminal GAIN control.

SFSEL : Super frame sync. control
0→All pattern comparison, 1→Edge detection

Test terminal 1 / 0 control
0→Output , 1→Inpput

I-BS : MCLK, RCLK RDATA
I-D1 : LRCK, BCK, DATA
I-D2 : 2LRCK, 2BCK, 2DATA

☆ Test terminal 1 / 0 control (Sub address 2) is prior to Test terminal output control (Sub address 1).

☆ "0" shall be put into poen bit above register.

☆ Sub address bit combination other than above must not be applied. (That is to be used for IC inspection)

Address B5HEX (Read register)

MSB							LSB
C_1	C_2	C_3	C_4	SERR	MUTE0	CIB1	CIB2

C1-4 : Control bit
SERR : Sync. error flag
0→Sync. error, 1→Synchronized
MUTE0 : Digital mute flag
0→Normal, 1→Mute
CIB1, 2 : Control information flag

☆ It is required to initialize write register with $\overline{\text{RESET}}$ (pin 67) of "L" level for start operation.

☆ Sub address bit combination other than the above must not be applied. (That is to be used for IC inspection)

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}, V_{DD}	V_{SS}~V_{SS} + 6.0	V
Input Voltage	V_{IN}	− 0.3~V_{CC}, V_{DD} + 0.3	V
Power Dissipation	P_D	1900 (Note 1)	mW
		900 (Note 2)	
Storage Temperature	T_{stg}	− 55~125	°C

(Note 1) Derated above Ta = 25°C in the proportion of 19.0mW / °C. [TB1212N (64pin SDIP Package)]
(Note 2) Derated above Ta = 25°C in the proportion of 9.0mW / °C. [TB1212F (80pin QFP Package)]

RECOMMENDABLE OPERATING CONDITION

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	—	—	4.5	5.0	5.5	V
Input Voltage	V_{IN}	—	—	0	—	V_{DD}	V
Operting Temperature	T_{opr}	—	—	− 20	—	65	°C

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (Ta = 25°C, V_{CC}, V_{DD} = 5.0V)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Consumption Current		I_{CC}	—	—	15	35	55	mA
Consumption Current		I_{DD}	—	—	5	15	35	mA
Power Dissipation		P_D	—	—	90	250	495	mW
Input Voltage	High Level	V_{IH}	—	(*1)	4.0	—	—	V
	Low Level	V_{IL}	—	(*1)	—	—	1.0	V
Hysterisis Width		V_H	—	(*2)	—	0.6	—	V
Input Current	High Level	I_{IH}	—	V_{IH} = D V_{DD} (*1)	—	—	10	μA
	Low Level	I_{IL}	—	V_{IL} = D GND (*1)	− 10	—	—	μA
Output Voltage	High Level	V_{OH1}	—	I_{OH} = − 2.0mA (*3)	4.0	—	—	V
	Low Level	V_{OL1}	—	I_{OL} = 2.0mA (*3)	—	—	0.4	V
	High Level	V_{OH2}	—	I_{OH} = − 4.0mA (*4)	4.0	—	—	V
	Low Level	V_{OL2}	—	I_{OL} = 4.0mA (*4)	—	—	0.4	V

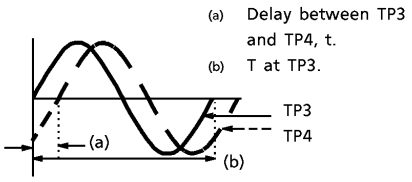
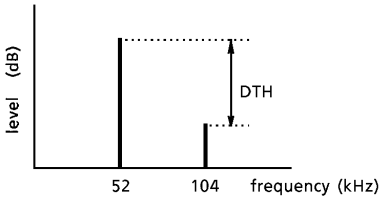
(*1) For GAIN, MUTE LVL, SCL, SDA, DE SEL, SEL2, SEL1, MUTE IN, TEST3, TEST2, TEST1, $\overline{\text{RESET}}$

(*2) SCL, SDA, $\overline{\text{RESET}}$

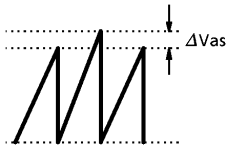
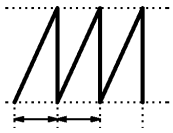
(*3) 2LRCK, 2BACK, 2DATA, LRCK, BCK, DATA, SDA, MUTE OUT, DGATE, DDATA, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, MCLK, RCLK, RDATA, $\overline{\text{FM}}$ / PCM

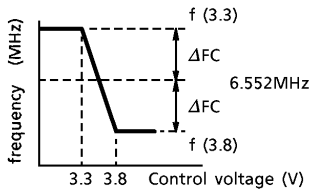
(*4) $\overline{C_4}$, $\overline{\text{MONO2}}$, $\overline{\text{MONO1}}$, $\overline{\text{STEREO}}$

AC CHARACTERISTIC (1) (Ta = 25°C, V_{CC}, V_{DD} = 5.0V)

TEST ITEM	SYM-BOL	TEST CIR-CUIT	SWITCH 4	5	6	8	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
AGC Flat Level	eF	—	b	b	off	a	(1) Apply 6.5MHz, 200mV$_{p-p}$ CW to pin 7. (*A) (2) Measure amplitude at TP4.	0.4	0.7	1.0	V$_{p-p}$
AGC Flat Level vs Power Supply	eFV	—	b	b	off	a	(1) Apply 6.5MHz, 200mV$_{p-p}$ CW to pin 7. (*A) (2) Measure eF at $V_{CC} = V_{DD}$ = 4.5V and 5.5V eFV = ((eF (5.5V) – eF (4.5V)) / eF	– 10	—	10	% / V
AGC Flat Level vs Temperature	eFT	—	b	b	off	a	(1) Apply 6.5MHz, 200mV$_{p-p}$ CW to pin 7. (2) Measure eF at Ta = – 20°C and 65°C eFT = ((eF (65°C) – eF (– 20°) / eF)) / 85	– 0.1	—	0.1	% / °C
AGC Control Characteristics	A	—	b	b	off	a	(1) Apply 6.5MHz, 100mV$_{p-p}$ / 400mV$_{p-p}$ CW to pin 7. (*A) (2) Measure Amplitude at TP4. A = 100 × (eF – eF (100mV) / eF, and A = 100 × (eF – eF (400mV) / eF	– 10	0	10	%
Output Level Dev.	ΔEO	—	b	b	off	a	(1) Apply 6.5MHz, 200mV$_{p-p}$ CW to pin 7. (2) Measure Amplitude at TP3 and TP4. ΔE0 = eF (TP4) – eF (TP3)	– 100	—	100	mV
Relative Dev. Phase	ϕb	—	b	b	off	a	(1) Apply 6.5MHz, 200mV$_{p-p}$ CW to pin 7. ϕb = (t / T) × 360 – 90 	– 10	0	10	°
2nd Order Distortion	DTH	—	b	b	off	a	(1) Apply 6.5MHz, 200mV$_{p-p}$ CW to pin 7. (2) Measure level difference between the fundamentals and the 2nd harmonics. 	—	– 50	—	dB

(*A)Clock VCXO OFF (CL-VCXO-I2 (Pin 1) connect to GND)

TEST ITEM	SYM-BOL	TEST CIR-CUIT	SWITCH 4	SWITCH 5	SWITCH 6	SWITCH 8	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Demodulate Output Residual Carrier Wave	eCW	—	b	b	off	a	(1) Apply 6.5MHz, 200mV$_{p-p}$ CW to pin 7. (2) Measure level difference between 52kHz and 6.5MHz component.	—	−50	—	dB
Analog SW Sencitivity	Gs	—	a	a	off	a	(1) Apply 10kHz, 0.7V$_{p-p}$ CW to TP6 and TP7 with 90° phase difference. (2) Measure pin 19 output. $Gs = \frac{mV_{p-p}}{90°}$ 	3.0	4.5	6.0	mV/°
Analog SW Output Level Dev.	ΔVas	—	a	a	off	a	(1) Apply 10kHz, 0.7V$_{p-p}$ CW to TP6 and TP7 with 90° phase difference. (2) Measure peak level difference at pin 13 	0	—	20	mV
Analog SW Cycle Ratio	RTB	—	a	a	off	a	(1) Apply 10kHz, 0.7V$_{p-p}$ CW to TP6 and TP7 with 90° phase difference. (2) RTB is the ratio of the max. period and the min. perdiod. 	0.8	1.0	1.2	—
QPSK Input Level	Qin	—	b	b	off	a	(1) Apply 1kHz QPSK modulated signal to QPSK IN. (2) Monitor "Eye Pattern" by changeing the QPSK input level. (Note) Recommended input level to untilize AGC function is 0.1~0.4V$_{p-p}$.	0.1	0.8	2.0	V$_{p-p}$

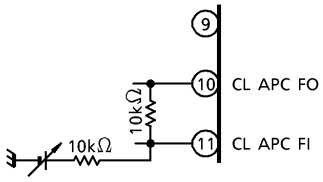
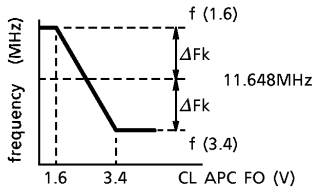
TEST ITEM	SYM-BOL	TEST CIR-CUIT	SWITCH 4	5	6	8	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Carrier VCXO Control Range	ΔFC	—	b	b	on	a	(1) Applying 3.3~3.8V DC as Control Voltage at CA APC DC. (2) Measure Control Range of Carrier VCXO Frequency. (*B) ΔFC = 6.552 – f (3.3) = 6.552 – f (3.8) 	± 1.5	± 2.0	—	kHz
Carrier VCXO Frequency vs Power Supply	ΔFCV	—	b	b	off	a	(1) Apply 6.5MHz, 200mV$_{p-p}$ CW to pin 7. (2) Measure carrier VCXO frequency at $V_{CC} = V_{DD} = 4.5$~5.5V. (*B) ΔFCV is the max. frequency change.	– 2000	0	2000	Hz
Carrier VCXO Frequency vs Temperature Characteristics	ΔFCT	—	b	b	off	a	(1) Appiy 6.5MHz, 200mV$_{p-p}$ CW to pin 7. (2) Measure carrier VCXO frequency at Ta = – 20~65°C. (*B) ΔFCV is the max. frequency deviation from 25°C value.	—	—	400	Hz
Carrier Regeneration PLL Pull-in Rage.	fpcQ	—	b	b	off	a	(1) Appiy 6.5MHz, 200mV$_{p-p}$ CW to pin 7. (2) Sweep pin 7 frequency and note pull-in and hold lange. (*B)	± 600	± 1000	—	Hz
Carrier Regeneration PLL Hold Range	fhcQ	—	b	b	off	a		± 600	± 1000	—	Hz

(*B) Method of measureing Carrier VCXO frequency.

(1) Stop the Clock VCXO oscilator. (Connect CL-VCXO-I2 (pin 1) to GND)

(2) Apply 6.5MHz, 200mV$_{p-p}$ CW to pin 7.

(3) Measure frequency at TP4 (CH-A-OUT (pin 9)).
This is difference between input frequency (6.552MHz) and carrier VCXO frequency.

TEST ITEM	SYM-BOL	TEST CIR-CUIT	SWITCH 4	5	6	8	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Clock VCXO Control Rage	ΔFk	—	b	b	off	a	(1) Measure control range of Clock VCXO frequency by applying control voltage CL-APC-F (pin 16) through a 10kΩ resistor. (2) This control voltage is 1.6~3.4V DC at CL-APC-FO (pin 4).  (3) Measure frequency difference between Clock VCXO frequency and 11.648MHz. ΔFk = 11.648 – f (1.6) = 11.648 – f (3.4) 	± 1.5	± 2.0	—	kHz
Clock VCXO Frequency vs Power Supply	ΔFkV	—	b	b	off	a	Measure Clock VCXO frequency at $V_{CC} = V_{DD} = 4.5$~$5.5V$. (*C) ΔFKV is the max. frequency change.	– 2000	0	2000	Hz / V
Clock VCXO Frequency Temp. Characteristics	ΔFkT	—	b	b	off	a	Measure Clock VCXO frequency at Ta = – 20~65°C. (*C) ΔFKT is the max. frequency change.	—	—	± 300	Hz
Clock Regeneration PLL Hold Range	fpk	—	a	a	off	a	(1) Apply 364kHz, $0.7V_{p-p}$ CW to TP6. (2) Sweep TP6 frequency and note pull-in and hold range. (*C)	± 2000	± 3000	—	Hz
Clock Regeneration PLL Pull-in Range	fhk	—	a	a	off	a		± 2000	± 3000	—	Hz

(*C) Method of measuring Clock VCXO frequency.

(1) Output test signal to MCLK (pin 68) by O-BS of I^2C (address B4H, sub-address 1).

(2) This test signal's frequency is half of clock VCXO frequency

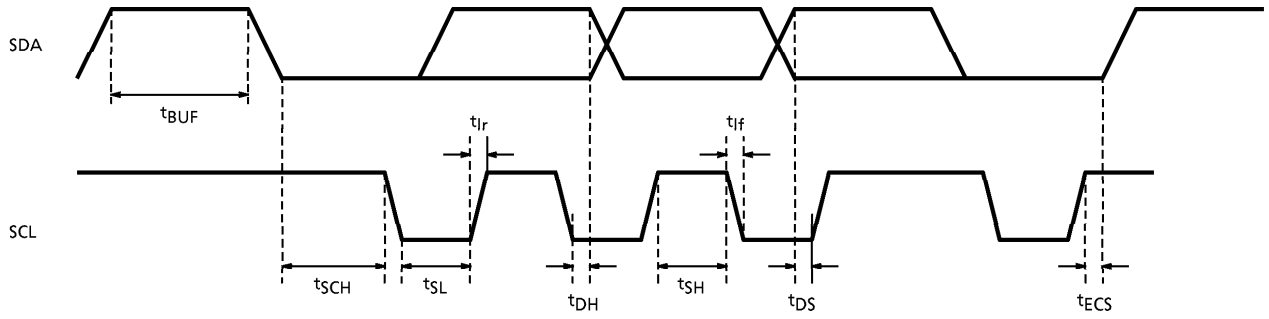
AC CHARACTERISTIC (2)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
SCL Clock Frequency	f_{SCL}	—	$f_{SCL} = 1 / TSCL$	0	—	100	kHz
SCL High Level	t_{SH}	—	$C_L = 400pF$	4.0	—	—	μs
SCL Low Level	t_{SL}	—	$C_L = 400pF$	4.7	—	—	μs
Data Setup Time	t_{DS}	—	$C_L = 400pF$	250	—	—	ns
Data Hold Time	t_{DH}	—	$C_L = 400pF$	5.0	—	—	μs
Transmittion Start Condition Hold Time	t_{SCH}	—	$C_L = 400pF$	4.0	—	—	μs
Transmittion Stop Condition Hold Time	t_{ECS}	—	$C_L = 400pF$	4.7	—	—	μs
Data Transmittion Interval	t_{BUF}	—	$C_L = 400pF$	4.7	—	—	μs
I^2C Time	t_{Ir}	—	$C_L = 400pF$	—	—	1.0	μs
I^2C Fall Time	t_{If}	—	$C_L = 400pF$	—	—	300	ns

AC CHARACTERISTIC (3)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Digital Filter Pass Band Width Ripple	D_{Fpr}	—	—	—	0.2	—	dB
Digital Filter Pass Band	D_{Fpb}	—	GAIN −1dB frequency	—	15.0	—	kHz
Digital Filter Attenuation	D_{Frr}	—	—	—	−40.0	—	dB
Digital De-emphasis Characteristics Error	D_{Eer}	—	—	—	0.5	—	dB

I^2C BUS TIMING CHART



Purchase of TOSHIBA I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

X'tal Specification

(1) 11.648MHz

Maker	:	TOKYO DENPA COMPANY, LTD.	
Type	:	TR49 (11.648MHz)	
Specification	:	load capacity	LC = 16pF
		temperature characteristic	±30ppm (– 10 to 70°C)
		frequency deviation	RT = ±30ppm
		resistance	CI = 25Ω
		parallel capacity	CO = ~7.0pF

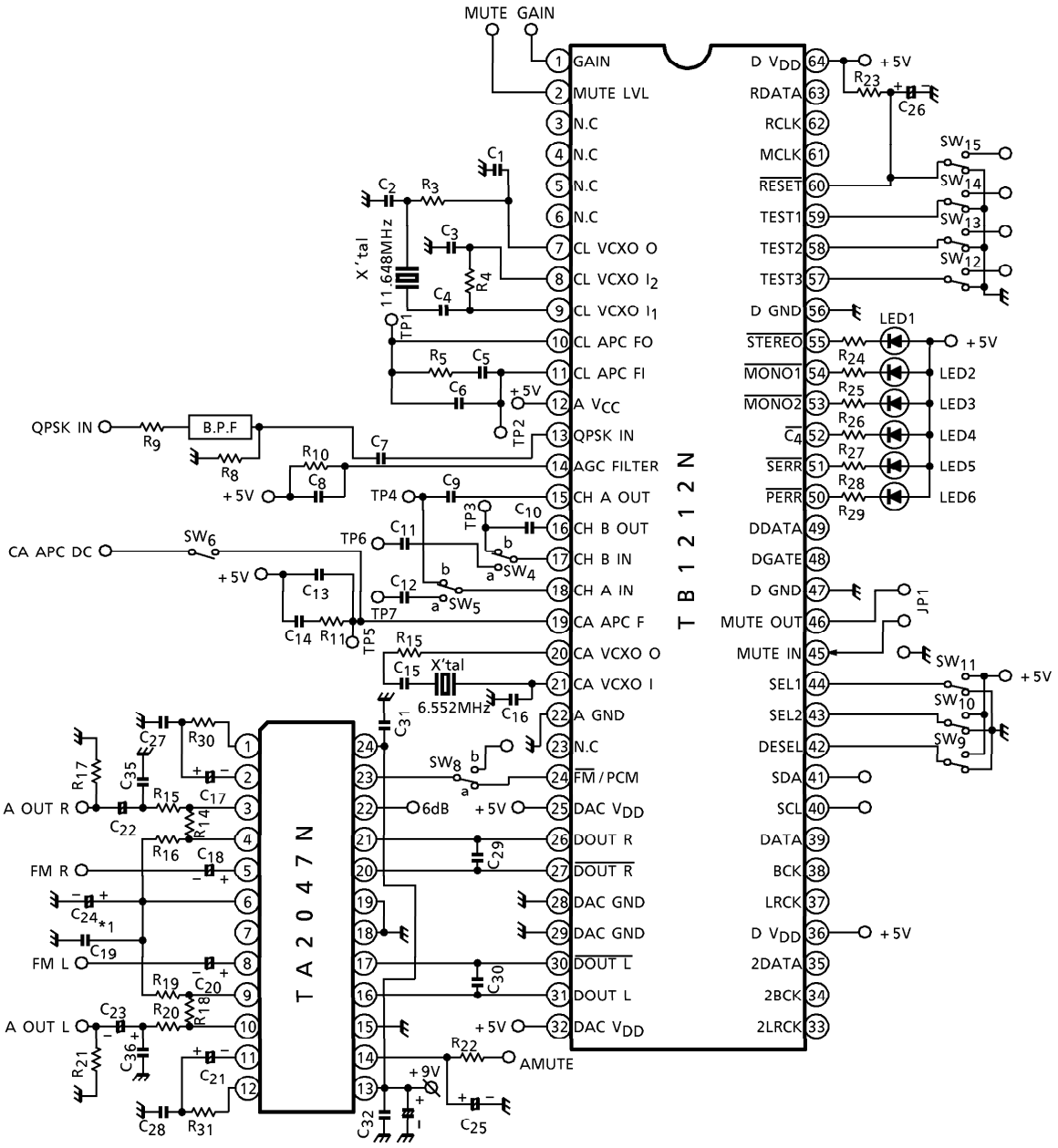
(2) 6.552MHz

Maker	:	TOKYO DENPA COMPANY, LTD.	
Type	:	TR49 (6.552MHz)	
Specification	:	load capacity	LC = 16pF
		temperature characteristic	±30ppm (– 10 to 70°C)
		frequency deviation	RT = ±30ppm
		resistance	CI = 50Ω
		parallel capacity	CO = ~7.0pF

(3) 5.85MHz

Maker	:	TOKYO DENPA COMPANY, LTD.	
Type	:	TR49 (5.85MHz)	
Specification	:	load capacity	LC = 16pF
		temperature characteristic	±30ppm (– 10 to 70°C)
		frequency deviation	RT = ±30ppm
		resistance	CI = 50Ω
		parallel capacity	CO = ~7.0pF

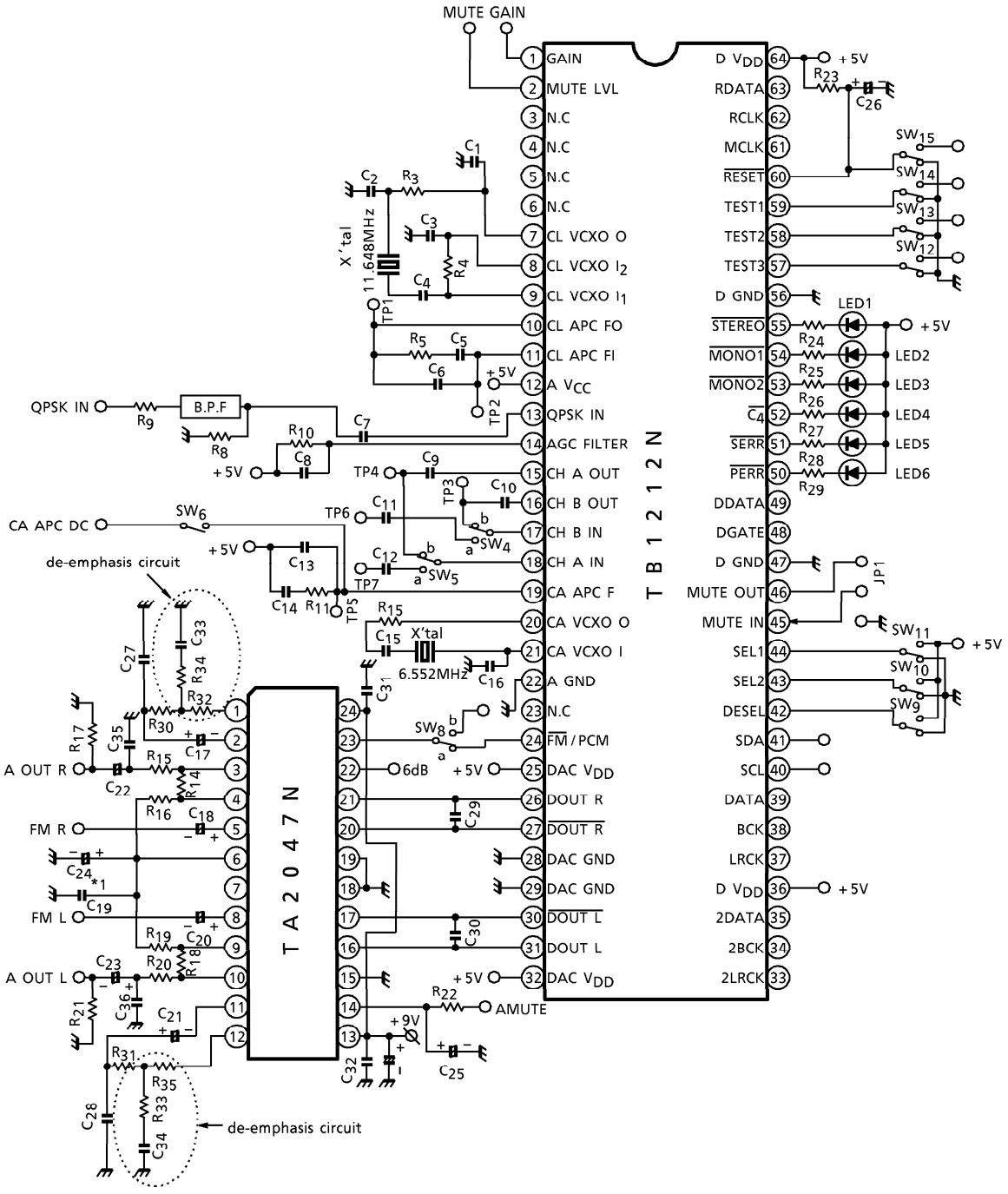
TEST CIRCUIT 1 (Digital de-emphasis)



About TA2047N

1. It is require to connect ceramic or film condenser not to receive temperature characteristics. (*1)
2. Pin 7 to be open. (Don't connect to GND or V_{CC})
3. It is require to other writing GND line of pin 18, 19 and pin 15.
4. C_{38} connect between pin 6 and pin 15.

TEST CIRCUIT 2 (Analog de-emphasis)

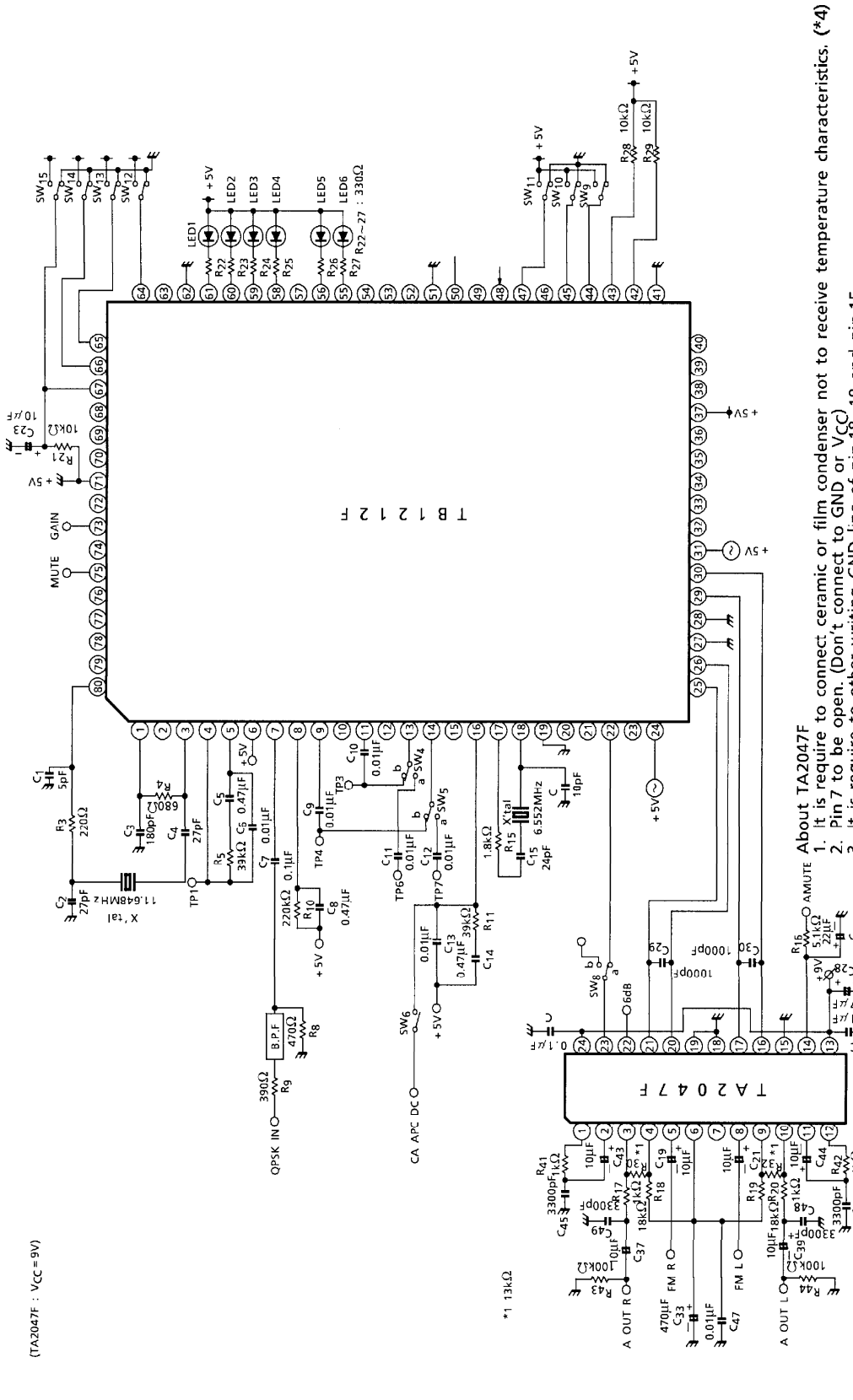


About TA2047N

1. It is require to connect ceramic or film condenser not to receive temperature characteristics. (*1)
2. Pin 7 to be open. (Don't connect to GND or V_{CC})
3. It is require to other writing GND line of pin 18, 19 and pin 15.
4. C_{38} connect between pin 6 and pin 15.

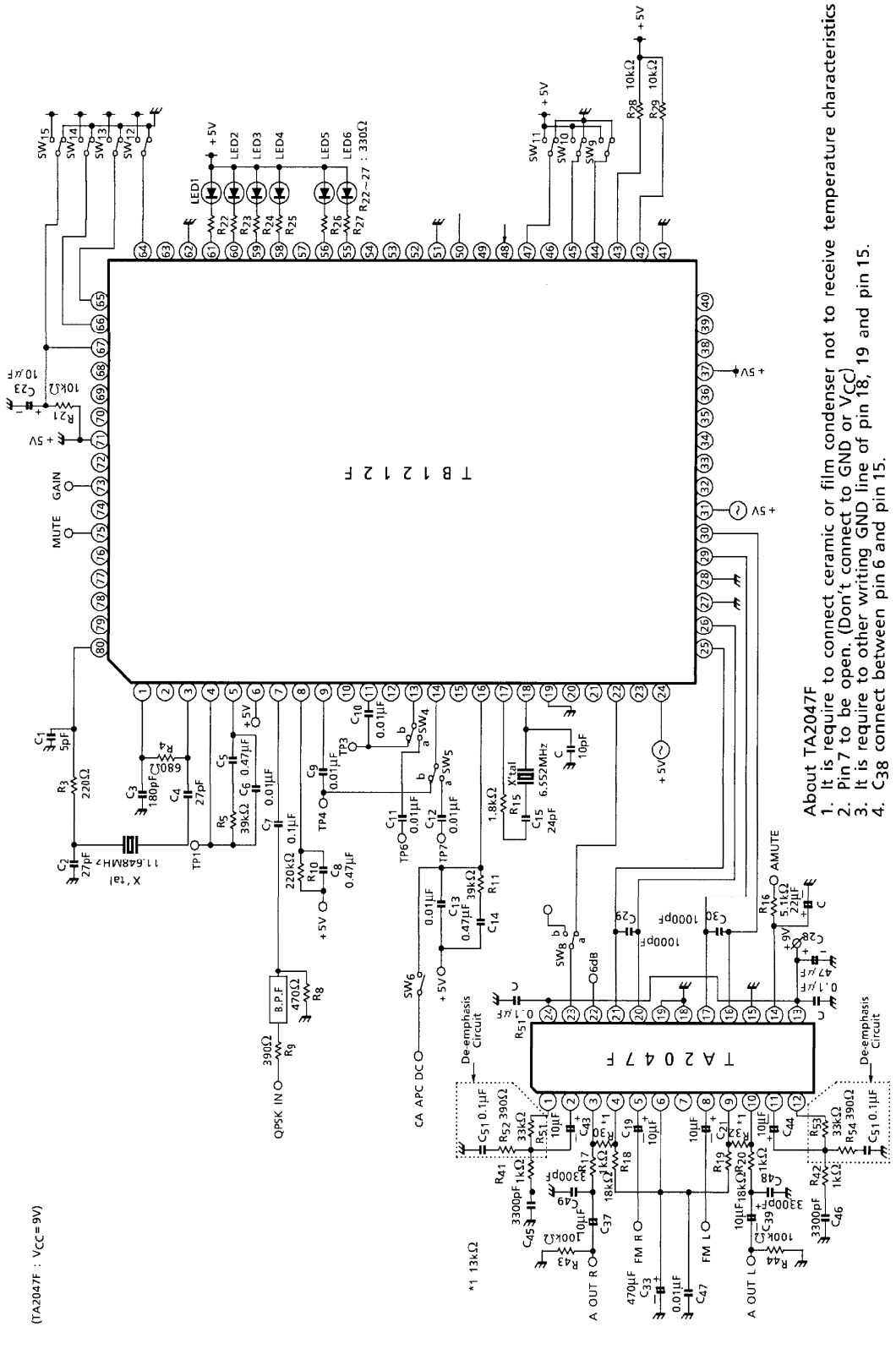
TEST CIRCUIT 3 (Digital de-emphasis)

(TA2047F : V_{CC} = 9V)



TEST CIRCUIT 4 (Analog de-emphasis)

(TA2047F : V_{CC} = 9V)



About TA2047F
1. It is require to connect ceramic or film condenser not to receive temperature characteristics (*1)
2. Pin 7 to be open. (Don't connect to GND or V_{CC})
3. It is require to other writing GND line of pin 18, 19 and pin 15.
4. C_{38} connect between pin 6 and pin 15.

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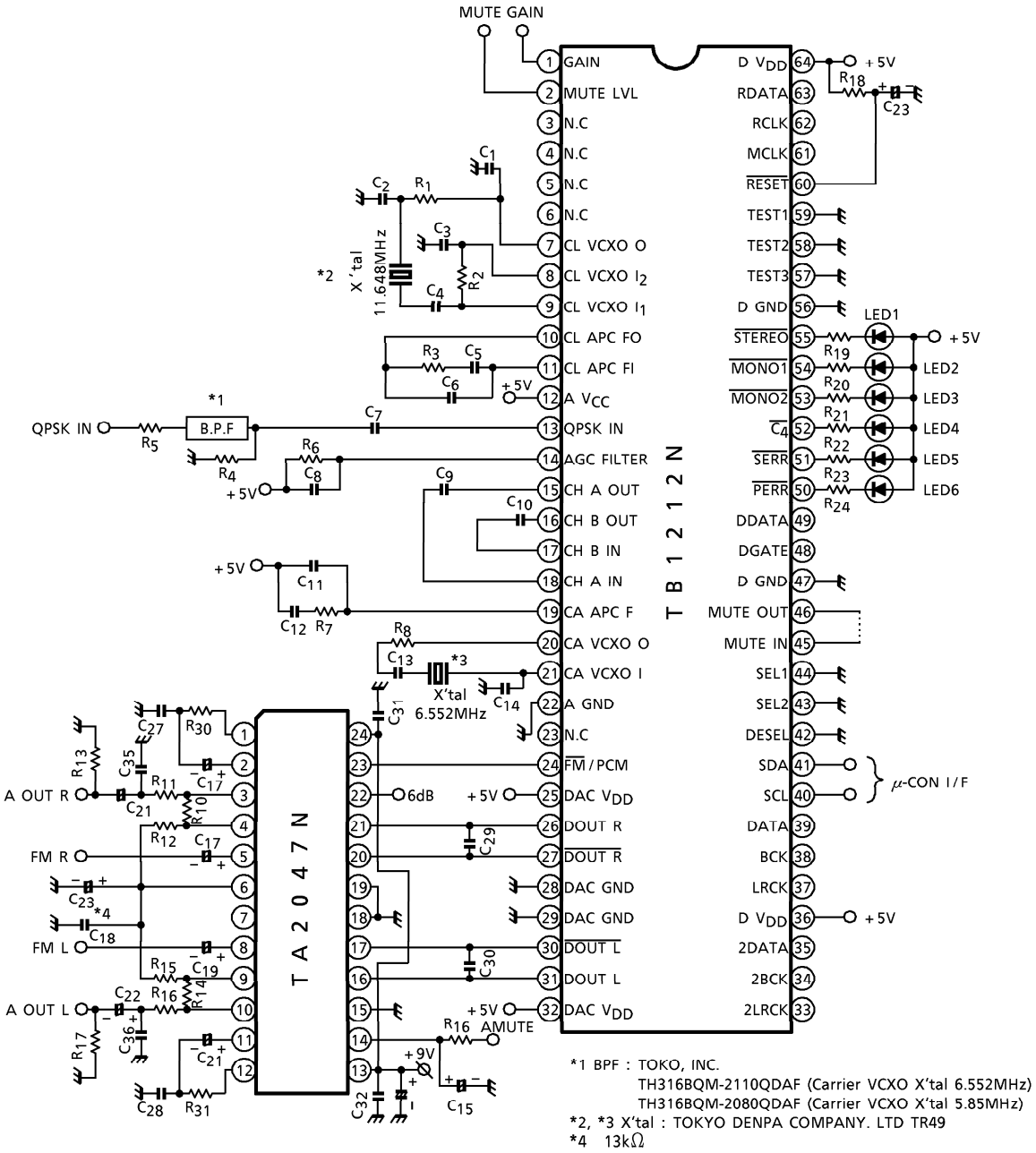
APPLICATION CIRCUIT 1 (Digital de-emphasis)

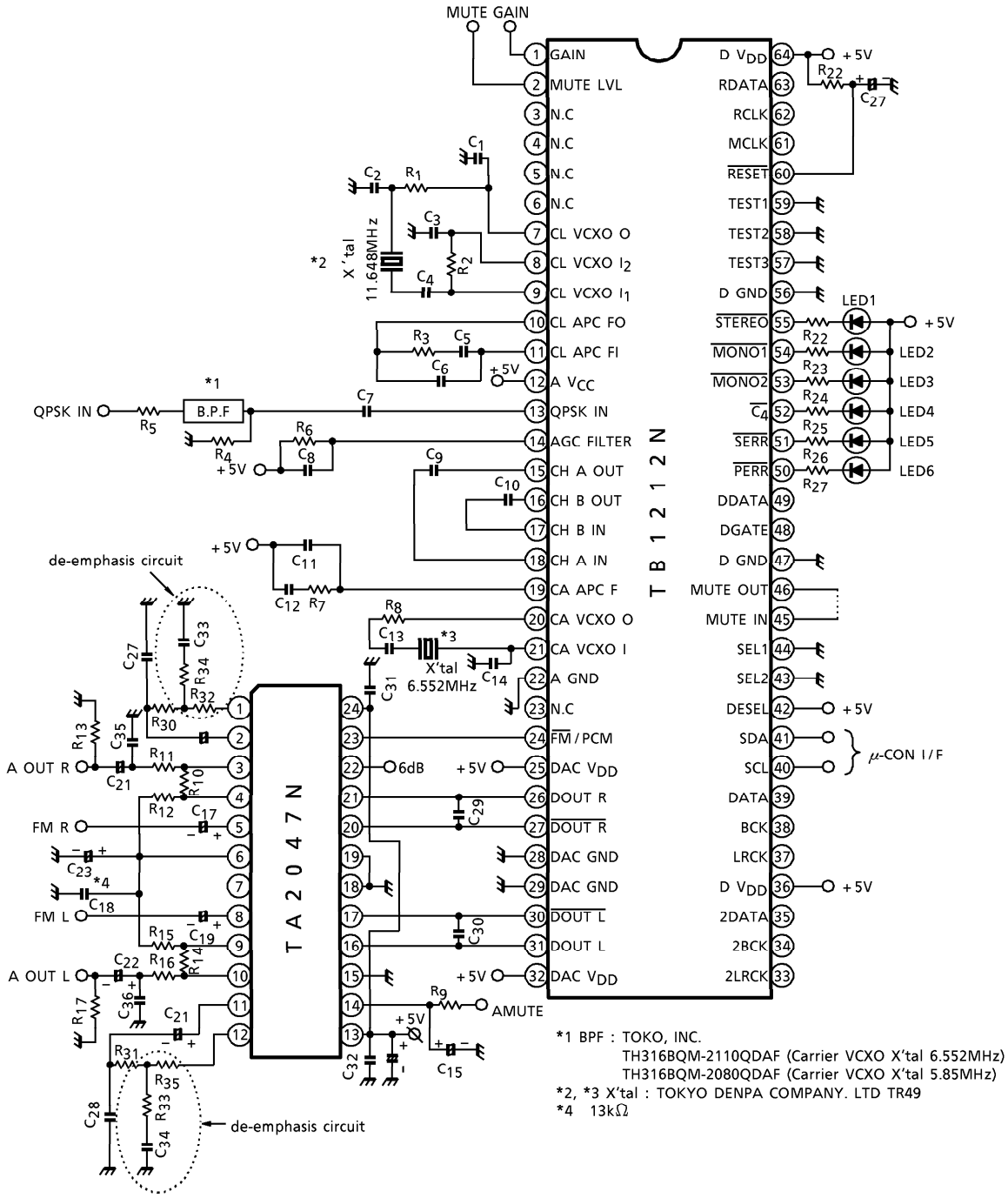


*1 BPF : TOKO, INC.
TH316BQM-2110QDAF (Carrier VCXO X'tal 6.552MHz)
TH316BQM-2080QDAF (Carrier VCXO X'tal 5.85MHz)
*2, *3 X'tal : TOKYO DENPA COMPANY. LTD TR49
*4 13kΩ

About TA2047N

1. It is require to connect ceramic or film condenser not to receive temperature characteristics. (*4)
2. Pin 7 to be open. (Don't connect to GND or V_{CC})
3. It is require to other writing GND line of pin 18, 19 and pin 15.
4. C_{38} connect between pin 6 and pin 15.

APPLICATION CIRCUIT 2 (Analog de-emphasis)

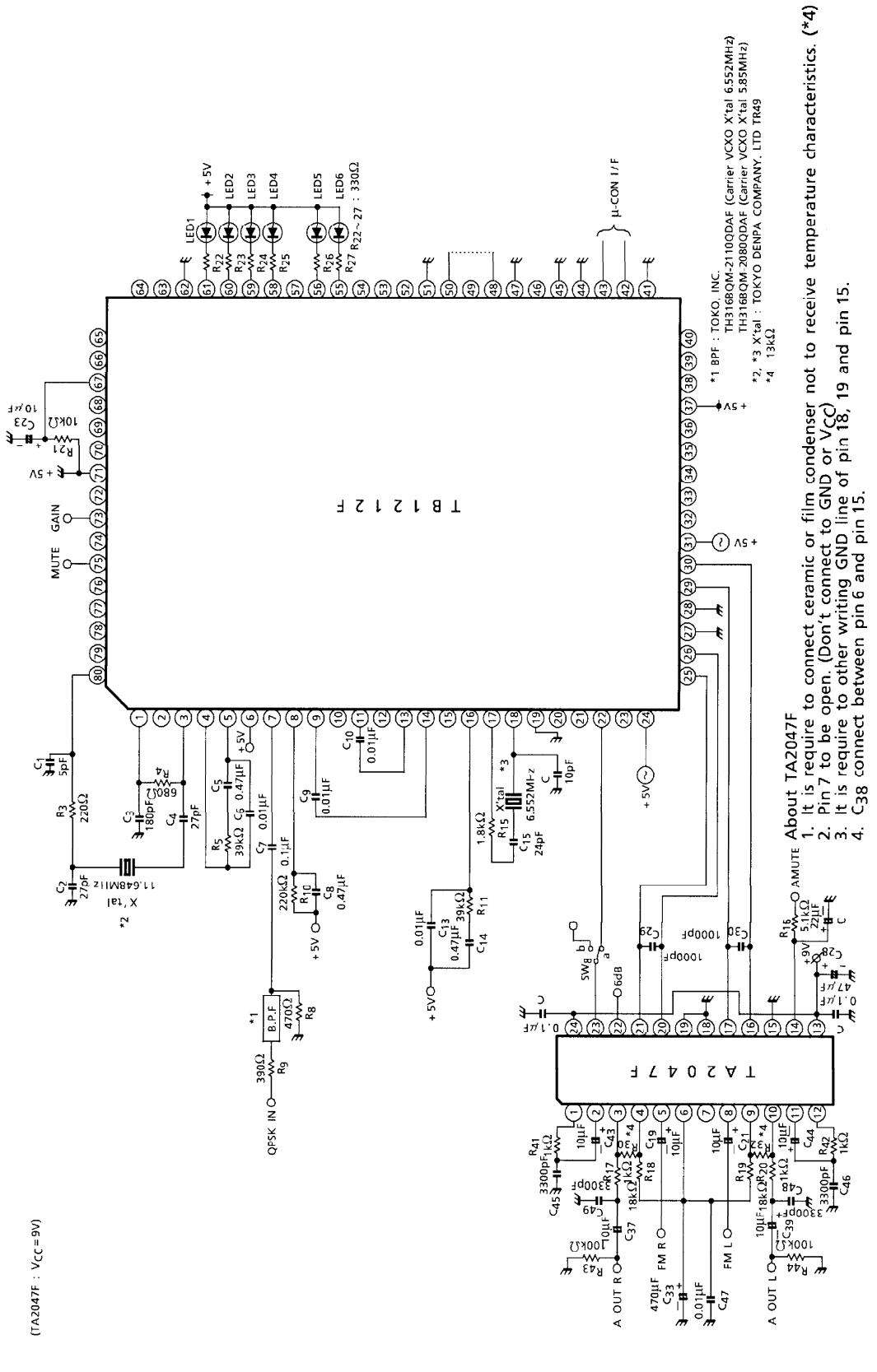


About TA2047N

1. It is require to connect ceramic or film condenser not to receive temperature characteristics. (*4)
2. Pin 7 to be open. (Don't connect to GND or V_{CC})
3. It is require to other writing GND line of pin 18, 19 and pin 15.
4. C_{38} connect between pin 6 and pin 15.

APPLICATION CIRCUIT 3 (Digital de-emphasis)

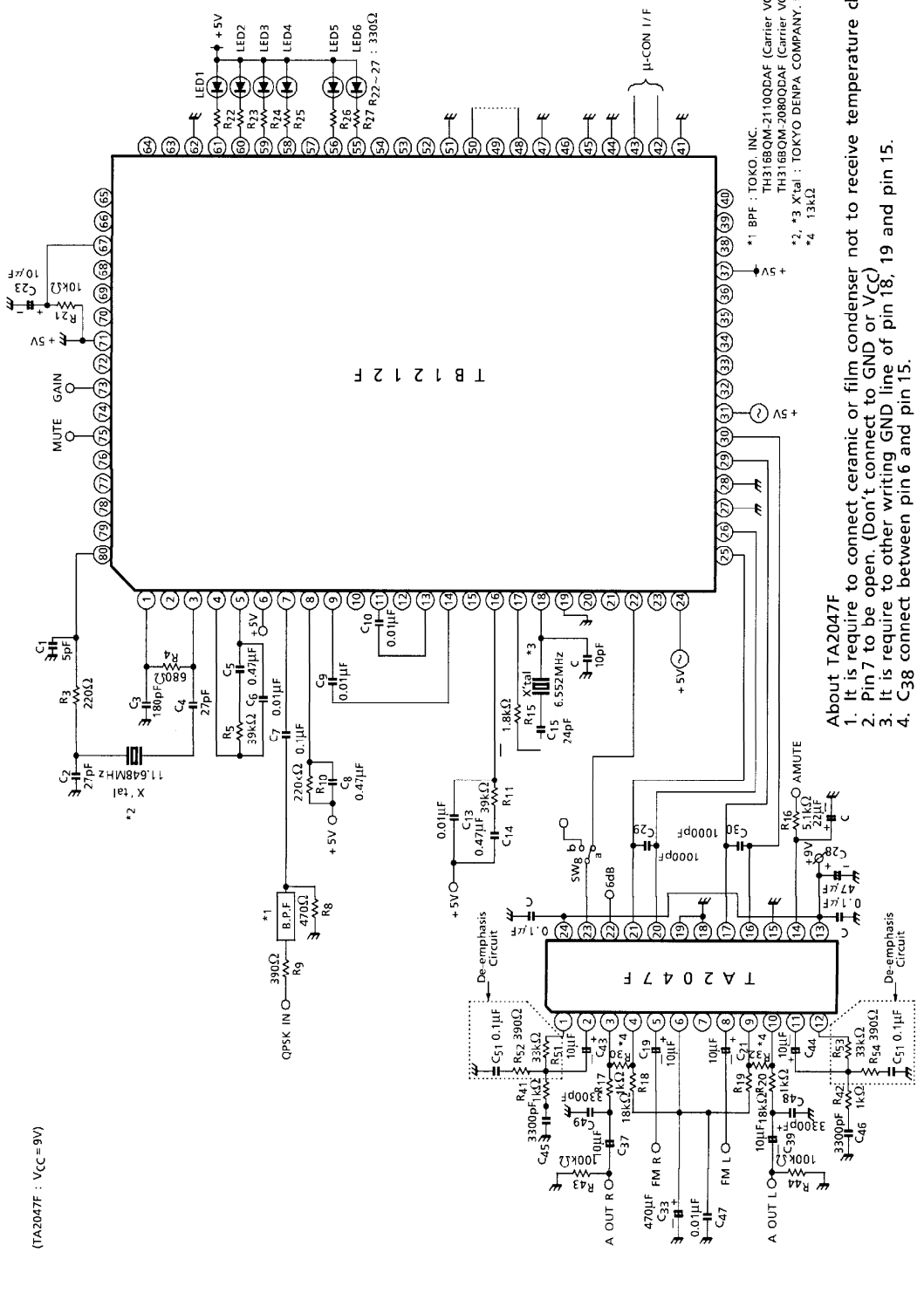
(TA2047F : V_{CC} = 9V)



TB1212N/F—30

APPLICATION CIRCUIT 4 (Analog de-emphasis)

(TA2047F : V_{CC} = 9V)



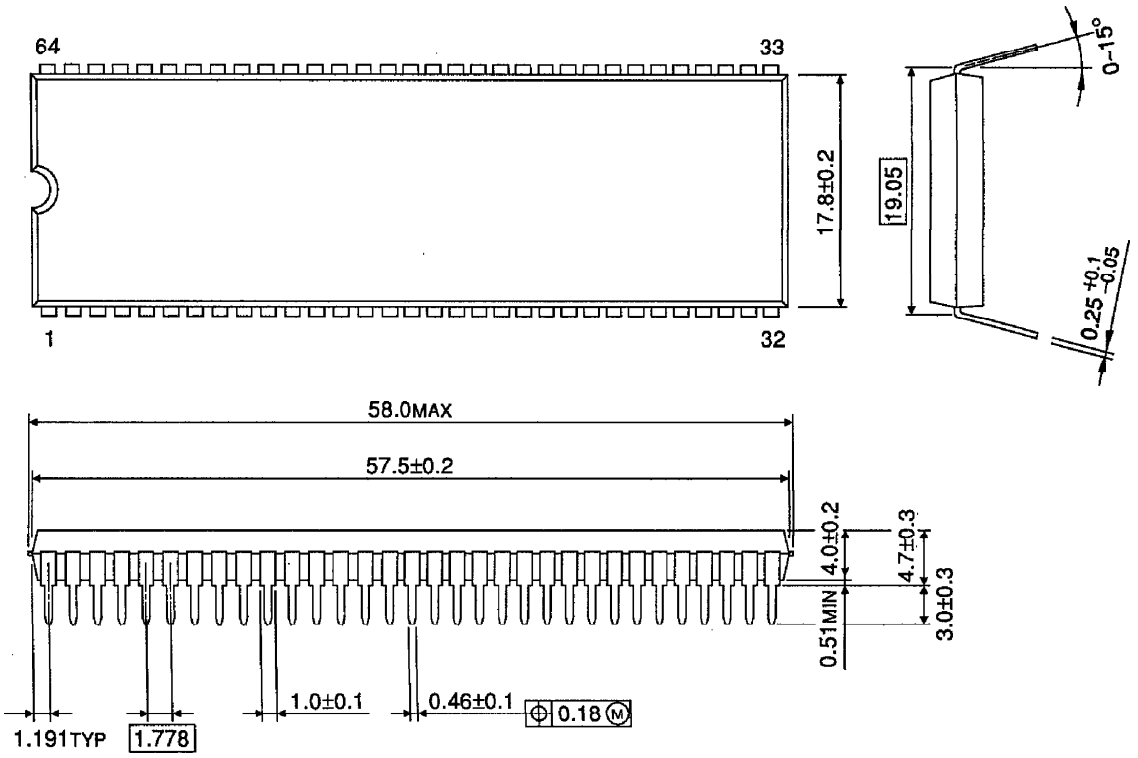
About TA2047F

1. It is require to connect ceramic or film condenser not to receive temperature characteristics. (*4)
2. Pin 7 to be open. (Don't connect to GND or V_{CC})
3. It is require to other writing GND line of pin 18, 19 and pin 15.
4. C_{38} connect between pin 6 and pin 15.

TB1212N/F—31

OUTLINE DRAWING

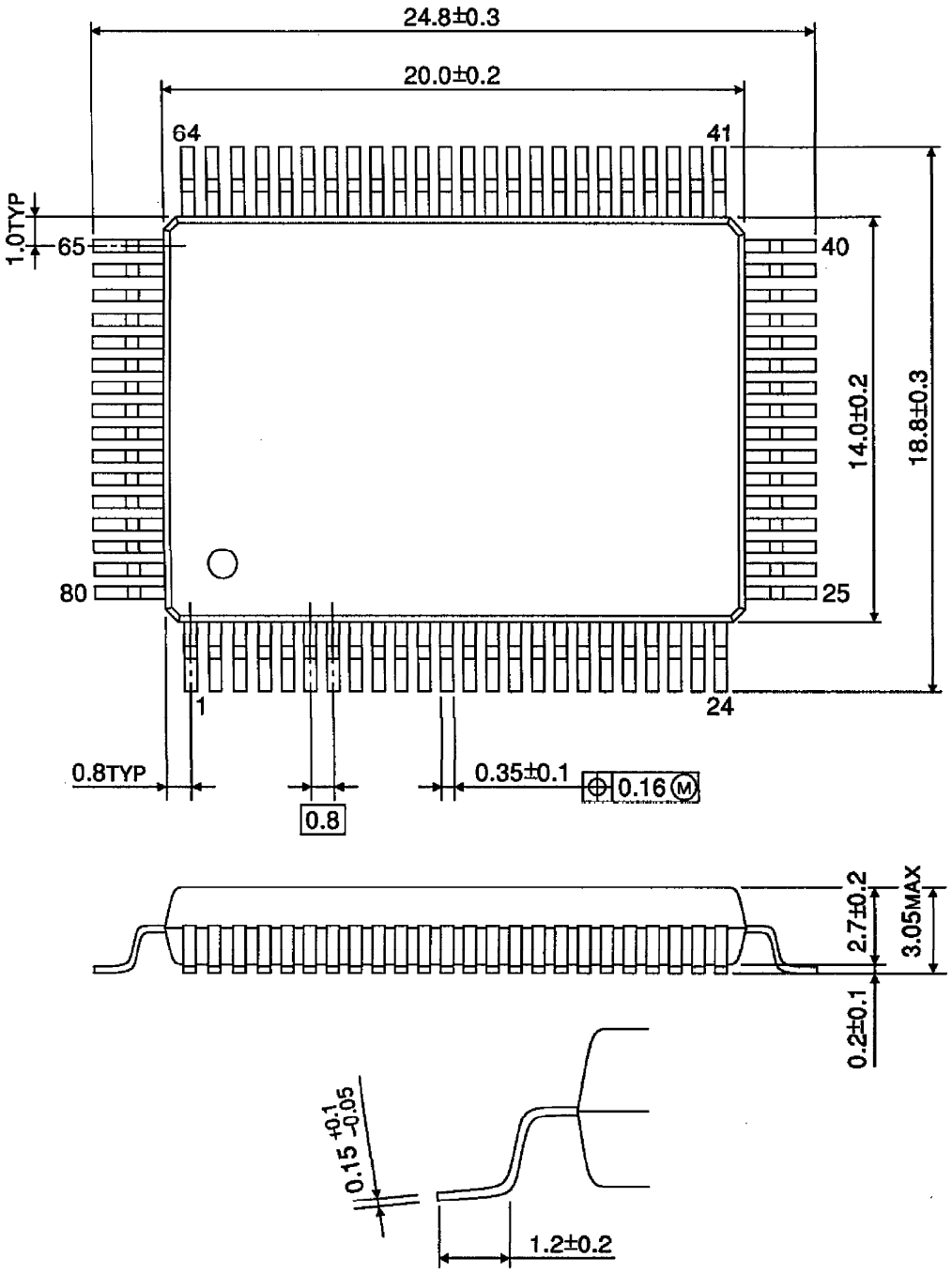
SDIP64-P-750-1.78 Unit : mm



Weight : 8.85g (Typ.)

OUTLINE DRAWING

QFP80-P-1420-0.80A Unit : mm



Weight : 1.6g (Typ.)