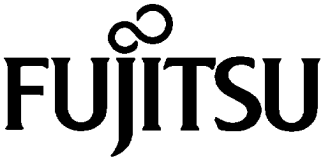
MPEG2 1chip Audio/Video Encoder
MB86391 Product Specification

Revision 1.1
12, November 2001



Contents

1 Overview

1.1 Product Overview

The MB86391 (MPEG2 1chip Audio/Video Encoder) is an LSI that accomplishes all of video encoding, audio encoding, and video and audio encode stream data multiplexing with a single chip rather than several LSIs as in the past. This LSI enables you to minimize the size, cost and power consumption of MPEG2 application systems, such as digital video recorders.

An easy control command interface is achieved by firmware dedicated to the internal controller.

1.2 System Configuration

Fig. 1.2 shows an example system configuration using the MB86391.

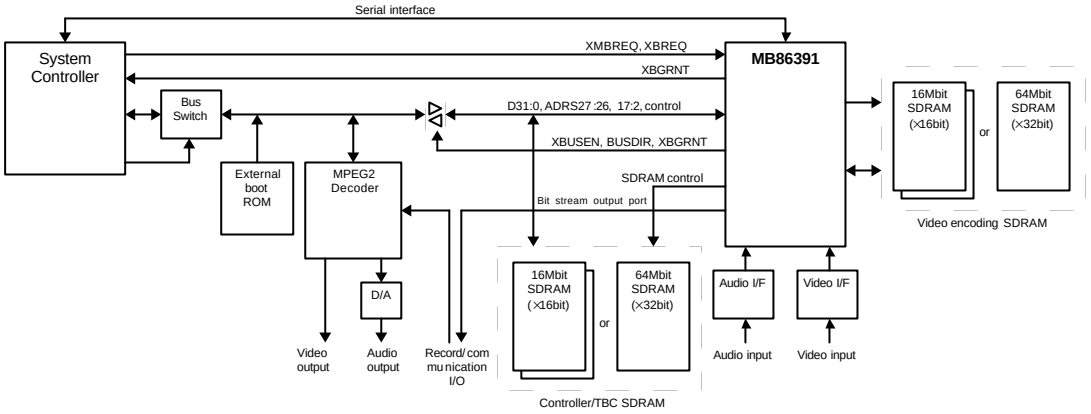


Fig. 1.2 : System configuration (Example))

1.3 Specification Overview

1.3.1 Major Items

Table 1.3.1 : Major items

Model	MB86391
Function	MPEG2 1chip Audio/Video encoder
Operating frequency	54MHz (27MHz for some) [27MHz input clock frequency, 54MHz clock generated by internal PLL]
Technology	0.18µm, Al 4 layers
Supply voltage	I/O 3.0 to 3.6V, Internal 1.65 to 1.95V
Power consumption	T.B.D
Operating temperature	Ta = -20 to 85°C
Package	208pin HQFP(FPT−208P−M04)

1.3.2 Function List

Table 1.3.2 : Function list

Video encoder	Encoding	Compliant to ISO/IEC13818−2 (MPEG2 video)MP@ML and ISO/IEC11172−2 (MPEG1 video)
	Screen size	When interlacing at 29.97Hz Compatible with size 32m×32n less than 720×480 (m, n : any integers) When interlacing at 25Hz : Compatible with size 32m×32n less than 720×576 (m, n : any integers)
	Video input interface	D1 8bit parallel, YC multiplex 8bit parallel
	Bit rate	Max. 15Mbps
Audio encoder	Encoding method	ISO/IEC11172−3 (MPEG1 audio) layer 1/2−compliant
	Sampling frequency	32kHz, 44.1kHz, 48kHz
	Channel count	2 (mono, stereo, dual, joint stereo)
	Audio input interface	LR multiplex serial
	Bit rate	Max. 448kbps
Multiplexer	Encoding method	ISO/IEC11172−1 (MPEG1 system) ISO/IEC13818−1 (MPEG2 system PS/TS) [Can also output to mono media in ES and PES formats.]
	Stream output	8bit parallel
	Bit rate	Max. 20Mbps (CBR/VBR)
Overall controller		Internal 32bit RISC processor
External memory interface	SDRAM I/F for video encoding	Connects two 16Mbit (1M×16bits) or one 64Mbit (2M×32bits)
	Host/SDRAM I/F	Connects two 16Mbit (1M×16bits) or one 64Mbit (2M×32bits)
Serial interface		One internal port for overall controller BOOT and command I/F
Time base corrector		Absorbs timing errors due to disarrayed input video images by temporarily buffering before reading video input data on an SDRAM connected to the host/SDRAM I/F.

1.3.3 Package

1.4 Block Diagram

Fig. 1.4 shows a block outline diagram of this LSI and Table 1.4 lists the functional overviews of major blocks.

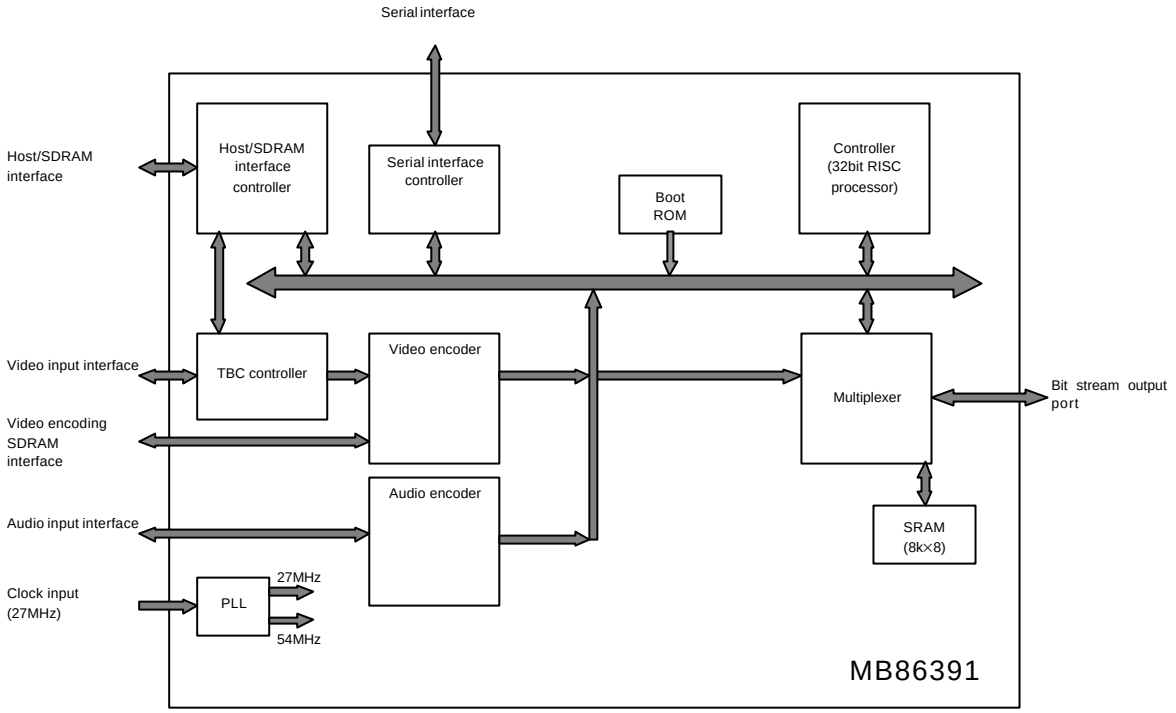


Fig. 1.4 : MB86391 block diagram

Table 1.4 : Overview of major block functions

Block name	Functional overview
Video encoder	Encodes video data input from the TBC controller to create video streams.
Audio encoder	Encodes audio data input from outside to create audio streams.
Multiplexer	Multiplexes video and audio streams generated by video and audio encoders to generate 8bit parallel stream data for output to outside.
Controller	Controls the entire MB86391 using dedicated firmware.
TBC controller	Stores video data input from outside in an external SDRAM and theninput it to the video encoder. The TBC (Time Base Corrector) function is accomplished by buffering video data in the SDRAM.
Host/SDRAM interface controller	Arbitrates SDRAM and MB86391 internal register access requests from MB86391 internal blocks and external master devices. Also used as the command interface with the host.
Serial interface controller	Downloads dedicated firmware to the external SDRAM via this interface at the time of serial booting. Also used as a command interface with the host.
Video PES converter	Converts the format of video streams the video encoder has generated and outputs to the multiplexer.
DMA controller	Controls DMA transfer among MB86391 blocks and external SDRAMs.
Boot ROM	Stores the boot program for the internal controller.

2 Pin Description

2.1 I/O Signals

Fig. 2.1 shows the I/O signals of this LSI.

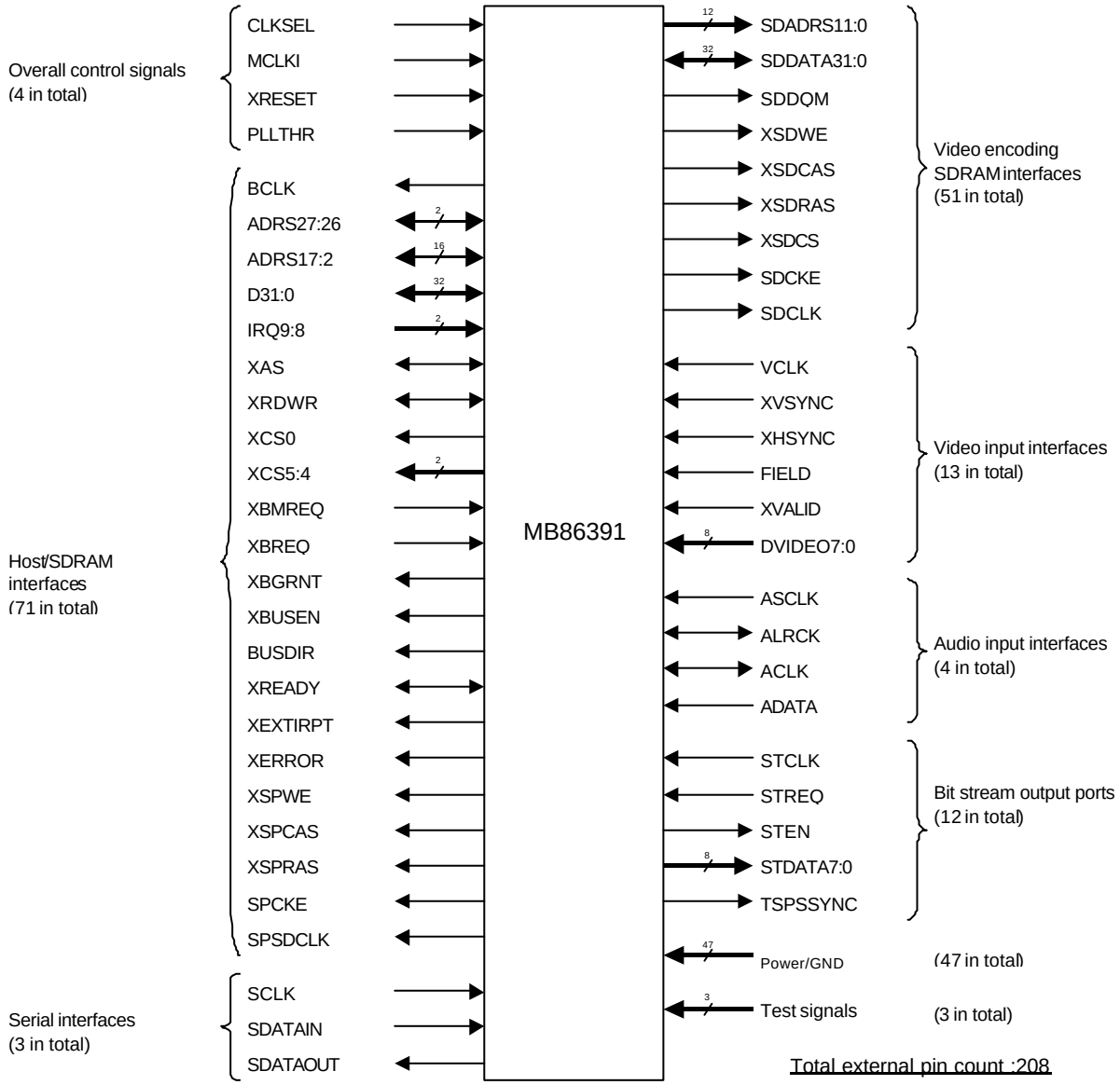


Fig. 2.1 : I/O signal diagram

2.2 Pin Arrangement

2.2.1 Pin Arrangement Diagram

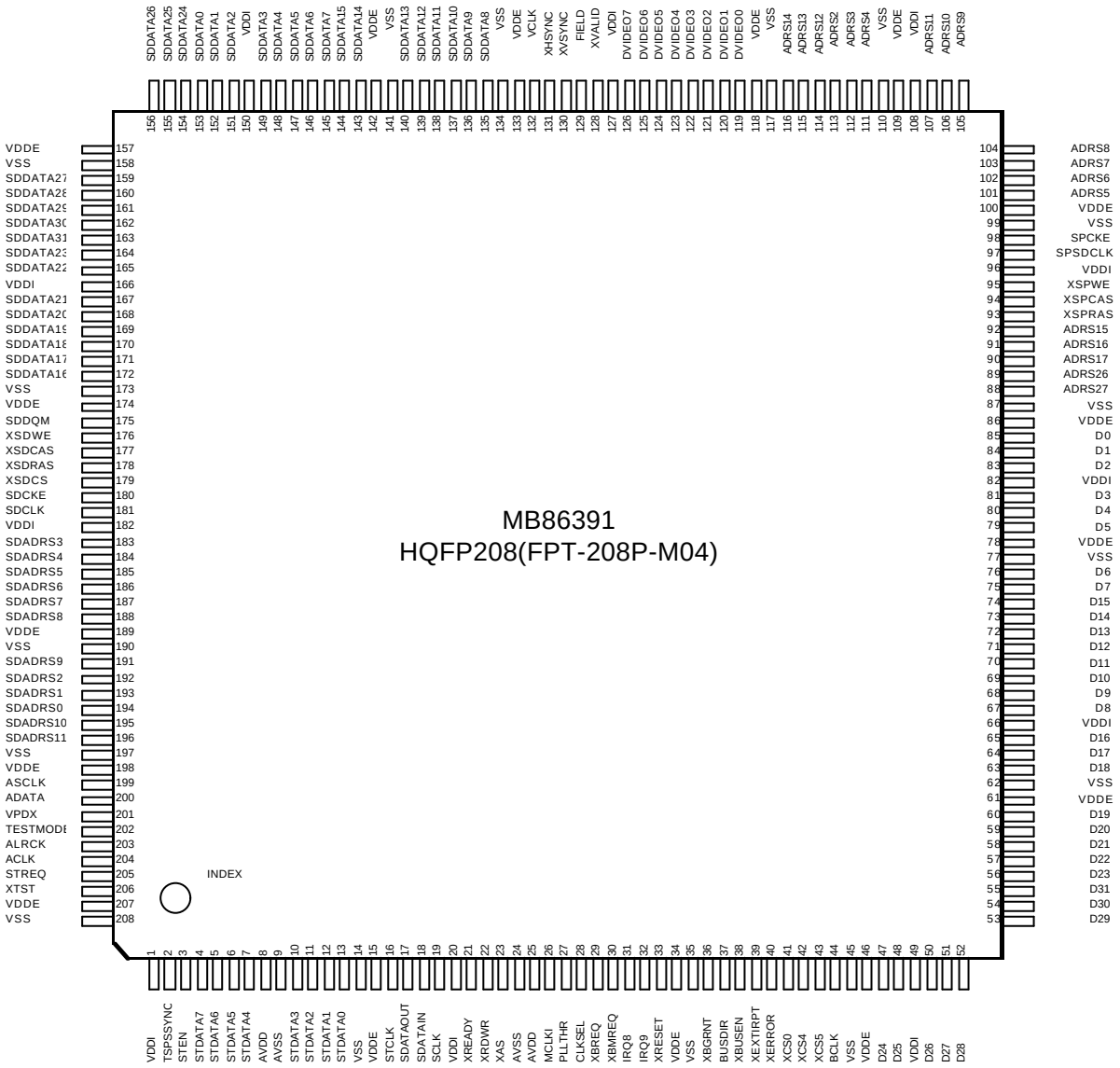


Fig. 2.2.1 : Pin arrangement diagram

2.2.2 Pin Numbers

Table 2.2.2 : Pin number list

Pin No.	I/O	Pin name	Pin No.	I/O	Pin name	Pin No.	I/O	Pin name	Pin No.	I/O	Pin name
1	–	VDDI	53	I/O	D29	105	I/O	ADRS9	157	–	VDDE
2	O	TSPSSYNC	54	I/O	D30	106	I/O	ADRS10	158	–	VSS
3	O	STEN	55	I/O	D31	107	I/O	ADRS11	159	I/O	SDDATA27
4	O	STDATA7	56	I/O	D23	108	–	VDDI	160	I/O	SDDATA28
5	O	STDATA6	57	I/O	D22	109	–	VDDE	161	I/O	SDDATA29
6	O	STDATA5	58	I/O	D21	110	–	VSS	162	I/O	SDDATA30
7	O	STDATA4	59	I/O	D20	111	I/O	ADRS4	163	I/O	SDDATA31
8	–	AVDD	60	I/O	D19	112	I/O	ADRS3	164	I/O	SDDATA23
9	–	AVSS	61	–	VDDE	113	I/O	ADRS2	165	I/O	SDDATA22
10	O	STDATA3	62	–	VSS	114	I/O	ADRS12	166	–	VDDI
11	O	STDATA2	63	I/O	D18	115	I/O	ADRS13	167	I/O	SDDATA21
12	O	STDATA1	64	I/O	D17	116	I/O	ADRS14	168	I/O	SDDATA20
13	O	STDATA0	65	I/O	D16	117	–	VSS	169	I/O	SDDATA19
14	–	VSS	66	–	VDDI	118	–	VDDE	170	I/O	SDDATA18
15	–	VDDE	67	I/O	D8	119	I	DVIDEO0	171	I/O	SDDATA17
16	I	STCLK	68	I/O	D9	120	I	DVIDEO1	172	I/O	SDDATA16
17	O	SDATAOUT	69	I/O	D10	121	I	DVIDEO2	173	–	VSS
18	I	SDATAIN	70	I/O	D11	122	I	DVIDEO3	174	–	VDDE
19	I	SCLK	71	I/O	D12	123	I	DVIDEO4	175	O	SDDQM
20	–	VDDI	72	I/O	D13	124	I	DVIDEO5	176	O	XSDWE
21	I/O	XREADY	73	I/O	D14	125	I	DVIDEO6	177	O	XSDCAS
22	I/O	XRDWR	74	I/O	D15	126	I	DVIDEO7	178	O	XSDRAS
23	I/O	XAS	75	I/O	D7	127	–	VDDI	179	O	XSDCS
24	–	AVSS	76	I/O	D6	128	I	XVALID	180	O	SDCKE
25	–	AVDD	77	–	VSS	129	I	FIELD	181	O	SDCLK
26	I	MCLKI	78	–	VDDE	130	I	XVSYNC	182	–	VDDI
27	I	PLLTHR	79	I/O	D5	131	I	XHSYNC	183	O	SDADRS3
28	I	CLKSEL	80	I/O	D4	132	I	VCLK	184	O	SDADRS4
29	I	XBREQ	81	I/O	D3	133	–	VDDE	185	O	SDADRS5
30	I	XBMREQ	82	–	VDDI	134	–	VSS	186	O	SDADRS6
31	I	IRQ8	83	I/O	D2	135	I/O	SDDATA8	187	O	SDADRS7
32	I	IRQ9	84	I/O	D1	136	I/O	SDDATA9	188	O	SDADRS8
33	I	XRESET	85	I/O	D0	137	I/O	SDDATA10	189	–	VDDE
34	–	VDDE	86	–	VDDE	138	I/O	SDDATA11	190	–	VSS
35	–	VSS	87	–	VSS	139	I/O	SDDATA12	191	O	SDADRS9
36	O	XBGRNT	88	I/O	ADRS27	140	I/O	SDDATA13	192	O	SDADRS2
37	O	BUSDIR	89	I/O	ADRS26	141	–	VSS	193	O	SDADRS1
38	O	XBUSEN	90	I/O	ADRS17	142	–	VDDE	194	O	SDADRS0
39	O	XEXTIRPT	91	I/O	ADRS16	143	I/O	SDDATA14	195	O	SDADRS10
40	O	XERROR	92	I/O	ADRS15	144	I/O	SDDATA15	196	O	SDADRS11
41	O	XCS0	93	O	XSPRAS	145	I/O	SDDATA7	197	–	VSS
42	O	XCS4	94	O	XSPCAS	146	I/O	SDDATA6	198	–	VDDE
43	O	XCS5	95	O	XSPWE	147	I/O	SDDATA5	199	I	ASCLK
44	O	BCLK	96	–	VDDI	148	I/O	SDDATA4	200	I	ADATA
45	–	VSS	97	O	SPSDCLK	149	I/O	SDDATA3	201	I	VPDX
46	–	VDDE	98	O	SPCKE	150	–	VDDI	202	I	TESTMODE
47	I/O	D24	99	–	VSS	151	I/O	SDDATA2	203	I/O	ALRCK
48	I/O	D25	100	–	VDDE	152	I/O	SDDATA1	204	I/O	ACLK
49	–	VDDI	101	I/O	ADRS5	153	I/O	SDDATA0	205	I	STREQ
50	I/O	D26	102	I/O	ADRS6	154	I/O	SDDATA24	206	I	XTST
51	I/O	D27	103	I/O	ADRS7	155	I/O	SDDATA25	207	–	VDDE
52	I/O	D28	104	I/O	ADRS8	156	I/O	SDDATA26	208	–	VSS

VDDE : 3.3V power supply, VDDI : 1.8V power supply, AVDD : 1.8V power supply to PLL
VSS, AVSS : ground

2.3 Pin Functions

The pin functions of this LSI are shown below.

2.3.1 Overall Control

Table 2.3.1 : Overall control pins

Pin No.	Pin symbol	Pin name	Bit	I/O	Active	Pull up /down	Description
28	CLKSEL	Internal Clock Select	1	I	–	–	Internal controller operating frequency selection input pin. When the screen size is D1, select 54MHz operations. 'H' = 54MHz operations 'L' = 27MHz operations
26	MCLKI	Main Clock Input	1	I	–	–	Operating clock (27MHz) input pin
33	XRESET	Reset	1	I	L	–	Reset signal input pin
27	PLLTHR	PLL through	1	I	–	–	Internal PLL control signal input pin (See figure on page 52)

2.3.2 Host/SDRAM interface

Table 2.3.2 : Host/SDRAM interface pins

Pin No.	Pin symbol	Pin name	Bit	I/O	Active	Pull up/down	Pin function
44	BCLK	Bus Clock	1	O	–	–	Host/SDRAM interface bus clock (27MHz) output pin
88,89	ADRS27:26	Address 27:26	2	I/O	–	–	Address (upper 2bits) I/O pins
90 to 92, 116 to 114, 107 to 101, 111 to 113	ADRS17:2	Address 17:2	16	I/O	–	–	Address (lower 16bits) I/O pins
55 to 50,48,47, 56 to 60, 63 to 65, 74 to 67,75,76, 79 to 81, 83 to 85	D31:0	Data31:0	32	I/O	–	–	32bit data I/O pins
32,31	IRQ9:8	Interrupt Request 9:8	2	I	L	pullup	Interrupt request input pins. When not in use, connect to either OPEN or VDDE.
23	XAS	Address Strobe	1	I/O	L	–	Address strobe I/O pin
22	XRDWR	Read/Write	1	I/O	–	–	Read/write I/O pin: 'H' = Read 'L' = Write
41	XCS0	Chip Select 0	1	O	L	pullup	Chip select 0 output pin
43,42	XCS5:4	Chip Select 5:4	2	O	L	–	Chip select 5:4 output pins
30	XBMREQ	Burst Mode Request	1	I	L	pullup	Burst transfer request input pin
29	XBREQ	Bus Request	1	I	L	pullup	Bus privilege request input pin
36	XBGRNT	Bus Grant	1	O	L	–	Bus grant output pin
38	XBUSEN	Bus Buffer Enable	1	O	L	–	Bus buffer enable output pin
37	BUSDIR	Bus Buffer Direction	1	O	–	–	Bus buffer direction control output pin
21	XREADY	Ready	1	I/O	L	–	Ready I/O pin
39	XEXTIRPT	External Interrupt	1	O	L	–	External host interruption request pin
40	XERROR	Error	1	O	L	–	Error output pin
95	XSPWE	Write Enable	1	O	L	–	Write enable output pin to SDRAM connected to host/SDRAM interface
94	XSPCAS	Column Address Strobe	1	O	L	–	Column address strobe output pin to SDRAM connected to host/SDRAM interface
93	XSPRAS	Row Address Strobe	1	O	L	–	Row address strobe output pin to SDRAM connected to host/SDRAM interface
98	SPCKE	Clock Enable	1	O	H	–	Clock enable output pin to SDRAM connected to host/SDRAM interface
97	SPSDCLK	SDRAM Clock	1	O	–	–	Clock output pin to SDRAM connected to host/SDRAM interface

2.3.3 Serial Interface

Table 2.3.3: Serial interface pins

Pin No.	Pin symbol	Pin name	Bit	I/O	Active	Pull up/down	Pin function
19	SCLK	Serial Clock	1	I	–	–	Serial I/F serial clock input pin.
18	SDATAIN	Serial Data Input	1	I	–	–	Serial I/F data input pin.
17	SDATAOUT	Serial Data Output	1	O	–	–	Serial I/F data output pin.

2.3.4 SDRAM Interface for Video Encoding

Table 2.3.4: SDRAM interface pins for video encoding

Pin No.	Pin symbol	Pin name	Bit	I/O	Active	Pull up/down	Pin function
196,195,191, 188 to 183, 192 to 194	SDADRS11:0	SDRAM Address	12	O	–	–	Address output (12bits) pins to SDRAM connected to the video encoding SDRAM interface
163 to 159, 156 to 154, 164,165, 167 to 172, 144,143, 140 to 135, 145 to 149, 151 to 153	SDDATA31:0	SDRAM Data	32	I/O	–	pullup	Data I/O (32bits) pins to SDRAM connected to the video encoding SDRAM interface
175	SDDQM	Input Mask /Output Enable	1	O	H	–	Data mask output pin to SDRAM connected to the video encoding SDRAM interface
176	XSDWE	Write Enable	1	O	L	–	Write enable output pin to SDRAM connected to the video encoding SDRAM interface
177	XSDCAS	Column Address Strobe	1	O	L	–	Column address strobe output pin to SDRAM connected to the video encoding SDRAM interface
178	XSDRAS	Row Address Strobe	1	O	L	–	Row address strobe output pin to SDRAM connected to the video encoding SDRAM interface
179	XSDCS	Chip Select	1	O	L	–	Chip select output pin to SDRAM connected to the video encoding SDRAM interface
180	SDCKE	Clock Enable	1	O	H	–	Clock enable output pin to SDRAM connected to the video encoding SDRAM interface
181	SDCLK	SDRAM Clock	1	O	–	–	Clock output pin to SDRAM connected to the video encoding SDRAM interface

2.3.5 Video Input Interface

Table 2.3.5: Video input interface pins

Pin No.	Pin symbol	Pin name	Bit	I/O	Active	Pull up/down	Pin function
132	VCLK	Video Clock	1	I	–	–	Video clock input pin.
130	XVSYNC	Vertical Sync	1	I	L	–	Vertical sync input pin.
131	XHSYNC	Horizontal Sync	1	I	L	–	Horizontal sync input pin.
129	FIELD	Field	1	I	–	–	Field ID input pin.
128	XVALID	Data Valid	1	I	L	–	Input pin to indicate that valid data exists at DVIDEO7:0.
126 to 119	DVIDEO7:0	Digital Video	8	I	–	–	Video input data input pin.

2.3.6 Audio Input Interface

Table 2.3.6:Audio input interface pins

Pin No.	Pin symbol	Pin name	Bit	I/O	Active	Pull up/down	Pin function
199	ASCLK	Audio System Clock	1	I	–	–	System clock input pin for audio. Input clock 256 times the audio sampling frequency. Must be in sync with MCLKI.
203	ALRCK	Audio L/R Clock	1	I/O	–	–	Audio sampling clock pin. The pin outputs in master mode and inputs in slave mode.
204	ACLK	Audio Bit Clock	1	I/O	–	–	Audio bit clock pin. The pin outputs in master mode and inputs in slave mode.
200	ADATA	Audio Serial Data	1	I	–	–	Audio serial data input pin.

2.3.7 Bit Stream Output Port

Table 2.3.7: Bit stream output port pins

Pin No.	Pin symbol	Pin name	Bit	I/O	Active	Pull up/down	Pin function
16	STCLK	Bit Stream Transfer Clock	1	I	–	pullup	Bit stream transfer clock input pin. The clock is for stream reading in transfer clock sync mode.
205	STREQ	Bit Stream Transfer Request	1	I	H	–	Bit stream transfer request input pin. When transferring streams in transfer clock sync mode, connect to VDDE.
3	STEN	Bit Stream Output Enable	1	O	H	–	Bit stream output enable output pin.
4 to 7,10 to 13	STDATA7:0	Bit Stream Data7:0	8	O	–	–	Bit stream output port (8bit) pin. The error code is output in case of an error.
2	TSPSSYNC	TS/PS Sync	1	O	H	–	This output pin indicates the leading data of the TS/PS packet. 1cycle is set to 'H" at the sync byte of the packet in the case of TS and at the leading byte of the PACK header or PS end code in the case of PS.

2.3.8 Test Signals

Table 2.3.8: Test pins

Pin No.	Pin symbol	Pin name	Bit	I/O	Active	Pull up/down	Pin function
201	VPDX	–	1	I	H	–	A test pin. For typical usage, connect to VSS.
202	TESTMODE	–	1	I	H	pull down	A test pin. For typical usage, connect to OPEN or VSS.
206	XTST	–	1	I	L	pull up	A test pin. For typical usage, connect to OPEN or VDDE.

3 Functional Description

3.1 Host/SDRAM Interface

The host/SDRAM interface arbitrates bus privilege between the external master connected to this interface and MB86391 internal resources and also controls access to external resources (such as SDRAM, boot ROM, and MPEG decoder). Fig. 3.1 shows an example host/SDRAM interface connection. The next and subsequent chapters show timing diagrams for various accesses.

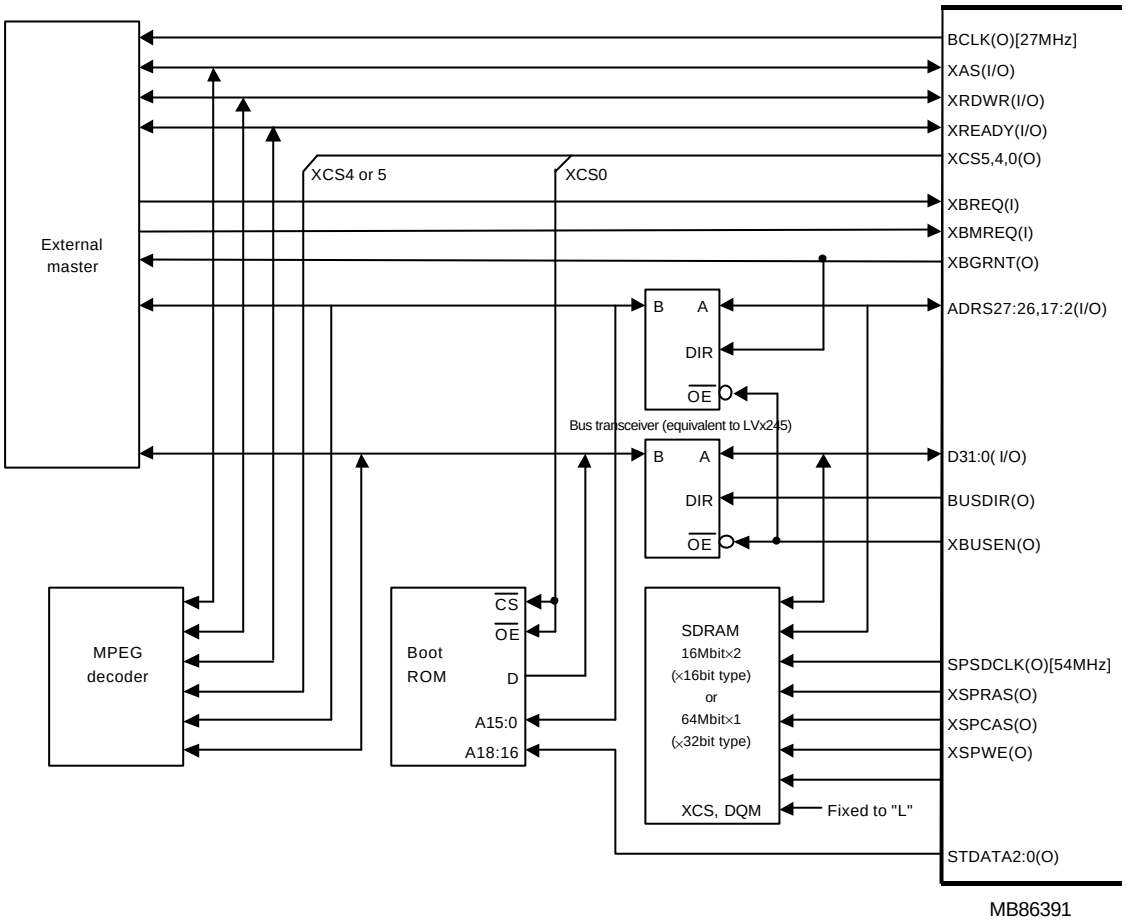


Fig. 3.1: Host/SDRAM interface connection (Example)

Note: In the case of a 16Mbit SDRAM, connect ADRS13:2 to BA, A10:0. In the case of a 64Mbit SDRAM, connect ADRS13:2 to BA1, A10:0. Keep BA0 fixed to 'H' or 'L.'
Install the MB86391 and the SDRAM as physically close as possible.
Pull up the SPSDCLK signal line with a resistance of 200Ω in the vicinity of the SDRAM.
The SPSDCLK signal line must be in a pattern of a single stroke, from the MB86391, the sending end, through the SDRAM CLK to the point of connection to the pull–up resistance.
Other signal lines do not require any particular handling such as pull–up. However, take care to avoid unnecessary routing when designing patterns.
MB86391 can connect each bit width of boot ROM such as ×8bit, ×16bit and ×32bit. (Recommended ×16bit) Recommended boot ROM size is over 4Mbit.

Fig. 3.1: Host/SDRAM interface connection (Example)

3.1.1 Access by External Master

Shown below are diagrams of timing according to which the external master accesses MB86391 internal resources and SDRAM and peripheral chips (MPEG2 decoder LSI, for example) connected to this interface.

3.1.1.1 MB86391 Internal Resource Accessing

(a) Write

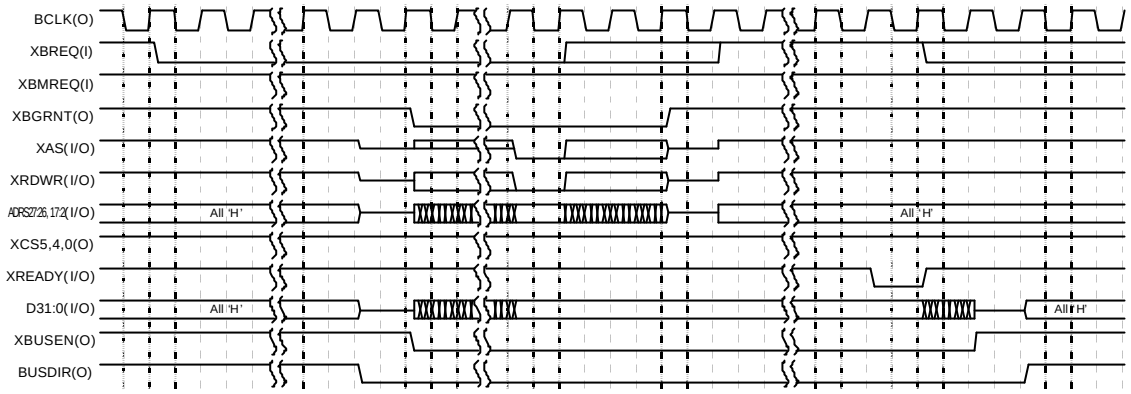


Fig. 3.1.1.1a:MB86391 internal resource access timing (Write)

(1) The external master asserts XBREQ and requests for bus privilege.

(2) Before granting bus privilege, the MB86391 sets XAS, XRDWR, ADRS27:26, 17:2 and D31:0 to Hi−Z and BUSDIR to 'L' (write direction) and asserts XBGRNT and XBUSEN to grant bus privilege to the external master.

(3) The external master outputs valid data to XRDWR, ADRS27:26, 17:2 and D31:0 and asserts the XAS signal. Note that XBREQ must be asserted up to this cycle.

(4) The MB86391 fetches the address and control signal statuses in (3) and then negates XBGRNT. At negation of XBGRNT, the external master needs to set XAS, XRDWR and ADRS27:26,17:2 to Hi−Z.

(5) After writing data, the MB86391 asserts XREADY and notifies the external master of write completion.

(6) The MB86391 negates XBUSEN, sets BUSDIR to 'H' (read direction), and resets to normal state.

Note: After negating XREADY, the next request for bus privilege (asserting XBREQ) is allowed.

(b) Read

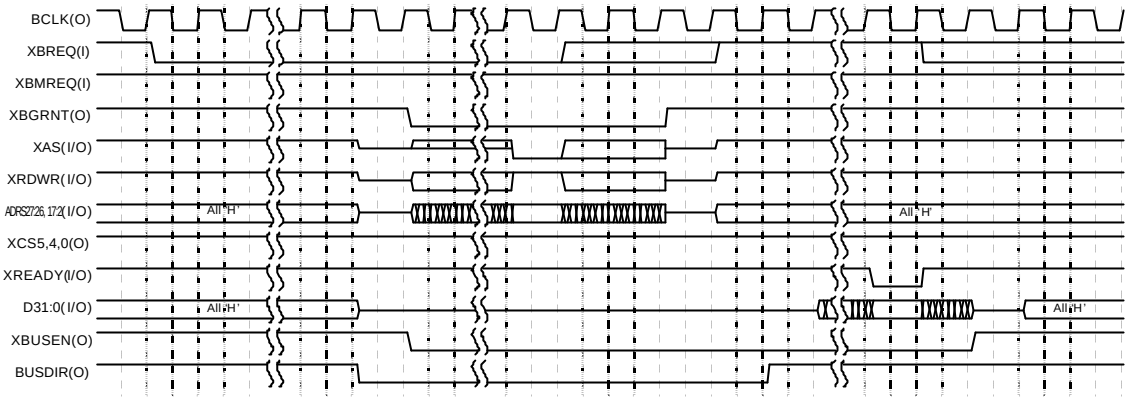


Fig. 3.1.1.1b: MB86391 internal resource access timing (Read))

(1) The external master asserts XBREQ and requests for bus privilege.

(2) Before granting bus privilege, the MB86391 sets XAS, XRDWR, ADRS27:26, 17:2 and D31:0 to Hi−Z and BUSDIR to 'L' (write direction) and then asserts XBGRNT and XBUSEN to grant bus privilege to the external master.

(3) The external master outputs valid data to XRDWR and ADRS27:26, 17:2 and asserts the XAS signal. Note that XBREQ must be asserted up to this cycle.

(4) The MB86391 fetches the address and control signal statuses in (3) and then negates XBGRNT. At negation of XBGRNT, the external master needs to set XAS, XRDWR and ADRS27:26,17:2 to Hi−Z.

(5) The MB86391 sets BUSDIR to 'H' (read direction) to allow read data output.

(6) The MB86391 outputs valid data to D31:0 at the same time as it asserts XREADY (the external master fetches read data at this timing).

(7) The MB86391 negates XBUSEN and resets to its normal state.

Note: After negating XREADY, the next request for bus privilege (asserting XBREQ) is allowed.

3.1.1.2 SDRAM Accessing

(a) Single write

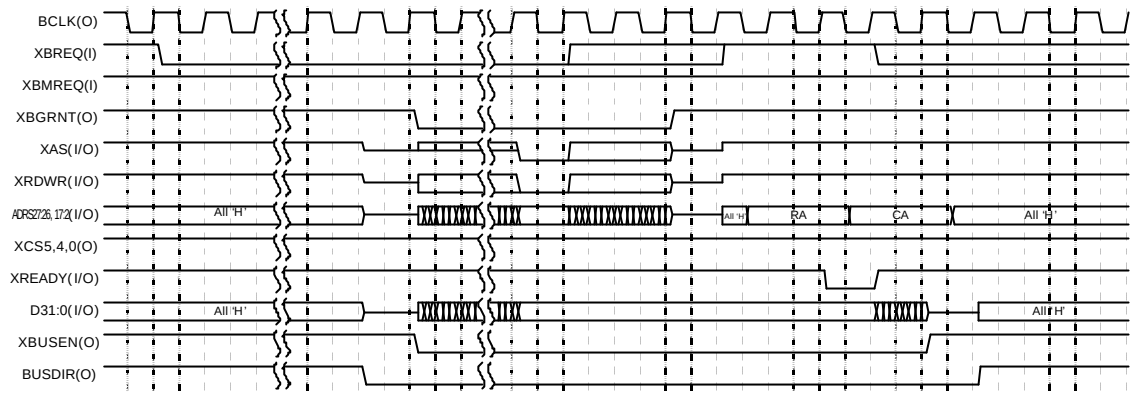


Fig. 3.1.1.2a:SDRAM access timing (Single write)

(1) The external master asserts XBREQ and requests for bus privilege.

(2) Before granting bus privilege, the MB86391 sets XAS, XRDWR, ADRS27:26,17:2 and D31:0 to Hi−Z and BUSDIR to 'L' (write direction) and then asserts XBGRNT and XBUSEN to grant bus privilege to the external master.

(3) The external master outputs valid data to XRDWR, ADRS27:26, 17:2, and D31:0 and asserts the XAS signal. Note that XBREQ must be asserted up to this cycle.

(4) The MB86391 fetches the address and control signal statuses in (3) and then negates XBGRNT. At negation of XBGRNT, the external master needs to set XAS, XRDWR and ADRS27:26,17:2 to Hi−Z.

(5) The MB86391 re−outputs the address fetched in (4) to the SDRAM at the command.

(6) The MB86391 asserts the XREADY signal during the cycle to write data to the SDRAM and notifies it to the external master.

(7) The MB86391 negates XBUSEN, sets BUSDIR to 'H' (read direction), and resets to normal state.

Note: After negating XREADY, the next request for bus privilege (asserting XBREQ) is allowed.

(b) Single read

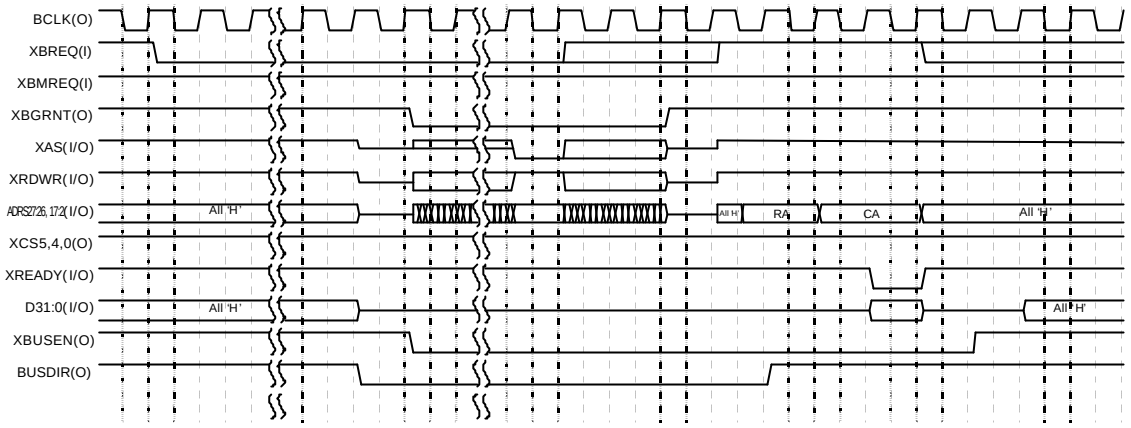


Fig. 3.1.1.2b: SDRAM access timing (Single read)

(1) The external master asserts XBREQ and requests for bus privilege.

(2) Before granting bus privilege, the MB86391 sets XAS, XRDWR, ADRS27:26,17:2 and D31:0 to Hi−Z and BUSDIR to 'L' (write direction) and then asserts XBGRNT and XBUSEN to grant bus privilege to the external master.

(3) The external master outputs valid data to XRDWR and ADRS27:26, 17:2 and asserts the XAS signal. Note that XBREQ must be asserted up to this cycle.

(4) The MB86391 fetches the address and control signal statuses in (3) and then negates XBGRNT. At negation of XBGRNT, the external master needs to set XAS, XRDWR and ADRS27:26, 17:2 to Hi−Z.

(5) The MB86391 re−outputs the address fetched in (4) to the SDRAM at the command.

(6) The MB86391 sets BUSDIR to 'H' (read direction) to allow read data output.

(7) The MB86391 asserts the XREADY signal during the SDRAM data read cycle and notifies it to the external master.

(8) The MB86391 negates XBUSEN and resets to its normal state.

Note: After negating XREADY, the next request for bus privilege (asserting XBREQ) is allowed.

(c) Burst write

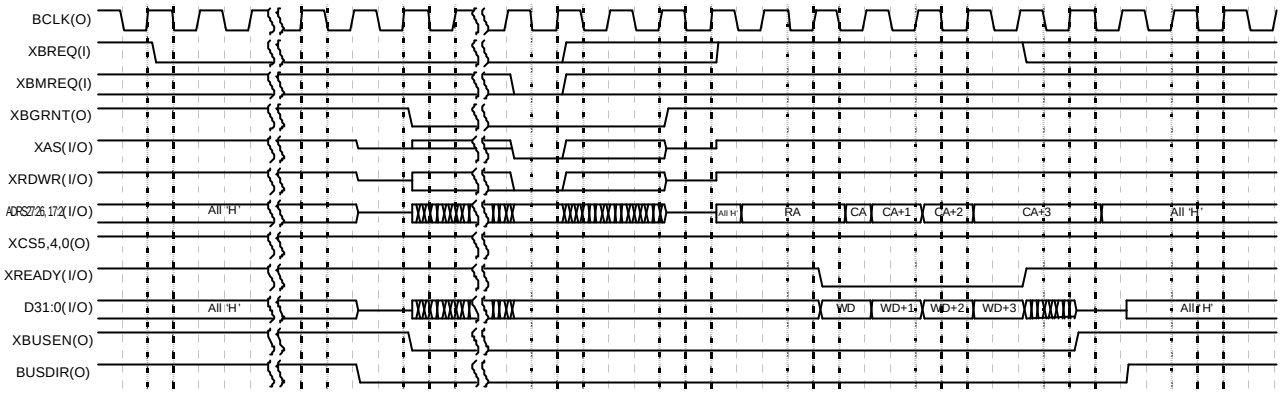


Fig. 3.1.1.2c: SDRAM access timing (Burst write))

(1) The external master asserts XBREQ and requests for bus privilege.

(2) Before granting bus privilege, the MB86391 sets XAS, XRDWR, ADRS27:26,17:2 and D31:0 to Hi−Z and BUSDIR to 'L' (write direction) and then asserts XBGRNT and XBUSEN to grant bus privilege to the external master.

(3) The external master outputs valid data to XBMREQ, XRDWR, ADRS27:26, 17:2, and D31:0 and asserts the XAS signal. Note that XBREQ must be asserted up to this cycle.

(4) The MB86391 fetches the address and control signal statuses in (3) and then negates XBGRNT. At negation of XBGRNT, the external master needs to set XAS, XRDWR and ADRS27:26,17:2 to Hi−Z.

(5) The MB86391 re−outputs the address fetched in (4) to the SDRAM at the command.

(6) The MB86391 asserts the XREADY signal during the cycle to write data to the SDRAM and notifies it to the external master.

(7) The MB86391 negates XBUSEN, sets BUSDIR to 'H' (read direction), and resets to normal state.

Notes: The burst length is fixed to 4.
After negating XREADY, the next request for bus privilege (asserting XBREQ) is allowed.
Burst access extending over 1 KB is not allowed.

(d) Burst read

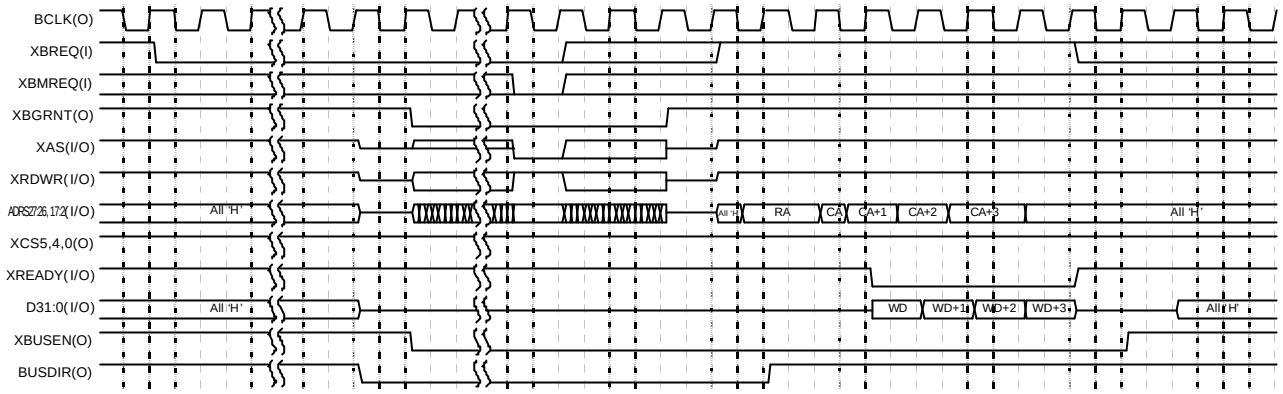


Fig. 3.1.1.2d: SDRAM access timing (Burst read)

(1) The external master asserts XBREQ and requests for bus privilege.

(2) Before granting bus privilege, the MB86391 sets XAS, XRDWR, ADRS27:26,17:2 and D31:0 to Hi–Z and BUSDIR to 'L' (write direction and then asserts XBGRNT and XBUSEN to grant bus privilege to the external master.

(3) The external master outputs valid data to XBMREQ, XRDWR and ADRS27:26, 17:2 and asserts the XAS signal. Note that XBREQ must be asserted up to this cycle.

(4) The MB86391 fetches the address and control signal statuses in (3) and then negates XBGRNT. At negation of XBGRNT, the external master needs to set XAS, XRDWR and ADRS27:26,17:2 to Hi–Z.

(5) The MB86391 re–outputs the address fetched in (4) to the SDRAM at the command.

(6) The MB86391 sets BUSDIR to 'H' (read direction) to allow SDRAM read data output.

(7) The MB86391 asserts the XREADY signal during the SDRAM data read cycle and notifies it to the external master.

(8) The MB86391 negates XBUSEN and resets to its normal state.

Notes: The burst length is fixed to 4.
After negating XREADY, the next request for bus privilege (asserting XBREQ) is allowed.
Burst access extending over 1 KB is not allowed.

3.1.1.3 External Resource Accessing

(a) Write

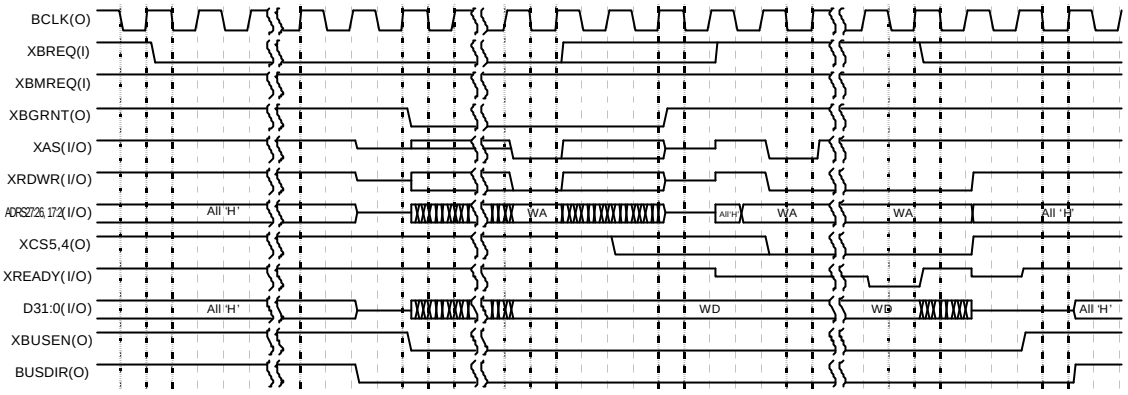


Fig. 3.1.1.3a: External resource access timing (Write)

(1) The external master asserts XBREQ and requests for bus privilege.

(2) Before granting bus privilege, the MB86391 sets XAS, XRDWR, ADRS27:26,17:2 and D31:0 to Hi−Z and BUSDIR to 'L' (write direction) and then asserts XBGRNT and XBUSEN to grant bus privilege to the external master.

(3) The external master outputs valid data to XRDWR, ADRS27:26, 17:2, and D31:0 and asserts the XAS signal. Note that XBREQ must be asserted up to this cycle.

(4) The MB86391 fetches the address and control signal statuses in (3) and then negates XBGRNT. At negation of XBGRNT, the external master needs to set XAS, XRDWR and ADRS27:26, 17:2 to Hi−Z.

(5) After setting XREADY to Hi−Z, the MB86391 asserts the appropriate XCSn(n = 5,4) and re−outputs XAS, XRDWR, and ADRS27:26, 17:2 fetched in (4) to the external resource.

(6) The external resource asserts the XREADY signal and notifies that data write is complete.

(7) The MB86391 negates XBUSEN and XREADY, sets BUSDIR to 'H' (read direction) and resets to its normal state.

Notes: After negating XREADY, the next request for bus privilege (asserting XBREQ) is allowed.
The external resource needs to be set to Hi−Z after setting XREADY to 'H.'

(b) Read

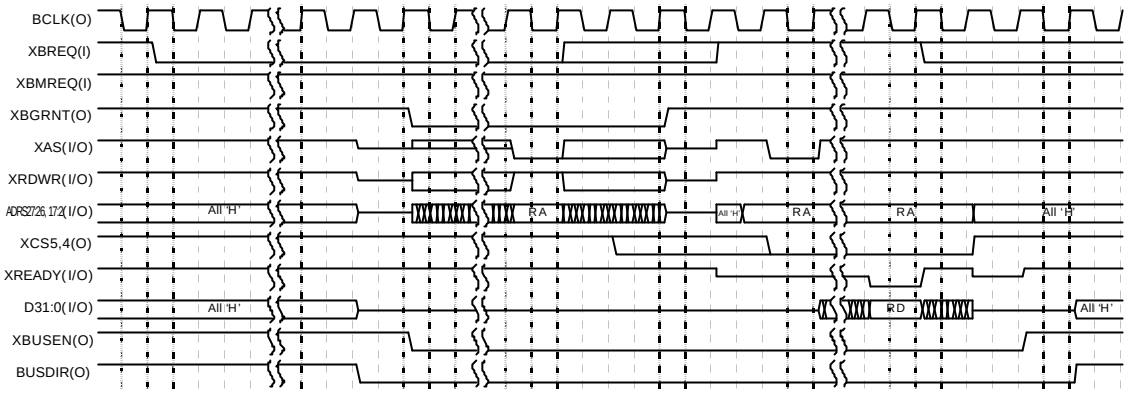


Fig. 3.1.1.3b: External resource access timing (Read)

(1) The external master asserts XBREQ and requests for bus privilege.

(2) Before granting bus privilege, the MB86391 sets XAS, XRDWR, ADRS27:26, 17:2 and D31:0 to Hi−Z and BUSDIR to 'L' (write direction) and then asserts XBGRNT and XBUSEN to grant bus privilege to the external master.

(3) The external master outputs valid data to XRDWR and ADRS27: 26, 17:2 at the same as it asserts the XAS signal. Note that XBREQ must be asserted up to this cycle.

(4) After fetching the address and control signal statuses in (3), the MB86391 negates XBGRNT. At negation of XBGRNT, the external master needs to set XAS, XRDWR and ADRS27:26, 17:2 to Hi−Z.

(5) After setting XREADY to Hi−Z, the MB86391 asserts the appropriate XCSn(n = 5,4) and re−outputs XAS, XRDWR, and ADRS27:26,17:2 fetched in (4) to the external resource.

(6) The external resource asserts the XREADY signal and notifies that valid data is output to D31:0.

(7) The MB86391 negates XBUSEN and XREADY, sets BUSDIR to 'H' (read direction), and resets to normal state.

Notes: After negating XREADY, the next request for bus privilege (asserting XBREQ) is allowed.
The external resource needs to be set to Hi−Z after setting XREADY to 'H."

3.1.2 Internal Controller Master Accessing

Shown below are diagrams of timing according to which the MB86391 internal controller accesses peripheral chips (such as the MPEG2 decoder LSI) connected to this interface.

3.1.2.1 External Resource Accessing

(a) Write

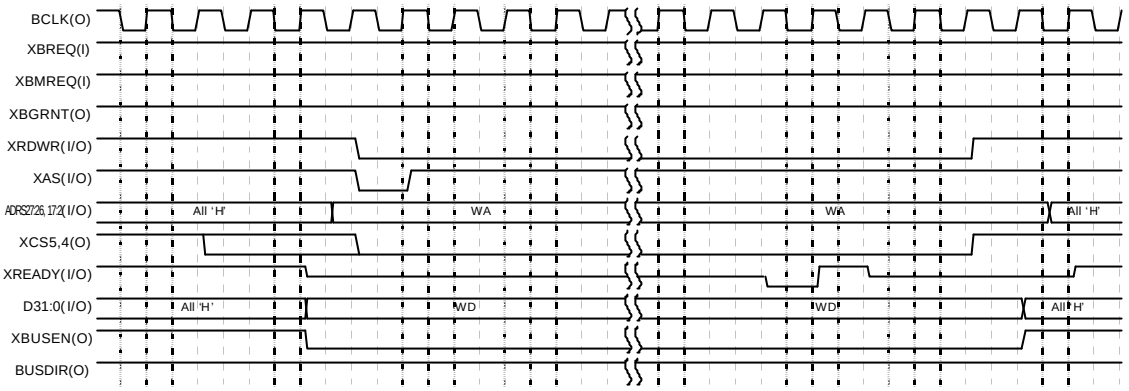


Fig. 3.1.2.1a: External resource access timing (Write)

(1) The MB86391 sets XREADY to Hi–Z and asserts XBUSEN to prepare for accessing.

(2) With XCSn (n = 5,4) asserted, the controller selects an external resource and, in conjunction with XAS assertion, outputs valid data to XRDWR, ADRS27:26, 17:2 and D31:0.

(3) When the external resource asserts the XREADY signal, the MB86391 negates XCSn (n = 5,4) and sets XRDWR to 'H' (read, normal state) at the same time as the selection is cancelled

(4) The controller negates the XBUSEN and XREADY signals to reset to its normal state.

Note: The external resource needs to be set to Hi–Z after setting XREADY to 'H.'

(b) Read

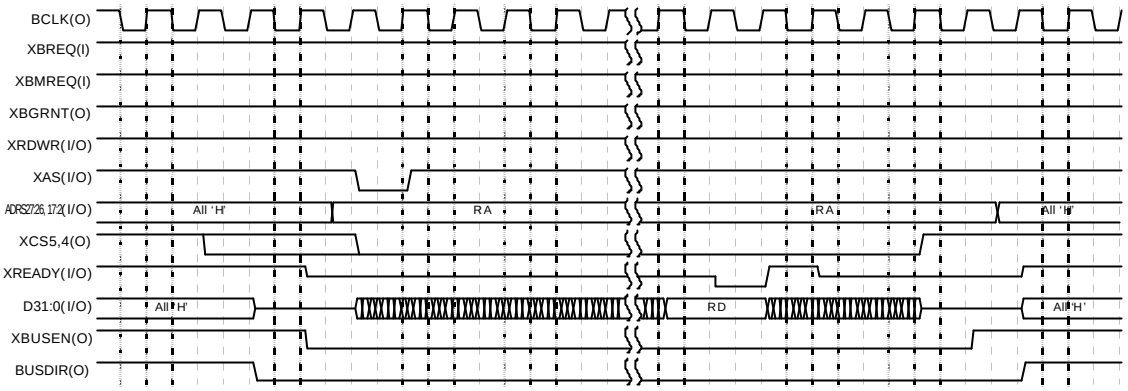


Fig. 3.1.2.1b: External resource access timing (Read)

(1) The MB86391 sets BUSDIR to 'L' (read direction) and XREADY to Hi−Z and asserts XBUSEN to prepare for accessing.

(2) With XCSn (n = 5,4) asserted, the MB86391 selects an external resource and, in conjunction with XAS, outputs valid data to ADRS27:26, 17:2.

(3) When the external resource outputs valid data to D31: 0 and asserts the XREADY signal in the next cycle, the MB86391 reads the data, negates XCSn(n = 5,4), and cancels the selection.

(4) The controller sets BUSDIR to 'H' (write direction), negates the XBUSEN and XREADY signals, and resets to its normal state.

Note: The external resource needs to be set to Hi−Z after setting XREADY to 'H.'

3.1.2.2 External Boot ROM Read

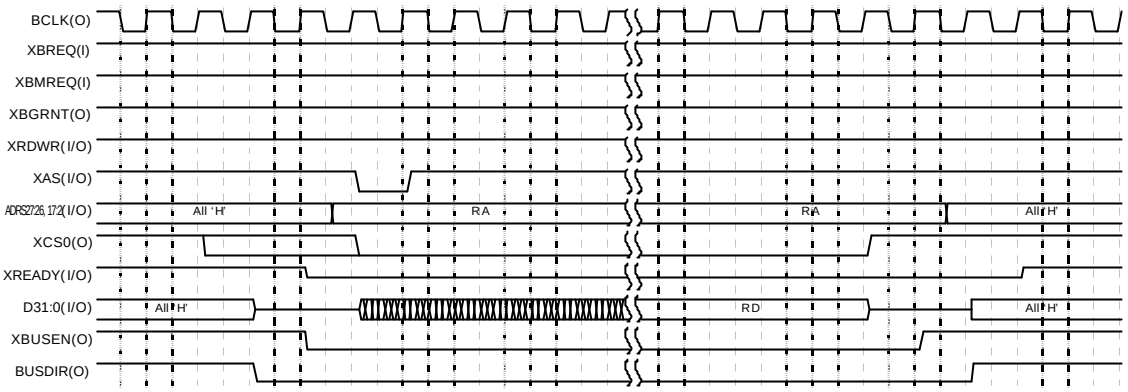


Fig. 3.1.2.2: External boot ROM access timing (Read)

(1) With XCS0 asserted, the MB86391 selects the external boot ROM, sets BUSDIR to 'L' (read direction) and XREADY to Hi–Z, and asserts XBUSEN to prepare for accessing.

(2) In conjunction with XAS, the MB86391 outputs valid data to ADRS27:26, 17:2 (let the external boot ROM output read data to the data bus after confirming XCS0).

(3) After proper wait cycles, the MB86391 reads data and negates XCSO to cancel the selection.

(4) The MB86391 sets BUSDIR to 'H' (write direction), negates the XBUSEN and XREADY signals, and resets to its normal state.

Note: The number of read wait cycles can be set in the boot program according to the ROM in use. When defaulted, accessing is done with 30 wait cycles.

3.1.3 Interruption

3.1.3.1 Internal Controller Interrupt Input (IRQ9:8)

This is the interrupt input to the internal controller. Use this input, for example, to control (using dedicated firmware) the MB86373 (MPEG2 decoder LSI) with the internal controller. When not in use, connect the input to either OPEN or VDDE (fixed to High).

3.1.3.2 Host Interrupt Output (XEXTIRPT)

This is the interrupt output from the internal controller to the external host. The firmware dedicated to the internal controller notifies the external host of the end of command processing, for example. (For more information, see "MB86391 Control Protocol Command Specification (Parallel I/F)").

3.1.4 Address Map

Table 3.1.4: MB86391 address map

Address [*1]	Size (byte)	CSn	Description
0x0000000 to 0x0000FFF	4K	CS0	Internal boot ROM (for internal boot)
0x0001000 to 0x003FFFF	252K	CS0	External ROM (for external boot)
0x4000000 to 0x401FFFF	128K	CS4	External chip select 4
0x4020000 to 0x403FFFF	128K	CS5	External chip select 5
0x8000000 to 0x87FFFFF	8M	–	External SDRAM (8Mbytes)[*2]
0xC000000 to 0xC00FFFF	64K	–	TBC controller & filter
0xC010000 to 0xC01FFFF	64K	–	SDRAM controller
0xC020000 to 0xC02FFFF	64K	–	DMA controller
0xC100000 to 0xC10FFFF	64K	–	Video encoder
0xC200000 to 0xC20FFFF	64K	–	PES converter
0xC300000 to 0xC30FFFF	64K	–	Multiplexing controller
0xC400000 to 0xC40FFFF	64K	–	AUDIO buffer
0xC800000 to 0xC80FFFF	64K	–	Internal controller (internal register)

*1: Any space with no description is reserved.
*2: An area of 4 Mbytes is actually used.

3.2 Serial Interface

The serial interface is provided for serial boot and serial API. Since this interface does not control flow with hardware, you need to control the flow with firmware such as a driver. The firmware dedicated to the internal controller uses ASCII mode.

3.2.1 Serial Interface Receive Operations

The serial interface supports the following receive data formats:

MODE	FM1	FM2	Data section bit count (N)	Description
ASCII	0	MSB	7	ASCII code 0x00 to 0x7F and others
Data32	1	0	32	32−bit binary data

Fig. 3.2.1a-b shows serial interface receive timings.

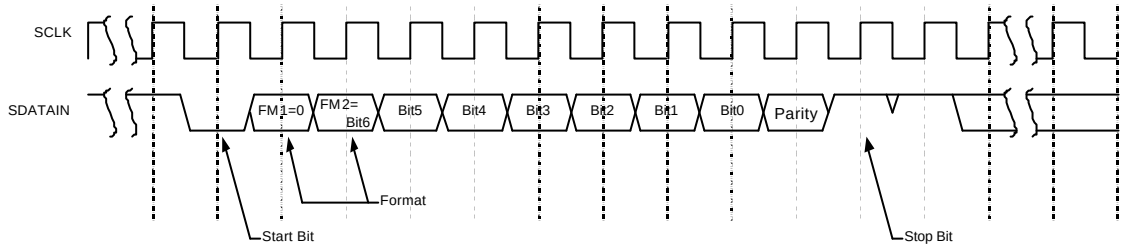


Fig. 3.2.1a: Serial interface receive timings (ASCII mode)

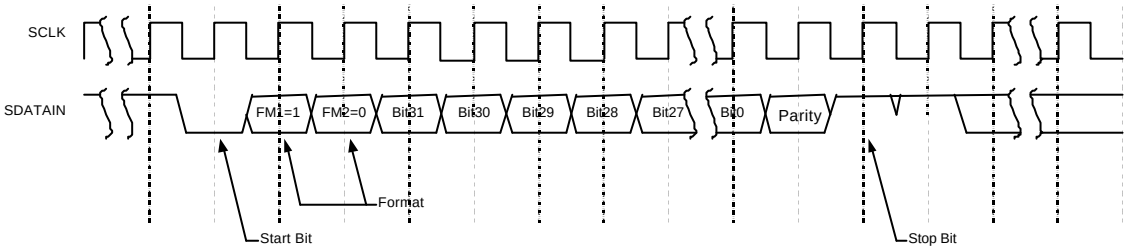


Fig.3.2.1b: Serial interface receiver timing (Dara32 mode)

There are 2 type transport mode (SCLK synchronization mode and start-stop synchronization mode). When using start−stop synchronization mode, pull the SDATAOUT pin down with about 3.3kΩ. When using SCLK synchronization mode, pull the SDATAOUT pin up with about 3.3kΩ. It is not possible to change the transport mode during working.

In SCLK synchronization mode, data is taken on raising edge of SCLK.
In start−stop synchronization mode, data is taken according to 9600bps with reference to the StartBit falling edge of the SDATAIN signal regardless of SCLK.

Use even parity from FM1 through DataN. After the parity bit, 1 is needed as StopBit. However, if 0 is received at this point, it is recognized as a break signal and invalidates receive data.

3.2.2 Serial Interface Send Operations

The serial interface supports the following send data formats

MODE	FM1	FM2	Data section bit count (N)	Description
ASCII	0	MSB	7	ASCII code 0x00 to 0x7F and others
Data32	1	0	32	32−bit binary data (for others)

Fig. 3.2.2a-b shows serial interface send timings.

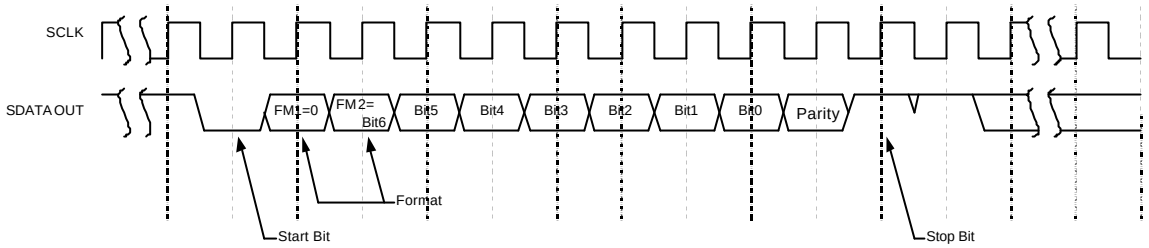


Fig. 3.2.2a: Serial interface send timings (ASCII mode)

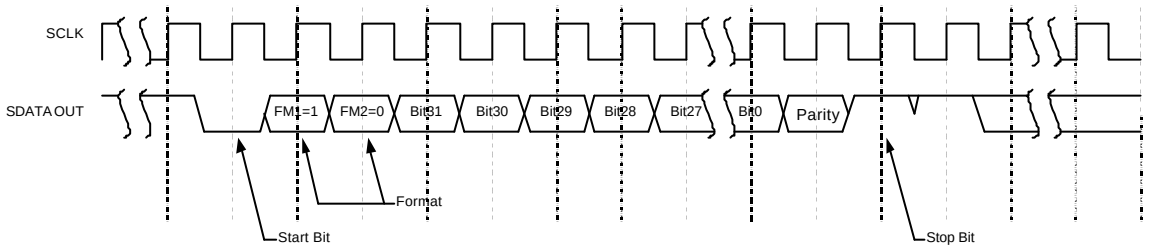


Fig. 3.2.2b: Serial interface send timings (DATA32 mode)

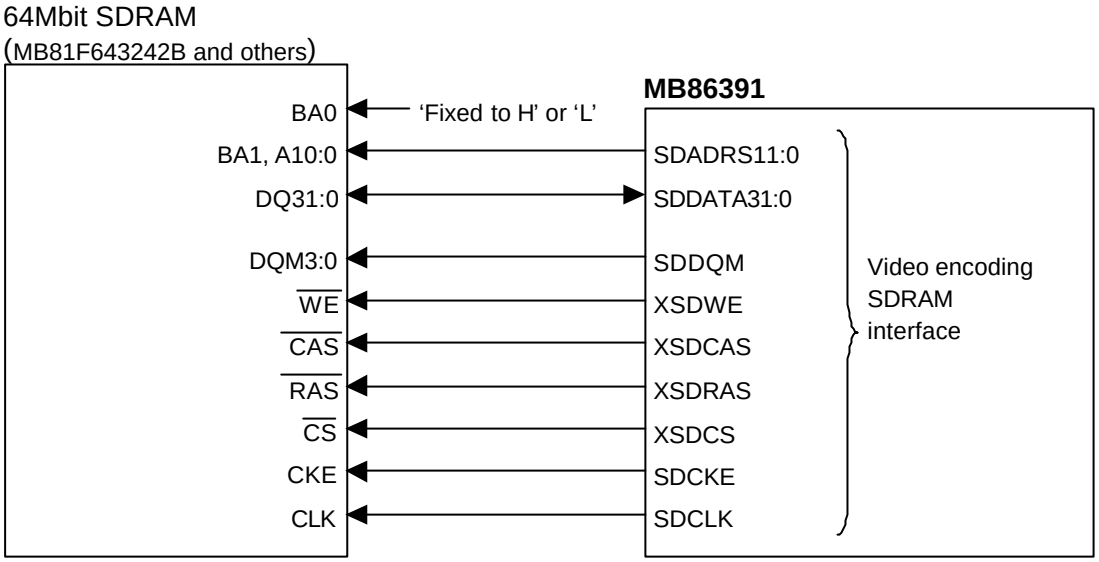
There are 2 type transport mode (SCLK synchronization mode and start-stop synchronization mode). When using start−stop synchronization mode, pull the SDATAOUT pin down with about 3.3kΩ. When using SCLK synchronization mode, pull the SDATAOUT pin up with about 3.3kΩ. It is not possible to change the transport mode during working.

Use even parity from FM1 through DataN.

3.3 SDRAM Interface for Video Encoding

The SDRAM interface for video encoding controls access to an external SDRAM that the video encoder built into this LSI uses to encode video input data.

Connect either two 16Mbit (512K×16bit×2bank configuration) SDRAMs or one 64Mbit (512K×32bit×4bank configuration) SDRAM. Fig. 3.3 shows an example 64Mbit SDRAM connection.



Note: Install the MB86391 and the SDRAM as physically close as possible.
Pull up the SDCLK signal line with a resistance of 200Ω in the vicinity of the SDRAM. The SDCLK signal line must be in a pattern of a single stroke, from the MB86391, the sending end, through the SDRAM CLK to the point of connection to the pull−up resistance.
Other signal lines do not require any particular handling such as pull−up. However, take care to avoid unnecessary routing when designing patterns.

Fig. 3.3: Example video encoding SDRAM interface connection

3.4 Video Input Interface

The video input interface is a dedicated interface between the MB86391 and an external device (such a an NTSC decoder) connected to the MB86391. Fig. 3.4 shows an example connection.

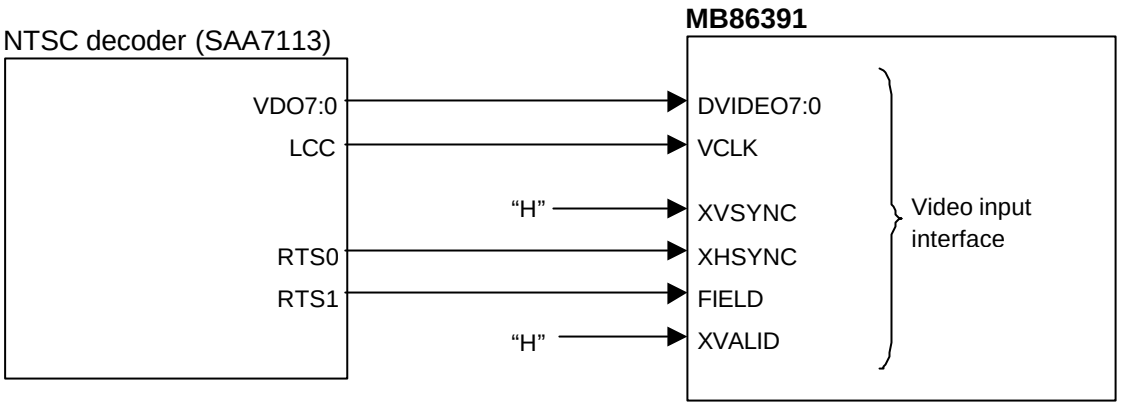


Fig. 3.4: Example video input interface connection

3.4.1 Input Formats

The video input interface is compatible with the following data input formats:

(a) D1 parallel input mode

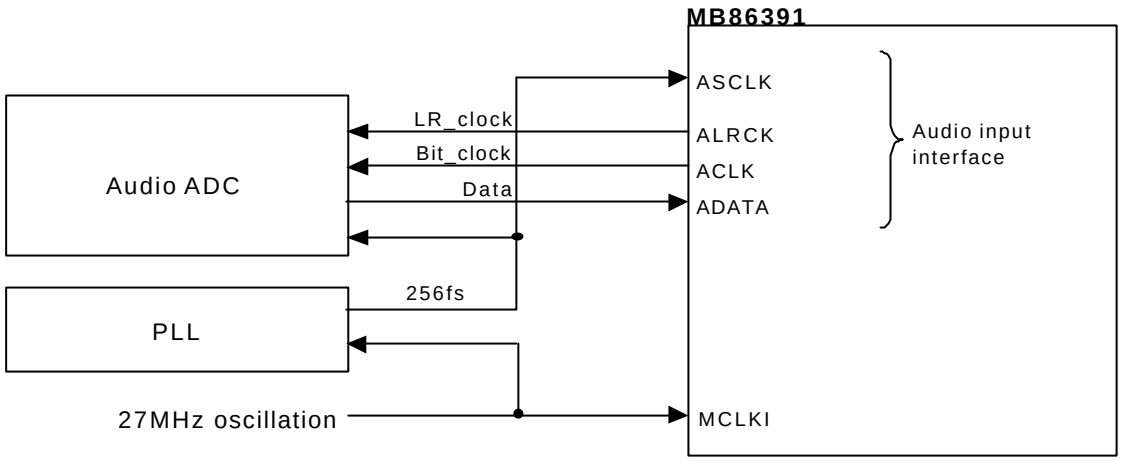
Input D1 format data to the DVIDEO7:0 pin.
The XVSYNC, XHSYNC, FIELD and XVALID pins are not used (keep them fixed to H.) since synchronization information is extracted from the SAV/EAV signal in the D1 data.

(b) Y/C multiplex input mode

Input video data multiplexed in 4:2:2 format (CbYCr in that order) to DVIDEO7:0 pin as well as sync and valid pixel signals to the XVSYNC, XHSYNC, FIELD and XVALID pins.

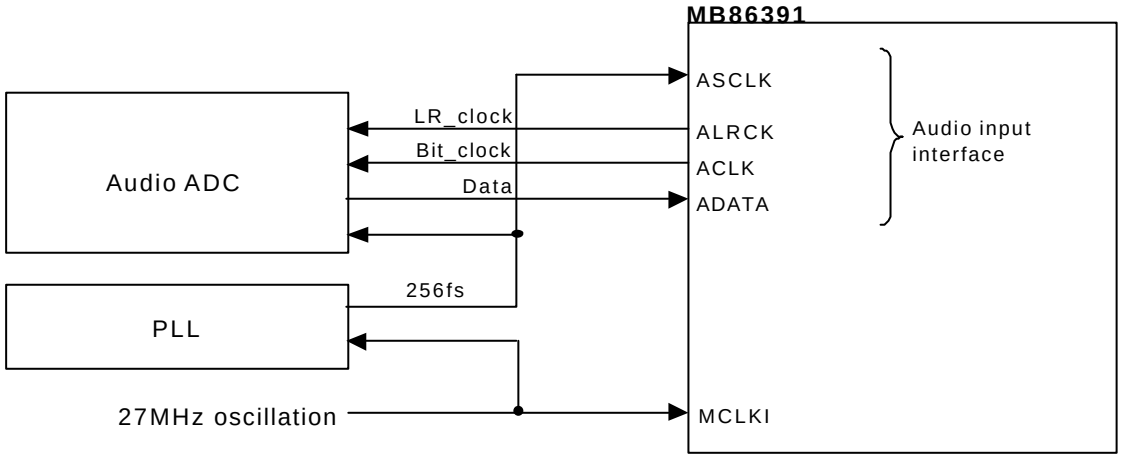
3.5 Audio Input Interface

The audio input interface is a dedicated audio data interface between the MB86391 and the audio A/D converter connected to the MB86391. Fig. 3.5 shows an example connection.



Note: MCLKI must be in sync with ASCLK.

Fig. 3.5: Example audio input interface connection (Master mode)



Note: MCLKI must be in sync with ASCLK.

Fig. 3.5: Example audio input interface connection (Slave mode)

3.5.1 Master/Slave Mode

Master (the MB86391 outputs ACLK and ALRCK) and slave (input of ACLK and ALRCK from the audio A/D converter to the MB86391) modes can be switched.

3.5.2 Input Formats

Setting each of the following parameters allows compatibility with various input formats:

(1) MSB first/LSB first of data

(2) Packing ALRCK with data (left/right packing))

(3) ALRCK polarity ('H'=Lch, 'L'=Rch / 'L'=Lch 'H'=Rch)

(4) Phase relationship between ALRCK and data (compatible with I^2S interface)

The phase relationship between ALRCK and ACLK is adjustable by 256 fs in master mode.

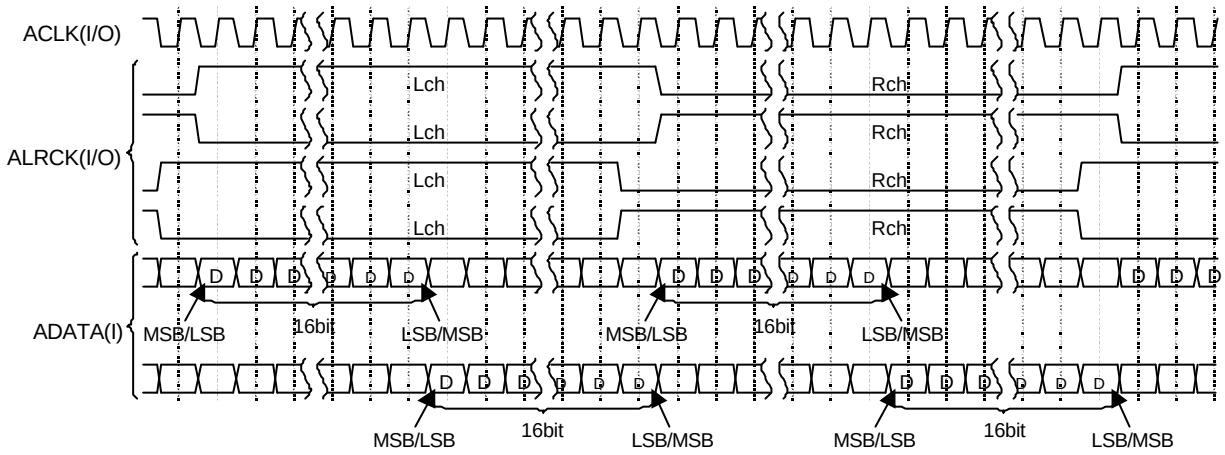


Fig. 3.5.2: Input formats

3.6 Bit Stream Output Port

The bit stream output port is compatible with various transfer modes described next:

(a) 27 MHz sync mode

This mode is for storage function products. The PCR(SCR) is made by the calculated value from bit-stream and datasize.

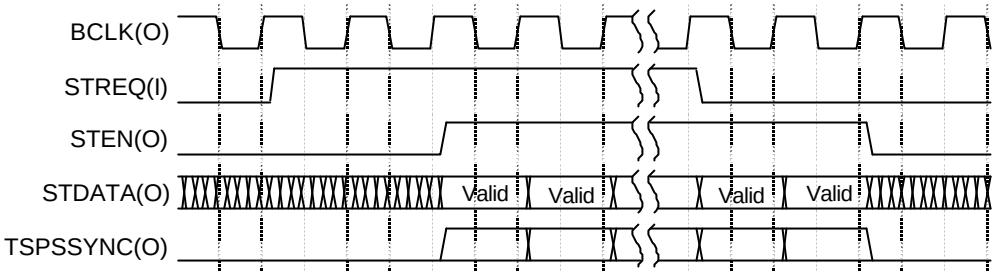


Fig. 3.6a: 27 MHz sync mode timings

(1) When ready to receive streams, set STREQ to 'H.'

(2) When valid data exists, the MB86391 sets STEN to 'H' at STDATA to instruct data fetching. It also sets the TSPSSYNC signal simultaneously to 'H' at the sync byte "0x47" if the stream is TS, and at pack start code "0x000001BA" or at the leading byte of the program end code "0x000001B9" if the stream is PS.

Notes: There is an instance during which two pieces of data are output at maximum even if STREQ is set 'L.'
Limit the duration during which STREQ is set to 'L' while encoding to a few tens of clocks. The bit rate must also be maintained on the average (The MB86391 is equipped with an internal buffer to temporarily store bit streams. However, the buffer fails if bit streams are not read for a lengthy period of time.)

(b) Handshake mode

This mode is for storage function products. The PCR(SCR) is made by the calculated value from bit-stream and datasize.

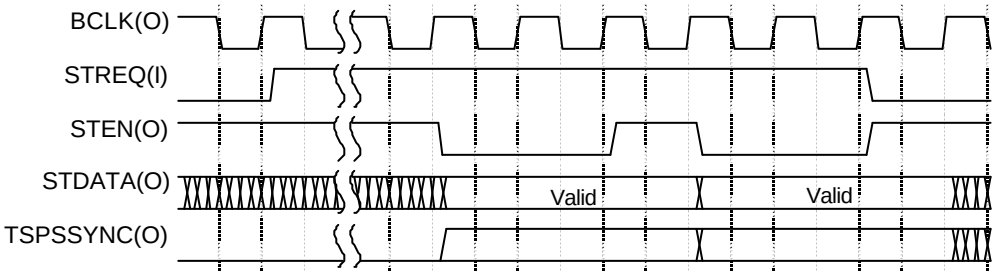


Fig. 3.6b: Handshake mode timings

(1) When ready to receive streams, set STREQ to 'H.'

(2) When valid data exists, the MB86391 changes STEN 'H'→'L' →'H' at STDATA. It simultaneously sets the TSPSSYNC signal to 'H' at the sync byte "0x47" if the stream is TS, and at the pack start code "0x000001BA" or at the leading byte of the program end code "0x 000001B9" if the stream is PS.

Note: Limit the duration during which STREQ is set to 'L' while encoding to a few tens of clocks. The bit rate must also be maintained on the average (The MB86391 is equipped with an internal buffer to temporarily store bit streams. However, the buffer fails if bit streams are not read for a lengthy period of time.)

(c) External clock sync mode(CBR)

This mode is for real time transfer function products. The PCR(SCR) is made by STCLK.

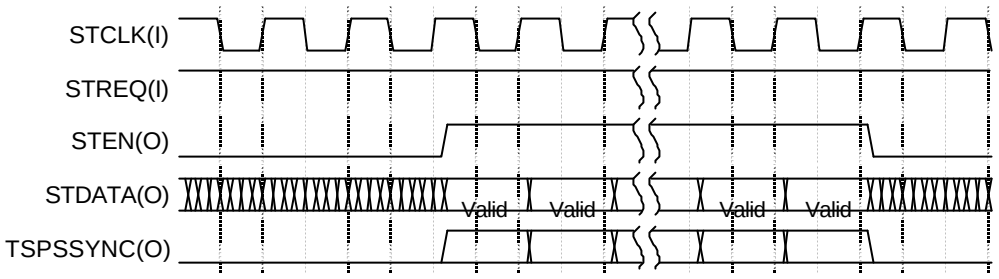


Fig. 3.6c: External clock mode (CBR)

(1) Input the transfer clock to STCLK according to the bit and set STREQ to 'H.'

(2) While transferring, the MB86391 outputs 'H' to STEN at all times and outputs valid data according to the external clock STCLK. It also simultaneously sets the TSPSSYNC signal to 'H' at the sync byte "0x47" if the stream is TS, and at the pack start code "0x000001BA" or at the leading byte of the program end code "0x000001B9" if the stream is PS.

Note: STCLK should be input over 1/8 x system bit-rate. (EX: When the system bit-rate is 8Mbps, STCLK should be over 1MHz.) When STCLK is more high frequency than system bit-rate which is setted, stuffing is implemented.

(d) External clock sync mode (VBR)

This mode is for real time transfer function products. The PCR(SCR) is made bySTCLK.

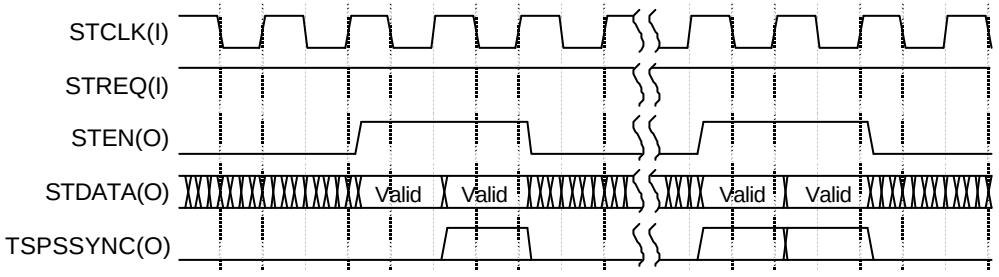


Fig. 3.6d: External clock mode (VBR)

(1) Input the transfer clock to STCLK according to the bit and set STREQ to 'H.'

(2) While transferring, the MB86391 outputs 'H' to STEN at all times and outputs valid data according to the external clock STCLK. It also simultaneously sets the TSPSSYNC signal to 'H' at the sync byte "0x47" if the stream is TS, and at the pack start code "0x000001BA" or at the leading byte of the program end code "0x000001B9" if the stream is PS.

Note: Stuffing is implemented as necessary.

3.7 Error Notification Function

The MB86391 has a built–in function to notify outside of an error when it occurs. In case of an error, it sets the XERROR pin to 'L' to output error information from the bit stream output port. When the error information is output, the STEN and TSPSSYNC pins are set to 'L' (Fig.3.7). Tables 3.7a and 3.7b list the pins and error descriptions related to occurrence of errors.

Table 3.7a: Error list

Pin status											Error description
XERROR	STDATA								STEN	TSPSSYNC	
	7	6	5	4	3	2	1	0			
1	–	–	–	–	–	–	–	–	–	–	No error (normal stream output)
0	0	0	1	Sub–error code					0	0	Timeout error
0	0	1	0	Sub–error code					0	0	External illegal access error
0	1	0	0	Sub–error code					0	0	Program error

Table 3.7b: Sub- error code list

Sub- error code					Description
0	0	0	0	0	Reset status
0	0	0	0	1	Firmware startup
0	0	0	1	0	Reserved
to					
0	1	1	1	1	
1	0	0	0	0	Boot complete
1	0	0	0	1	Boot in progress
1	0	0	1	0	Boot mode error
1	0	0	1	1	Boot header keyword error
1	0	1	0	0	Boot header checksum error
1	0	1	0	1	Data block header keyword error
1	0	1	1	0	Data block header checksum error
1	0	1	1	1	Data block checksum error
1	1	0	0	0	Reserved
to					
1	1	1	1	1	

Note: Being dependent on the firmware, this code is subject to change and addition.

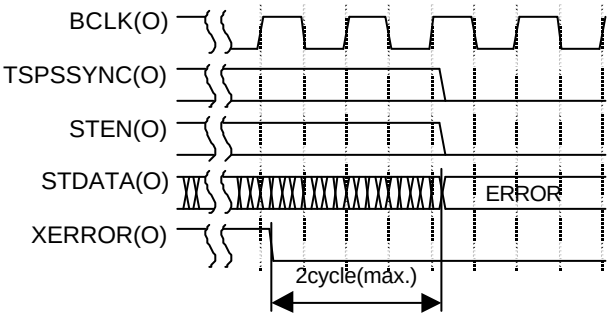


Fig. 3.7: Error information output timings

3.8 Boot Operations

The MB86391 starts booting operations when the internal controller starts the boot program of the internal ROM. The program required for the operation is downloaded to the SDRAM interface connected to the host/SDRAM according to the processing flow in Fig. 3.8. Each downloading procedure is described in the next and subsequent chapters.

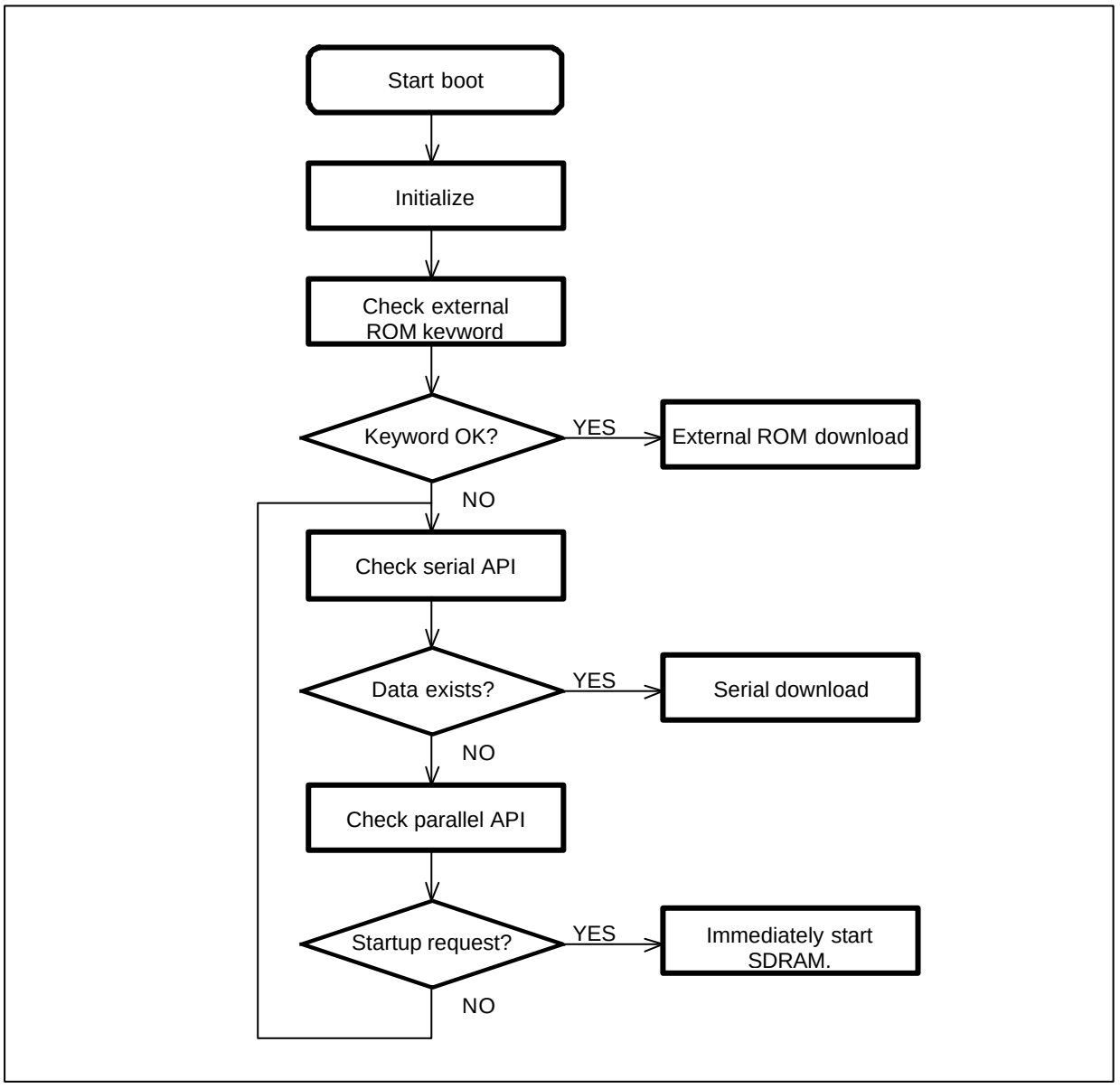


Fig. 3.8: Booting flow

3.8.1 Downloading from the External ROM

This mode downloads the program from an external ROM to the SDRAM. When the boot program of the internal ROM confirms of the external ROM, start downloading from the external ROM to SDRAM via MB86391. After downloading, MB86391 starts the program on SDRAM.

When the existence of an external ROM is confirmed, the program re−sets the wait count specified with "wait" in the header to download the data to be downloaded. The download data configuration is not dependent on the ROM bus width.

3.8.2 Serial Download

The internal ROM boot program of the MB86391 sets to either serial API or SDRAM direct download mode (see Chapter 3.8.3) if it confirms that there is no external ROM.

Upon arrival of an interrupt from the serial interface, the internal ROM boot program of the MB86391 receives the data transferred with the serial interface and, if the header of this data is configured as shown in Table 3.8.2a, downloads it as serial API.

The internal serial interface of the MB86391 supports Data32 and ASCII send and receive data formats (see Chapter 3.2). Since data can also be sent with SCLK synchronization or Asynchronization (9,600bps), four types of serial booting are available (Data32/SCLK synchronization, ASCII/SCLK synchronization, Data32/Asynchonization, and ASCII/Asynchronization).

3.8.3 Direct SDRAM Downloading

The SDRAM connected to the MB86391 host/SDRAM is assigned in the CS1 space by the internal ROM boot initialization routine. From the host interface with the parallel API, the entire SDRAM area is accessible if used with a bank register. This enables to write the program and data (including the header in Table 3.8.3) from the host/SDRAM interface to the SDRAM by directly accessing the memory.

During this period, the internal ROM boot program of the MB86391 is in an infinite loop waiting for interruption. Therefore, from the host/SDRAM interface, instruct to start the program by executing parallel API interruption (by writing to the register) after direct downloading to the SDRAM is complete.

The internal ROM boot program of the MB86391 verifies that the appropriate header is in from the SDRAM leading address and then jumps to the Entry Address to start executing the program.

4 Electrical Characteristics

4.1 Maximum Ratings

Table 4.1: Maximum ratings

Item	Symbol	Max. ratings	Unit
Supply voltage*1	VDDI	−0.5 to 2.5	V
	VDDE	−0.5 to 4.0	
	AVDD	−0.5 to 2.5	
Input voltage	VI	−0.5 to VDDE+0.5 (≤4.0)	V
Output voltage	VO	−0.5 to VDDE+0.5 (≤4.0)	V
Output current	IO	+13/−13	mA
Operating temperature	Ta	-20 to 85	°C
Storage temperature	TST	−55 to 125	°C

*1: VDDI – Internal logic power supply, VDDE – External I/O power supply, AVDD – PLL power supply

4.2 Recommended Operating Conditions

4.2.1 Recommended Operating Conditions

Table 4.2.1: Recommended operating conditions

Item		Symbol	Ratings			Unit
			Min.	Typical	Max.	
Supply voltage		VDDI	1.65	1.8	1.95	V
		VDDE	3.0	3.3	3.6	
		AVDD	1.65	1.8	1.95	
H–level input voltage	3.3V	VIH	2.0	–	VDDE+0.3	V
L–level input voltage	3.3V	VIL	–0.3	–	0.8	V
Operating temperature		Ta	-20	25	85	°C

4.2.2 Precautions When Connecting the Power

- Although VDDI, VDDE and AVDD can be turned on and off in any order, Fujitsu recommends the following order:
  Turning on:VDDI, AVDD(internal) → VDDE(external) → signals
  Turning off:signals → VDDE(external) → VDDI, AVDD(internal)
  Do not keep VDDE (external) alone pressed (for more than a few seconds) with VDDI and AVDD (internal) disconnected.
- The following power supply sequence applies to 5V tolerant I/O
  Before turning on the device, never input 5V input signals (observe the maximum ratings at all times). Otherwise, you might destroy the device.
- After turning on the power, keep the PLLTHR pin set to the L level for more than 2µs. Next, set the PLLTHR pin to the H level and then input the L level to the XRESET signal for more than 300µs.

4.3 DC Characteristics

Measurement conditions:VDDI=1.65 to 1.95V, VDDE=3.0 to 3.6, VSS=0.0V, Ta=-20 to 85°C

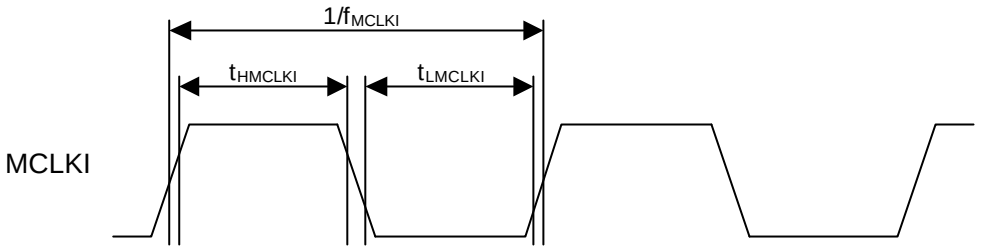
Item	Symbol	Ratings			Unit
		Min.	Typical	Max.	
H−level output voltage*1	VOH	VDDE−0.2	−	VDDE	V
L−level output voltage*2	VOL	0.0	−	0.2	V
H−level output current*3	IOH1 *6 IOH2 *5	−4.0 −8.0	−	−	mA
L−level output current*4	IOL1 *6 IOL2 *5	4.0 8.0	−	−	mA
Input leakage current	IL	−	−	+5 / −5	µA
Pull up/down resistance	Rp	10	25	70	kΩ
Pin capacity	C	−	−	16	PF

*1: Condition IOH=−100µA
*2: Condition IOL=100µA
*3: Condition VOH=VDDE−0.4V
*4: Condition VOL=0.4V
*5: BCLK, SPSDCLK, and SDCLK signal output characteristics
*6: Output characteristics of signals other than those in *5

4.4 AC Characteristics

4.4.1 Overall Control

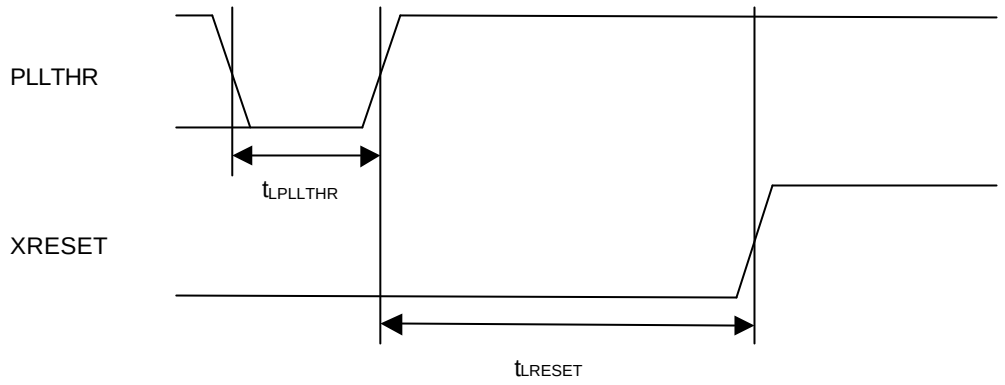
4.4.1.1 Clock Input



Item	Symbol	Condition	Standard			Unit
			Min.	Typical	Max.	
MCLKI frequency	f_{MCLKI}		–	27	–	MHz
MCLKI H duration	t_{HMCLKI}		14	–	–	ns
MCLKI L duration	t_{LMCLKI}		14	–	–	ns

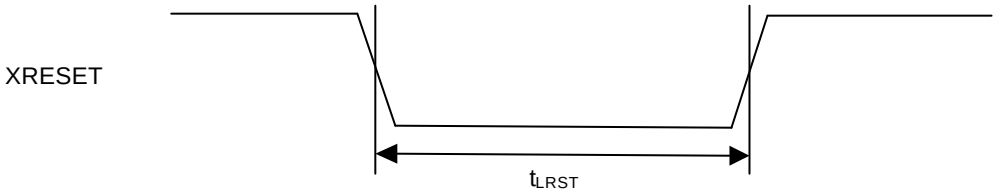
4.4.1.2 Reset Input

(a) After turning the power on



Item	Symbol	Condition	Standard			Unit
			Min.	Typical	Max.	
PLLTHR L duration	$t_{LPLLTHR}$		2	–	–	µs
XRESET L duration	t_{LRESET}		300	–	–	µs

(b) Other than after turning the power on

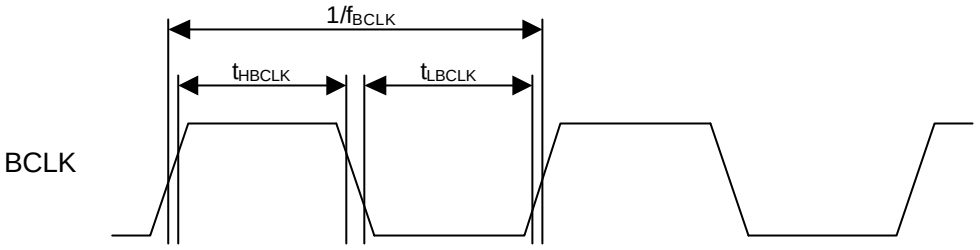


Item	Symbol	Condition	Standard			Unit
			Min.	Typical	Max.	
XRESET L duration	t_{LRST}		500	–	–	ns

4.4.2 Host/SDRAM Interface

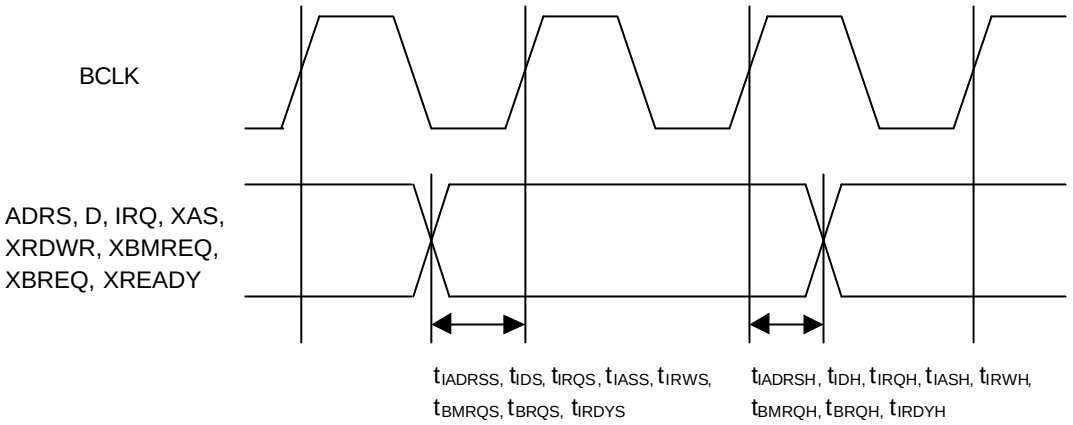
4.4.2.1 Host Interface

Clock (BCLK)

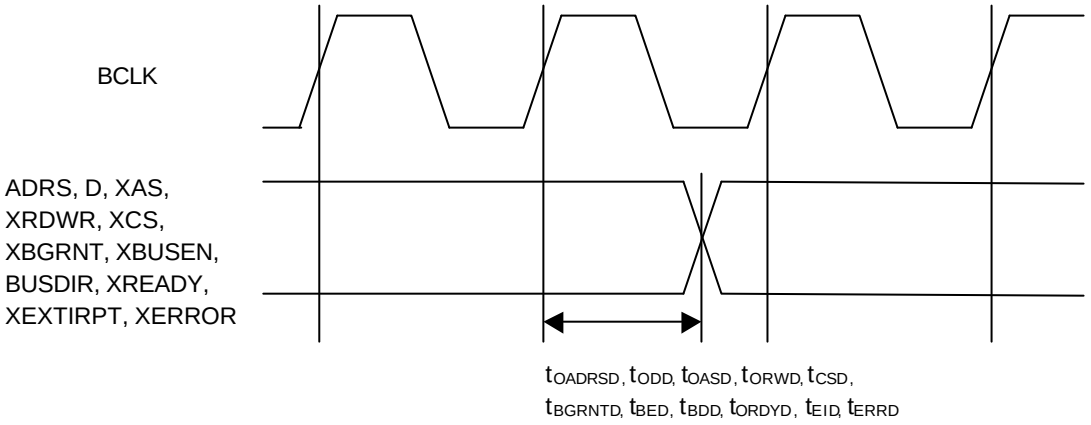


Item	Symbol	Condition	Standard			Unit
			Min.	Typical	Max.	
BCLK frequency	f_{BCLK}		–	27	–	MHz
BCLK H duration	t_{HBCLK}		13	–	–	ns
BCLK L duration	t_{LBCLK}		13	–	–	ns

Input sigals



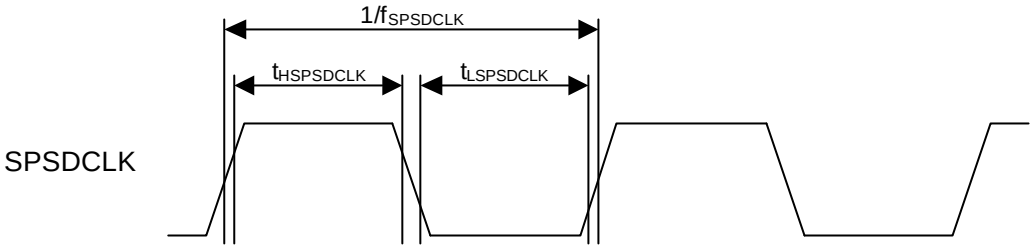
Output signals



Item	Symbol	Condition	Standard			Unit
			Min.	Typical	Max.	
Address input setup time	t_{IADRSS}		7	–	–	ns
Address input hold time	t_{IADRSH}		0.5	–	–	ns
Address output delay time	t_{OADRSD}		3	–	12	ns
Data input setup time	t_{IDS}		7.5	–	–	ns
Data input hold time	t_{IDH}		0	–	–	ns
Data output delay time	t_{ODD}		3	–	12	ns
IRQ setup time	t_{IRQS}		7	–	–	ns
IRQ hold time	t_{IRQH}		0	–	–	ns
XBREQ setup time	t_{BRQS}		7	–	–	ns
XBREQ hold time	t_{BRQH}		0	–	–	ns
XBMREQ setup time	t_{BMRQS}		7	–	–	ns
XBMREQ hold time	t_{BMRQH}		0	–	–	ns
XBGRNT delay time	t_{BGRNTD}		3	–	12	ns
XRDWR input setup time	t_{IRWS}		7	–	–	ns
XRDWR input hold time	t_{IRWH}		0	–	–	ns
XRDWR output delay time	t_{ORWD}		3	–	12	ns
XAS input setup time	t_{IASS}		7	–	–	ns
XAS input hold time	t_{IASH}		0	–	–	ns
XAS output delay time	t_{OASD}		3	–	12	ns
XCS delay time	t_{CSD}		3	–	12	ns
XREADY input setup time	t_{IRDYS}		7	–	–	ns
XREADY input hold time	t_{IRDYH}		0	–	–	ns
XREADY output delay time	t_{ORDYD}		3	–	12	ns
XBUSEN delay time	t_{BED}		3	–	12	ns
BUSDIR delay time	t_{BDD}		3	–	12	ns
XEXTIRPT delay time	t_{EID}		3	–	12	ns
XERROR delay time	t_{ERRD}		3	–	12	ns

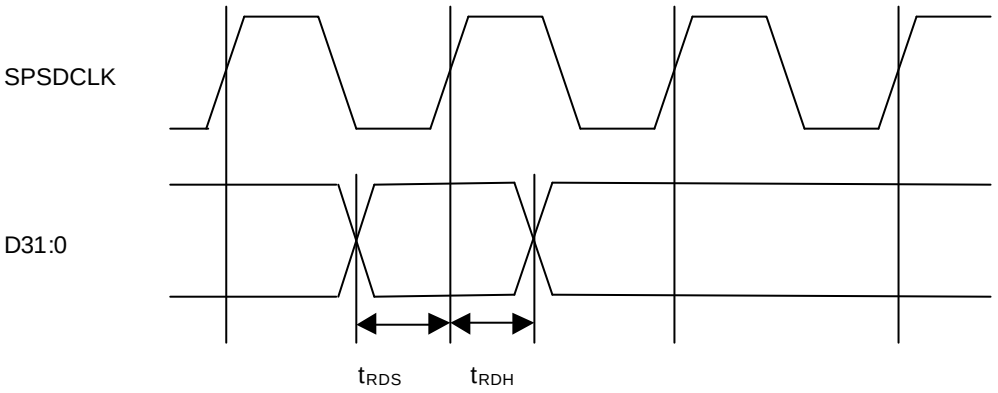
4.4.2.2 SDRAM Interface Signals

Clock (SPSDCLK)

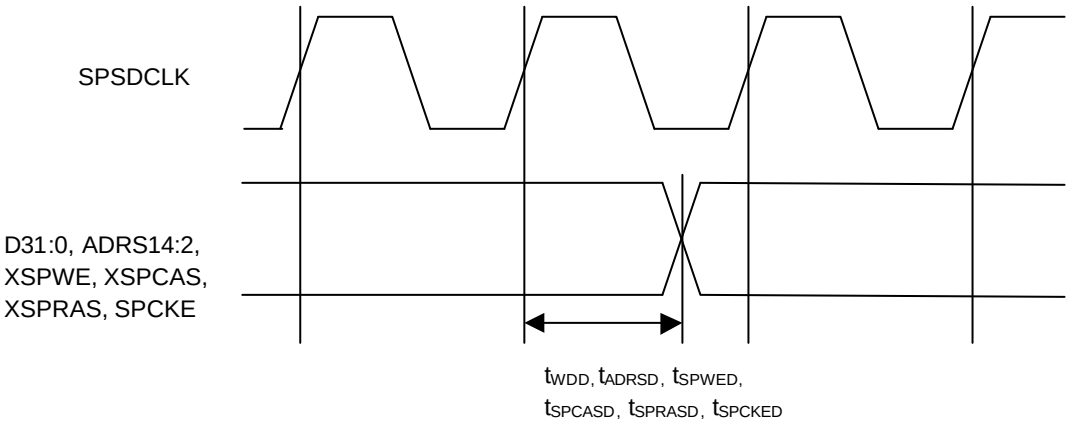


Item	Symbol	Condition	Standard			Unit
			Min.	Typical	Max.	
SPSDCLK frequency	$f_{SPSDCLK}$		–	54	–	MHz
SPSDCLK H duration	$t_{HSPSDCLK}$		6.5	–	–	ns
SPSDCLK L duration	$t_{LSPSDCLK}$		6.5	–	–	ns

Input signals



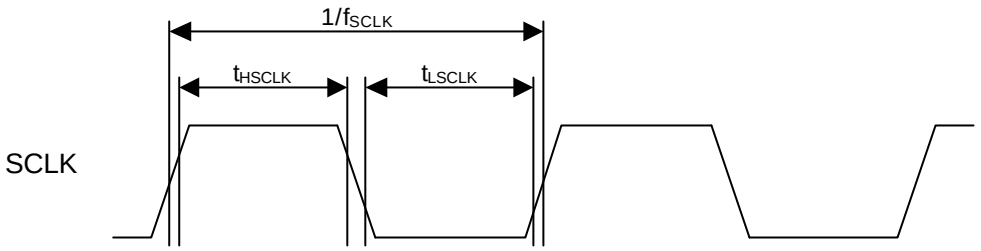
Output signals



Item	Symbol	Condition	Standard			Unit
			Min.	Typical	Max.	
Address output delay time	t_{ADRSD}		3	–	12	ns
Read data setup time	t_{RDS}		7	–	–	ns
Read data hold time	t_{RDH}		0	–	–	ns
Data output delay time	t_{WDD}		3	–	12	ns
SPWE delay time	t_{SPWED}		3	–	12	ns
SPCAS delay time	t_{SPCASD}		3	–	12	ns
SPRAS delay time	t_{SPRASD}		3	–	12	ns
SPCKE delay time	t_{SPCKED}		3	–	12	ns

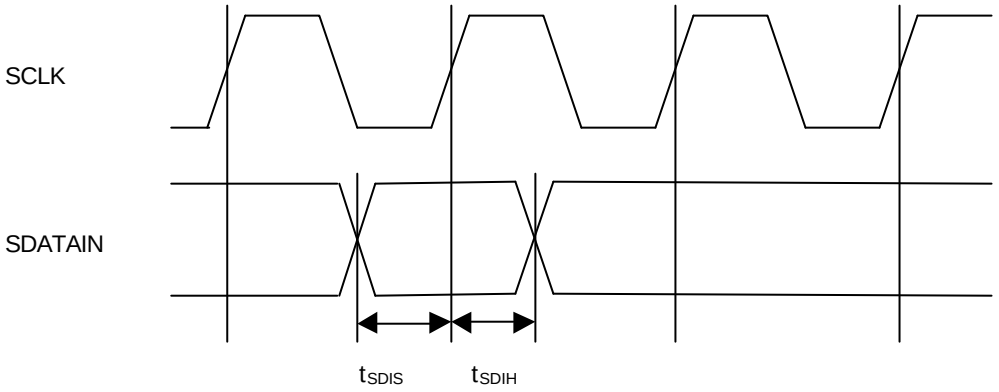
4.4.3 Serial Interface

Clock (SCLK)

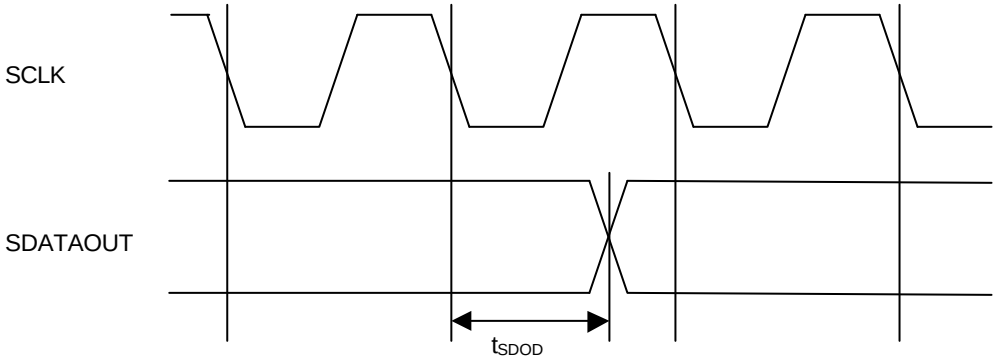


Item	Symbol	Condition	Standard			Unit
			Min.	Typical	Max.	
SCLK frequency	f_{SCLK}		–	–	2	MHz
SCLK H duration	t_{HSCLK}		200	–	–	ns
SCLK L duration	t_{LSCLK}		200	–	–	ns

Input signals



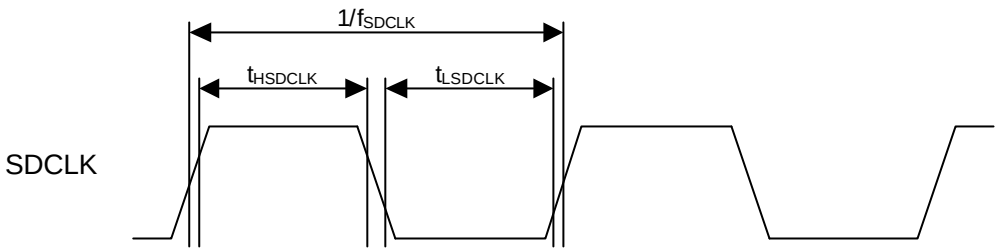
Output signals



Item	Symbol	Condition	Standard			Unit
			Min.	Typical	Max.	
Serial data input setup time	t_{SDIS}		100	–	–	ns
Serial data input hold time	t_{SDIH}		100	–	–	ns
Serial data output delay time	t_{SDOD}		–	–	160	ns

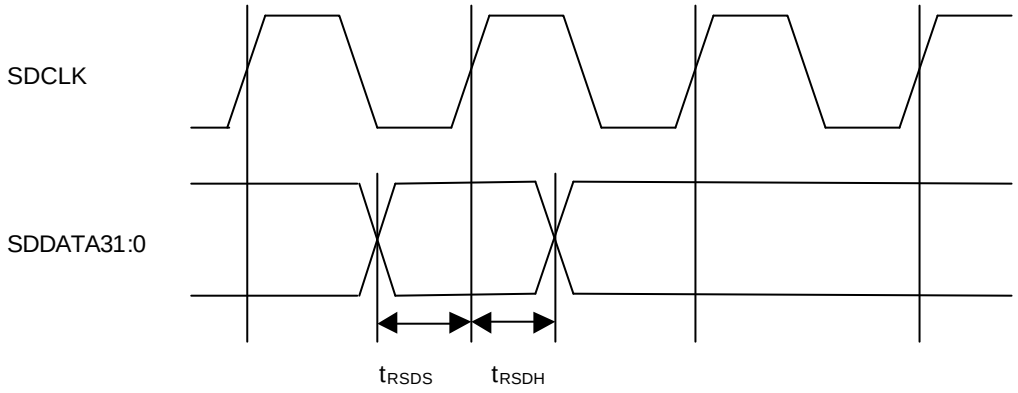
4.4.4 SDRAM Interface for Video Encoding

Clock (SDCLK)

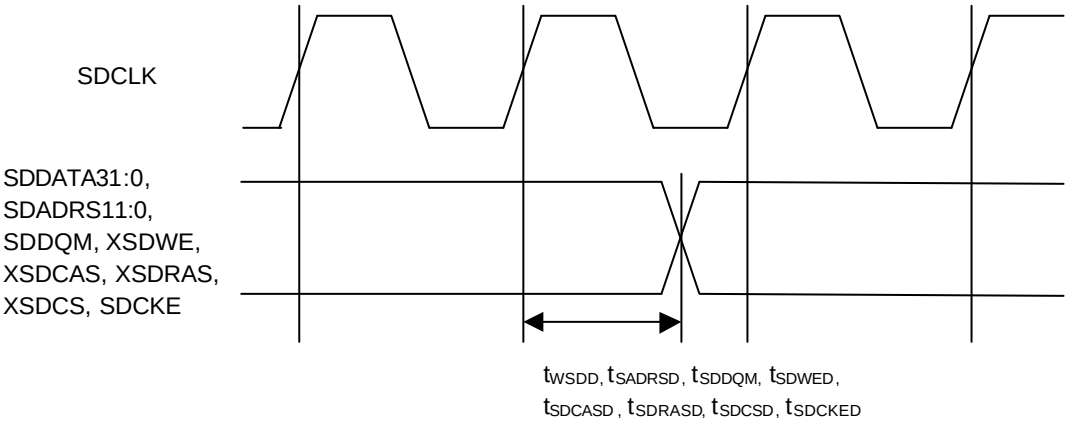


Item	Symbol	Condition	Standard			Unit
			Min.	Typical	Max.	
SDCLK frequency	f_{SDCLK}		–	–	54	MHz
SDCLK H duration	t_{HSDCLK}		6.5	–	–	ns
SDCLK L duration	t_{LSDCLK}		6.5	–	–	ns

Input signals



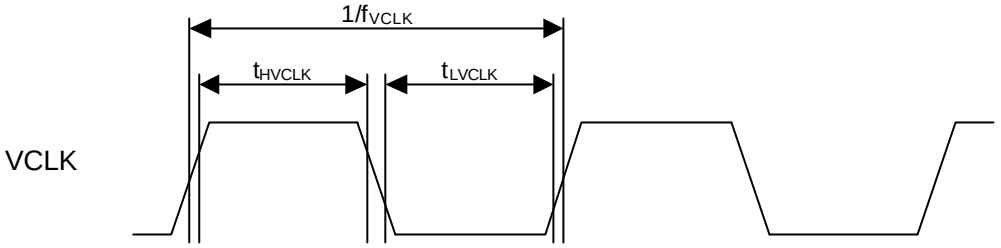
Output signals



Item	Symbol	Condition	Standard			Unit
			Min.	Typical	Max.	
Address output delay time	t_{SADRSD}		3.5	–	13	ns
Read data setup time	t_{RSDS}		5.5	–	–	ns
Read data hold time	t_{RSDH}		0	–	–	ns
Data output delay time	t_{WSDD}		3.5	–	13	ns
XSDDQM delay time	t_{SDDQM}		3.5	–	13	ns
XSDWE delay time	t_{SDWED}		3.5	–	13	ns
XSDCAS delay time	t_{SDCASD}		3.5	–	13	ns
XSDRAS delay time	t_{SDRASD}		3.5	–	13	ns
XSDCS delay time	t_{SDCSD}		3.5	–	13	ns
XSDCKE delay time	t_{SDCKED}		3.5	–	13	ns

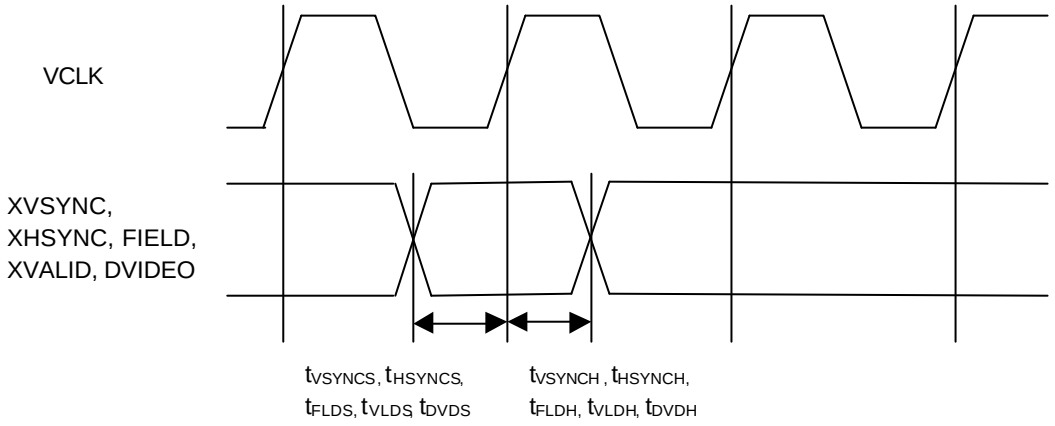
4.4.5 Video Input Interface

Clock (VCLK)



Item	Symbol	Condition	Standard			Unit
			Min.	Typical	Max.	
VCLK frequency	f_{VCLK}		27	–	36	MHz
VCLK H duration	t_{HVCLK}		11	–	–	ns
VCLK L duration	t_{LVCLK}		11	–	–	ns

Input signal

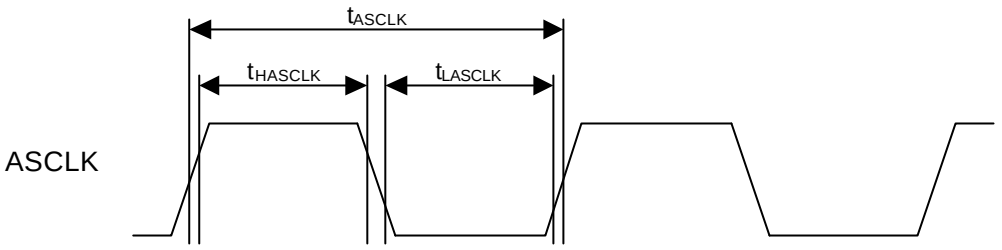


Item	Symbol	Condition	Standard			Unit
			Min.	Typical	Max.	
XVSYNC setup time	t_{VSYNCS}		10	–	–	ns
XVSYNC hold time	t_{VSYNCH}		0	–	–	ns
XHSYNC setup time	t_{HSYNCS}		10	–	–	ns
XHSYNC hold time	t_{HSYNCH}		0	–	–	ns
FIELD setup time	t_{FLDS}		10	–	–	ns
FIELD hold time	t_{FLDH}		0	–	–	ns
XVALID setup time	t_{VLDS}		10	–	–	ns
XVALID hold time	t_{VLDH}		0	–	–	ns
DVIDEO setup time	t_{DVDS}		10	–	–	ns
DVIDEO hold time	t_{DVDH}		0	–	–	ns

4.4.6 Audio Input Interface

(a) In master mode

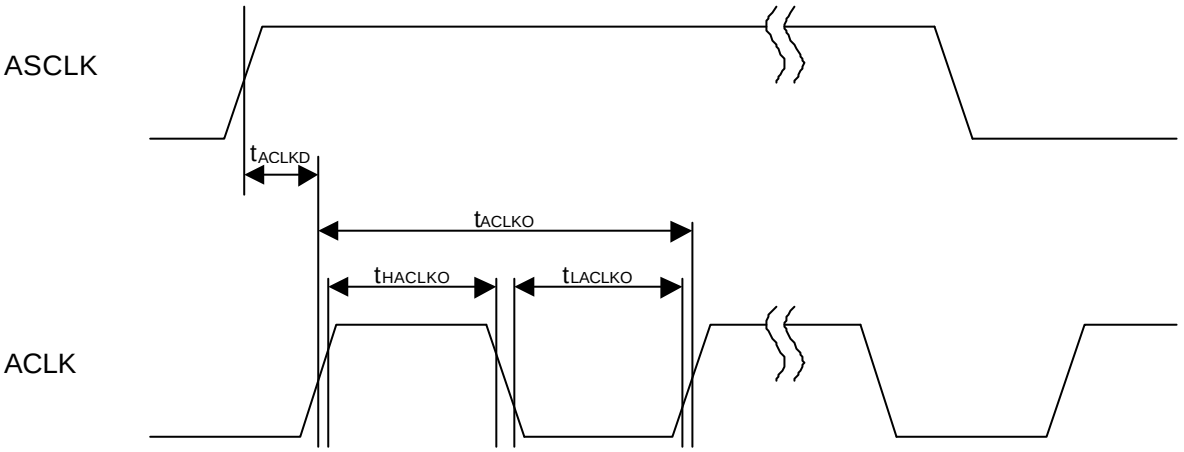
System clock input (ASCLK)



Item	Symbol	Condition	Standard			Unit
			Min.	Typical	Max.	
ASCLK frequency	t_{ASCLK}		–	1/256fs	–	ns
ASCLK H duration	t_{HASCLK}		30	–	–	ns
ASCLK L duration	t_{LASCLK}		30	–	–	ns

Note: fs: Audio sampling frequency

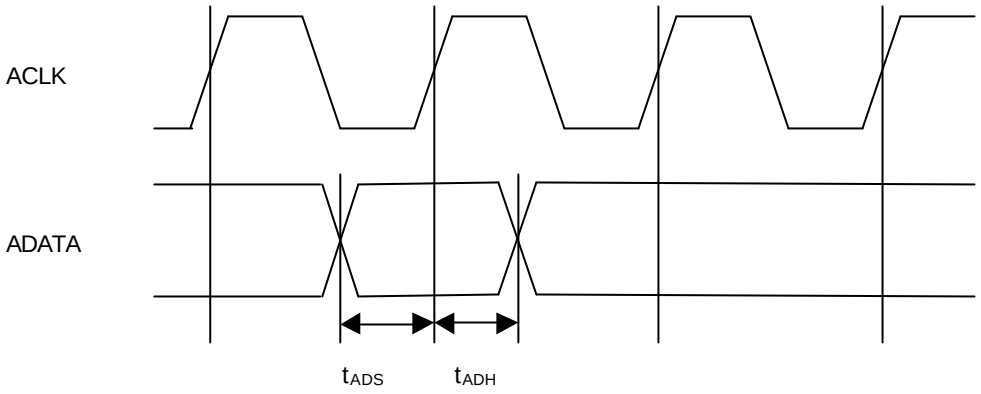
Audio bit clock output (ACLK)



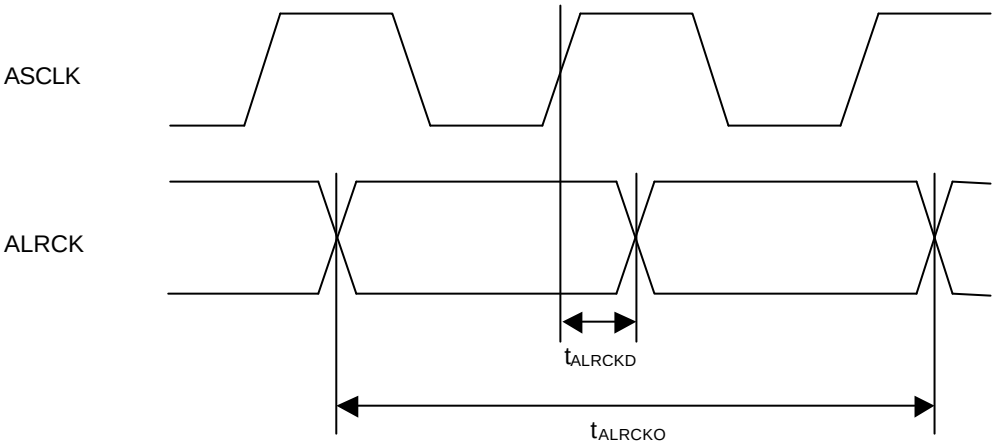
Item	Symbol	Condition	Standard			Unit
			Min.	Typical	Max.	
ACLK frequency	t_{ACLKO}		–	1/64fs	–	ns
ACLK H duration	t_{HACLKO}		135	–	–	ns
ACLK L duration	t_{LACLKO}		135	–	–	ns
ACLK delay time	t_{ACLKD}		3	–	15	ns

Note: fs: Audio sampling frequency

Serial audio data input signals



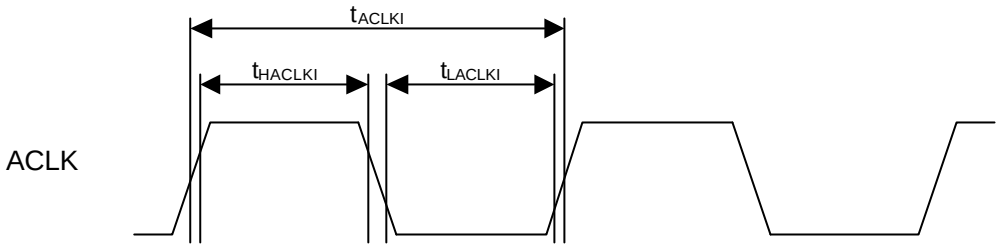
Audio sampling clock output signals



Item	Symbol	Condition	Standard			Unit
			Min.	Typical	Max.	
ADATA setup time	t_{ADS}		50			ns
ADATA hold time	t_{ADH}		50			ns
ALRCK cycle time	t_{ALRCKO}		20			µs
ALRCK delay time	t_{ALRCKD}		3		15	ns

(b) In slave mode

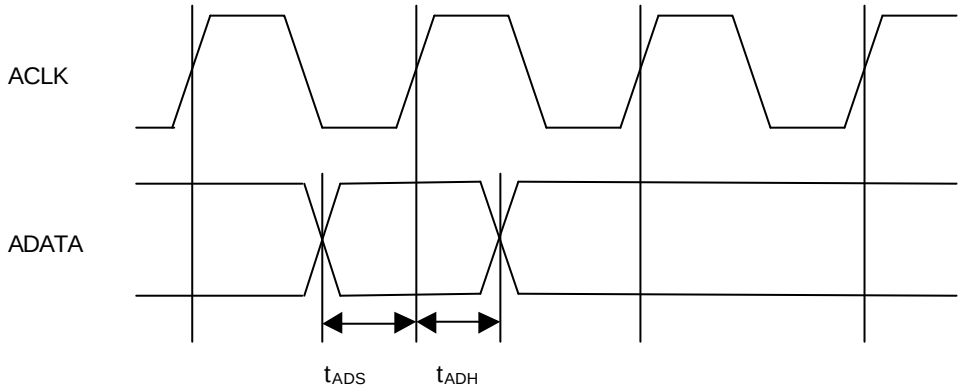
Audio bit clock input (ACLK)



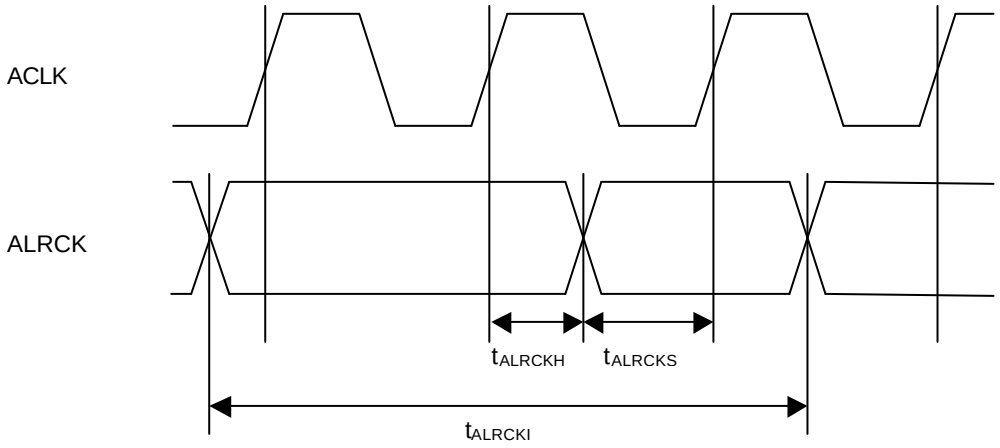
Item	Symbol	Condition	Standard			Unit
			Min.	Typical	Max.	
ACLK cycle duration	t_{ACLKI}		–	1/64fs	–	ns
ACLK H duration	t_{HSDCLK}		135	–	–	ns
ACLK L duration	t_{LSDCLK}		135	–	–	ns

Note: fs: Audio sampling frequency

Serial audio data input signals



Audio sampling clock input signals

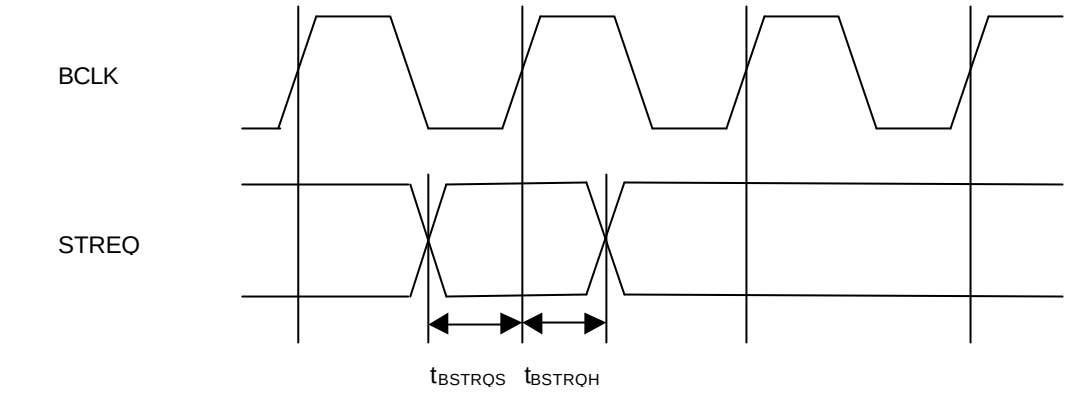


Item	Symbol	Condition	Standard			Unit
			Min.	Typical	Max.	
ADATA setup time	t_{ADS}		50			ns
ADATA hold time	t_{ADH}		50			ns
ALRCK cycle time	t_{ALRCKI}		20			µs
ALRCK setup time	t_{ALRCKS}		50			ns
ALRCK hold time	t_{ALRCKH}		50			ns

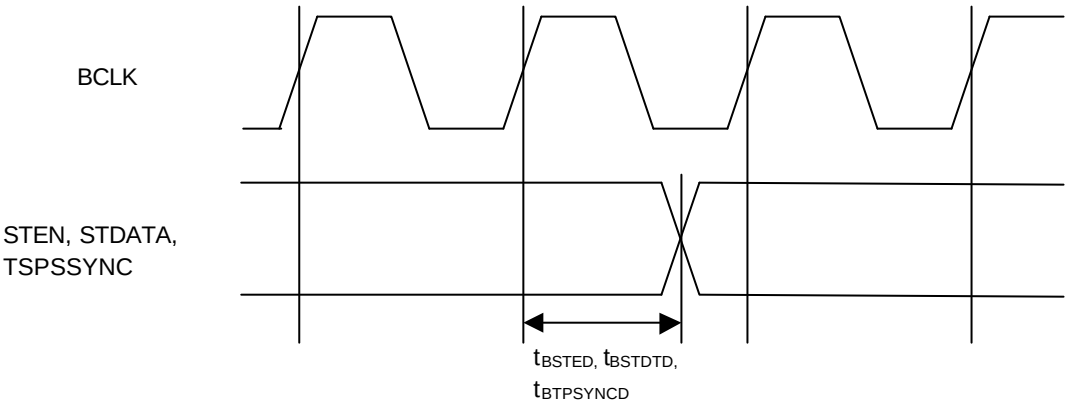
4.4.7 Bit Stream Output Port

(a) 27 MHz sync/handshake mode

Input singnals



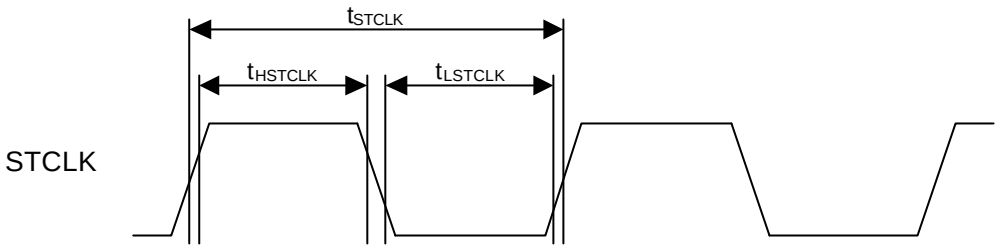
Output signals



Item	Symbol	Condition	Standard			Unit
			Min.	Typical	Max.	
STREQ setup time	t_{BSTRQS}		8			ns
STREQ hold time	t_{BSTRQH}		0			ns
STEN delay time	t_{BSTED}		5		15	ns
STDATA delay time	t_{BSTDTD}		5		15	ns
TSPSSYNC delay time	$t_{BTPSYNCD}$		5		15	ns

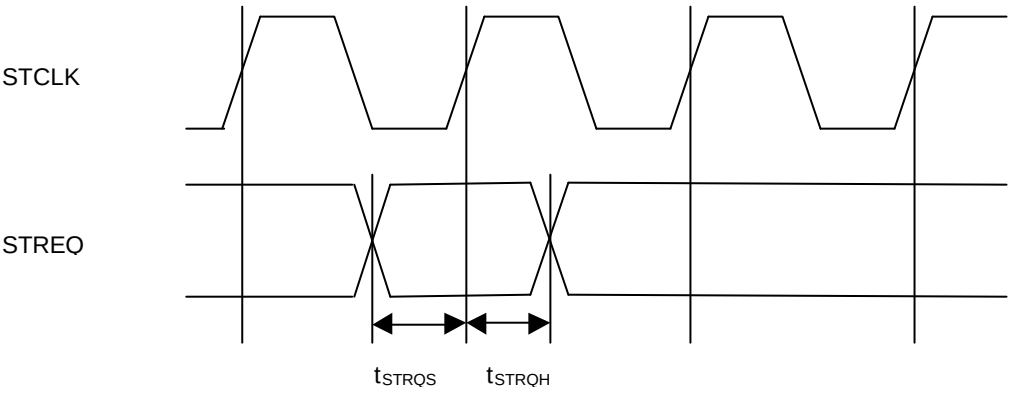
(b) Transfer clock sync mode

Clock (STCLK)

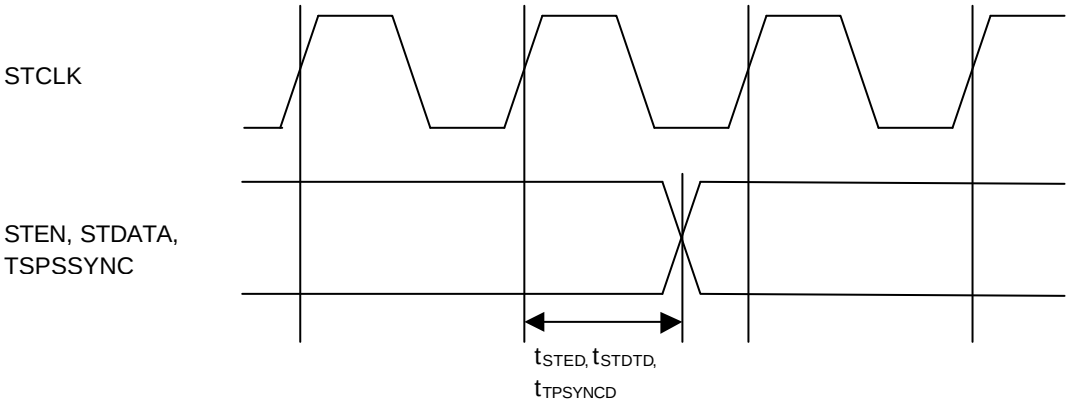


Item	Symbol	Condition	Standard			Unit
			Min.	Typical	Max.	
STCLK cycle duration	t_{STCLK}		150			ns
STCLK H duration	t_{HSTCLK}		60			ns
STCLK L duration	t_{LSTCLK}		60			ns

Input signals



Output signals



Item	Symbol	Condition	Standard			Unit
			Min.	Typical	Max.	
STREQ setup time	t_{STRQS}		0			ns
STREQ hold time	t_{STRQH}		60			ns
STEN delay time	t_{STED}				103	ns
STDATA delay time	t_{STDTD}				103	ns
TSPSSYNC delay time	$t_{TPSYNCD}$				103	ns