

CPC700 Memory Controller and PCI Bridge

High-performance companion chip for PowerPC 60x and 7xx processors

Overview

The CPC700™ Memory Controller and PCI Bridge brings high-performance, real-time control to PowerPC 60x/7xx driven designs. This single-chip micro-processor companion is specifically designed for embedded systems to provide a general purpose bridge to any PCI bus. The CPC700 companion chip also includes a high-speed memory controller, internal peripherals, and control for external ROM and external peripherals.

This CPC700 companion chip can function as a host bridge, as the basis for an intelligent add-in PCI controller, or in stand-alone modes. This versatility and the following features can help lower costs, enhance board efficiency and reduce your time-to-market.

- PowerPC 60x/7xx interface (66 MHz)
- 66 MHz SDRAM interface
- External peripheral bus
- PCI 2.1 compliant interface (32-bit, 25 to 66 MHz)
- Supports internal or external PCI bus arbitration
- Interrupt controller
- Programmable timers
- Two full-duplex UARTs (16550)
- Two I²C interfaces
- Byte swapping options ease communication in little-endian systems
- JTAG for board-level testing

General

- Extensive programmability
- Flexible and programmable error handling

Processor Interface

The PowerPC™ processor bus interface includes the interface to the system memory controller, as well as the Processor Local Bus (PLB) master/slave interface.

- 1 level processor address pipelining
- Processor bus arbiter
- L1 cache coherency support
- Two 32-byte write buffers

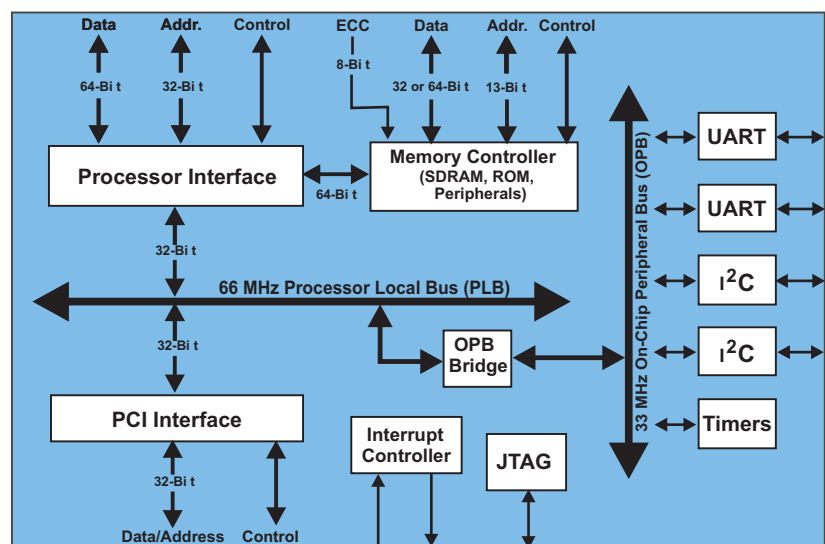
- Provides error tracking/status
- Iwarx/stwx support (reservation canceling snoops)
- Supports Address Only cycle

Memory Controller

This memory controller provides the local PowerPC processor with a low-latency access path supporting external peripherals and 5 banks of local memory.

SDRAM

- Up to 4 banks
- 11x9 to 13x11 addressing (for 2 and 4 internal bank SDRAMs)
- 8 MB to 512 MB per bank



CPC700 Block Diagram



- Programmable timings and address mapping
- CAS before RAS refresh
- ECC support across data and address
- Supports hardware coherency relative to PCI access of local memory
- Page Mode accesses
- 66 MHz memory bus frequency
- 72-bit memory interface with ECC
- Self-refresh mode support

ROM/External Peripheral

- Supports ROM, Flash ROM, SRAM, and Peripherals
- Burst and non-burst devices
- 1-5 banks (shared with SDRAM)
- 8-, 16-, 32-, and 64-bit data bus widths
- Programmable timing and address mapping
- Shared address/data/control with SDRAM interface
- External latch control for shared address bus support
- Peripheral device pacing with external "Ready"

PCI Interface

- PCI 2.1 compliant
- 32-bit PCI address/data bus
- Supports 25 to 66 MHz PCI bus speeds
- Supports processor access to all PCI address spaces

- Error tracking/status
- Support for synchronous and asynchronous clocking
- Internal PCI arbitration
- Support for fair external arbitration

Interrupt Controller

- Supports twelve (12) external interrupts
- Option for prioritized interrupt handler vector generation

UART (2)

- Compatible with the NS 16550
- 16-byte send FIFO, 16-byte receive FIFO
- Programmable baud rate generator
- Supports 5- to 8-bit word size, 1 or 2 stop bits, even/odd/no parity

I²C (2)

- 100 and 400 KHz operation
- 8-bit data transfers
- 7- and 10-bit address decode/generation
- Master/slave capability

General Purpose Timers

- 32-bit time base, based on system clock
- Five capture event timers
- Five compare timers

JTAG

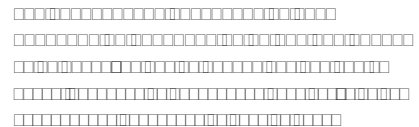
IEEE 1149.1 (JTAG) boundary scan is included to facilitate board level testing

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CPC700 Companion Chip Specifications

Technology	0.35µm (0.27µm L _{eff}) CMOS
Power Supply	3.3V +/- 5%
Temperature Range	-40°C to 105°C
Packaging	474-pin CBGA



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