

PRELIMINARY
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 some parametric limits are subject to change.

MITSUBISHI SOUND PROCESSOR LSI

M62481FP

PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

DESCRIPTION

The M62481FP is an optical pick-up servo system IC for a CD player. It has amplifiers, switches, comparators and logic controller for servo control of an optical pick-up. Furthermore, it has automatic adjustment system controlled by micro-controller. Many built-in functions and the 56pin shrink quad package realize the compact and moderate CD player with high performance.

FEATURES

- 8 times speed
- 3 beam pick-up servo system
- Adaptable to hologram pick-up system with additional input.
- Built-in automatic laser power control circuit
- Built-in mirror detector
- Built-in adjustment circuit for automatic tuning
- Built-in serial data command interface to reduce micro-controller overload
- Built-in self-reset circuit

APPLICATION

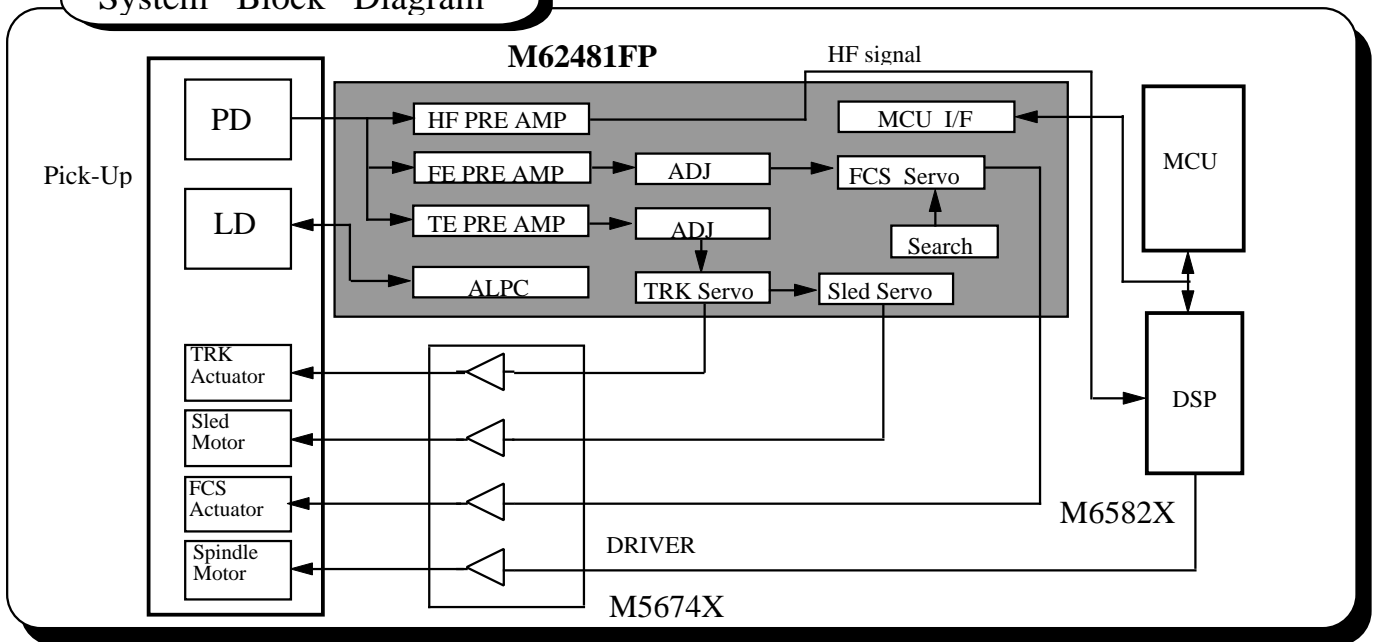
CD PLAYER, CD-ROM PLAYER

RECOMMENDED OPERATION CONDITIONS

- Supply Voltage Range 4.5 -> 5.5V
- Rated Supply Voltage 5.0V



System Block Diagram



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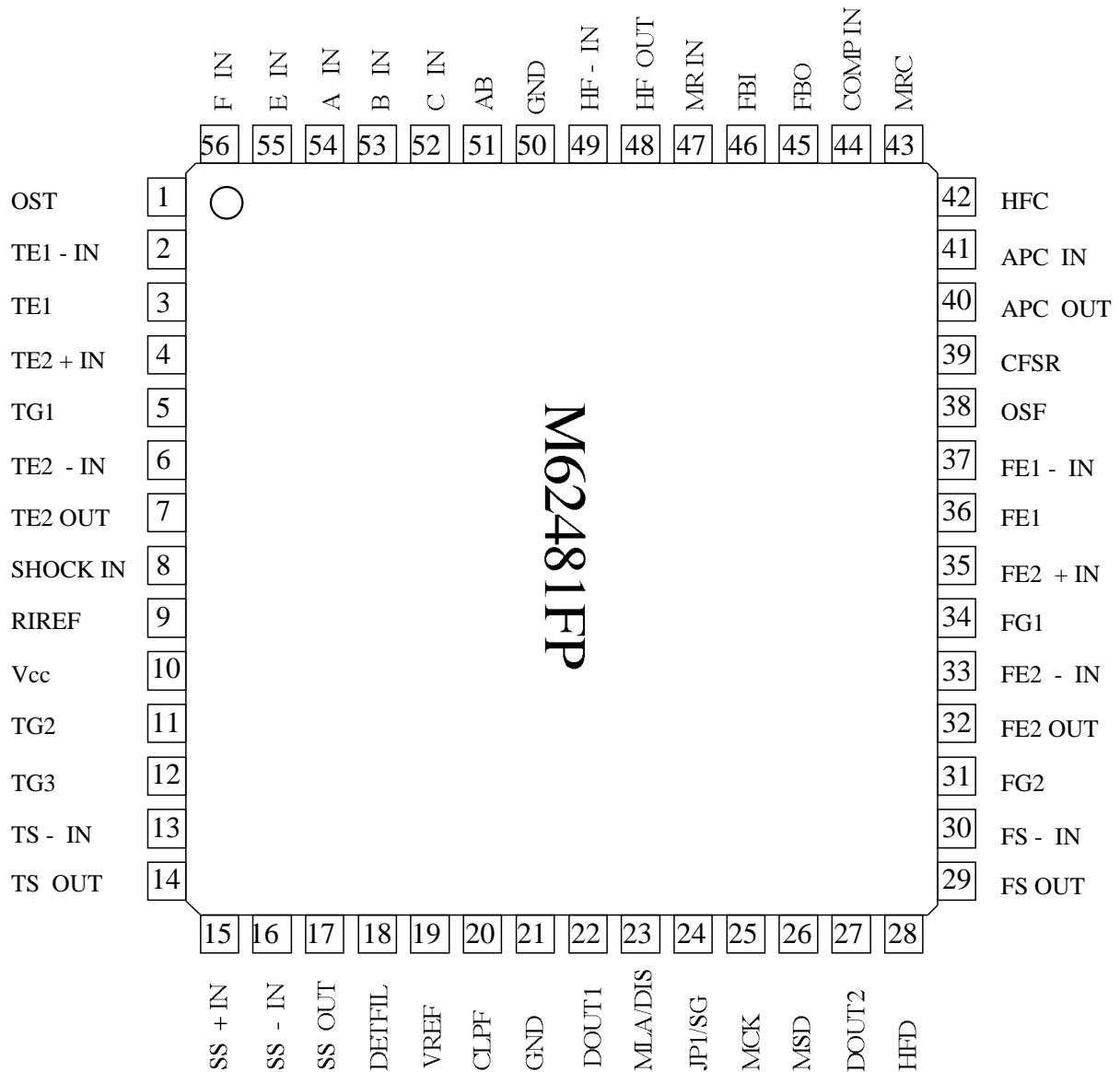
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PIN CONFIGURATION

(top view)



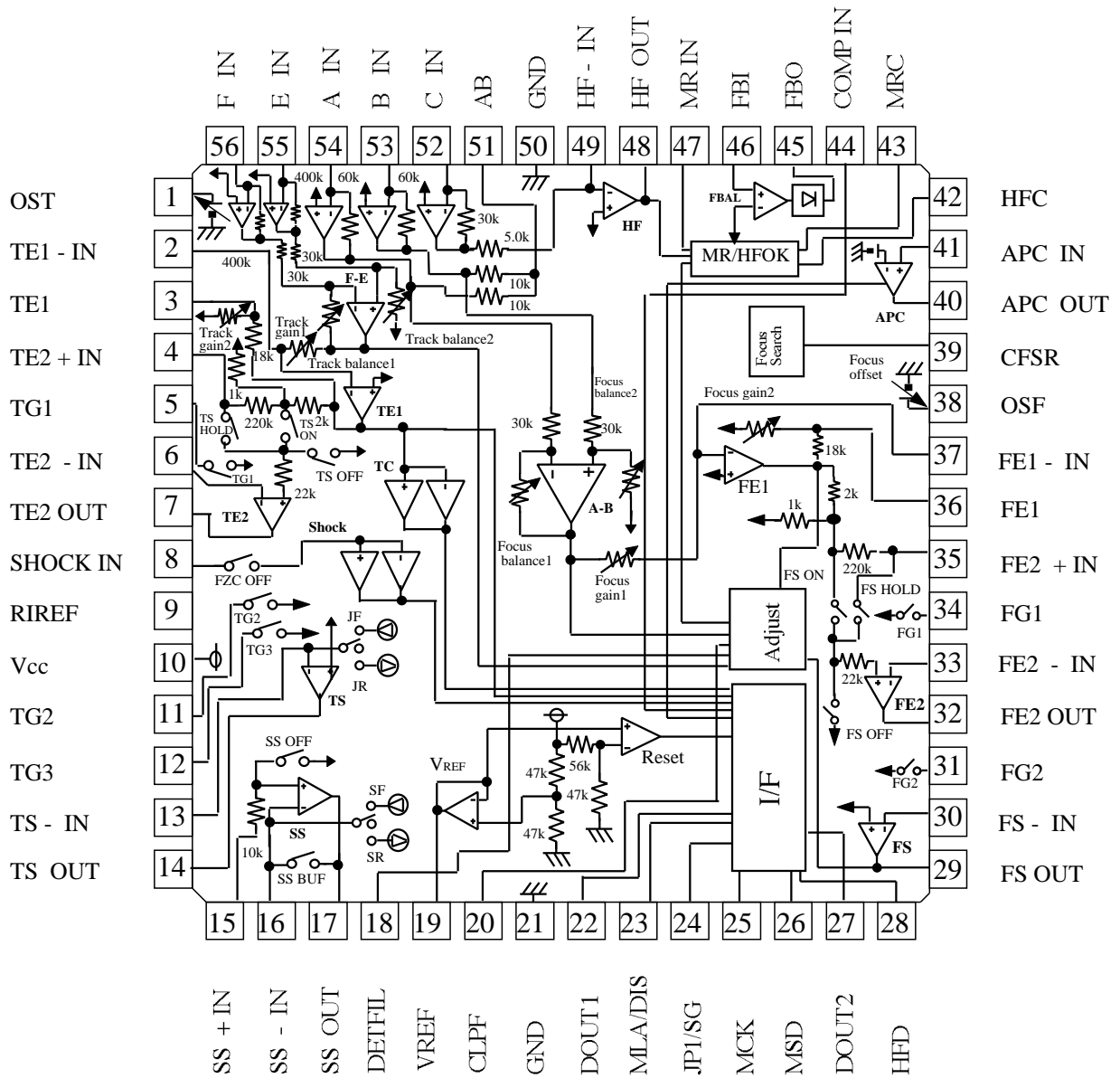
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BLOCK DIAGRAM



Unit Resistance :

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PIN DESCRIPTION

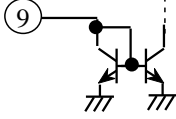
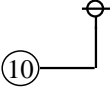
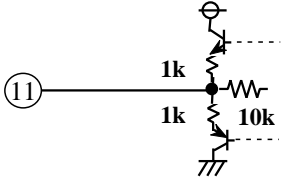
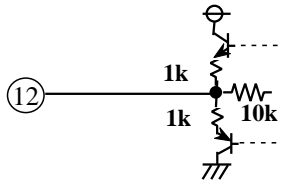
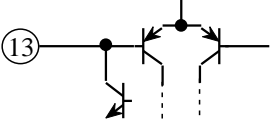
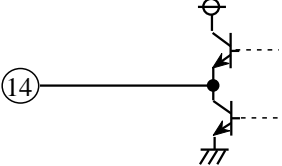
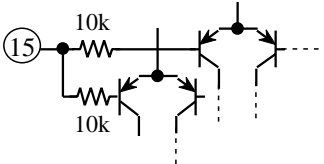
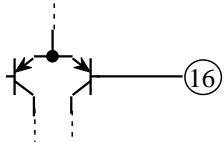
PIN No.	Symbol	Equivalent circuit	Function
1	OST		Voltage output for Track offset adjustment
2	TE1 -IN		TE1 Amp negative input
3	TE1		TE1 Amp output
4	TE2 +IN		TE2 Amp positive input
5	TG1		TG1 SW
6	TE2 -IN		TE2 Amp positive input
7	TE2 OUT		TE2 Amp output
8	SHOCK IN		Shock detector input

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PIN No.	Symbol	Equivalent circuit	Function
9	RIREF		Current reference
10	Vcc		Power supply
11	TG2		TG2 SW
12	TG3		TG3 SW
13	TS - IN		TS Amp negative input
14	TS OUT		TS Amp output
15	SS + IN		SS Amp positive input
16	SS - IN		SS Amp negative input

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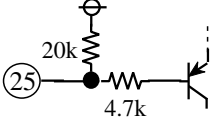
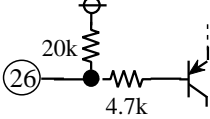
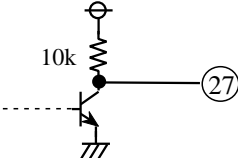
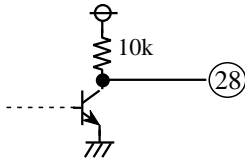
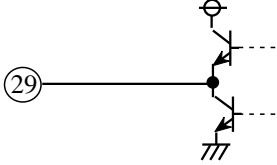
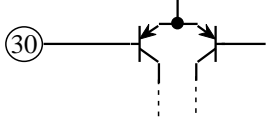
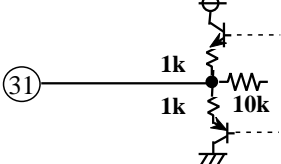
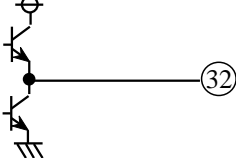
PIN No.	Symbol	Equivalent circuit	Function
17	SS OUT		SS Amp output
18	DETFIL		Filter for Phase Detector (Gain adjustment)
19	VREF		Vcc/2 Amp output
20	CLPF		LPF Capacitor for adjutment
21	GND		Ground
22	DOUT1		Servo status Data output1
23	MLA/DIS		MCU Latch Signal input (discharge control for LPF Capacitor of adjustment)
24	JP1/SG		Single Track Jump Control (reference signal input for Gain adjustment)

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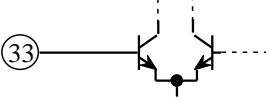
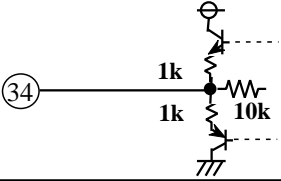
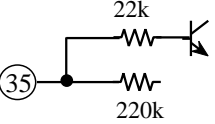
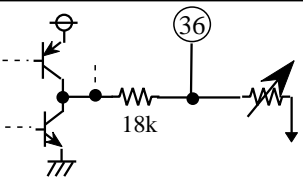
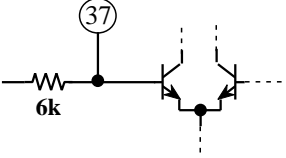
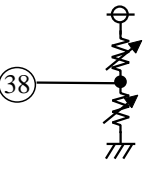
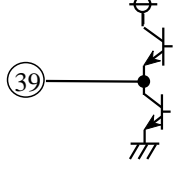
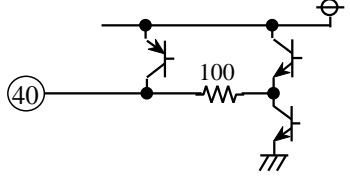
PIN No.	Symbol	Equivalent circuit	Function
25	MCK		MCU clock signal input
26	MSD		MCU serial Data input
27	DOUT2		Servo status Data output2
28	HFD		HF Detect output
29	FS OUT		FS Amp output
30	FS - IN		FS Amp negative input
31	FG2		FG2 SW
32	FE2 OUT		FE2 Amp output

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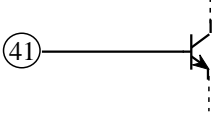
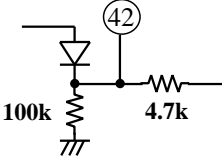
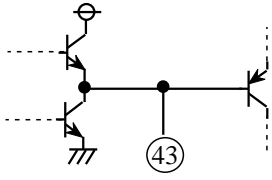
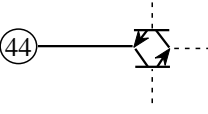
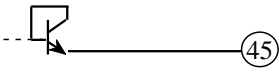
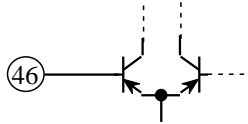
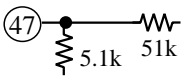
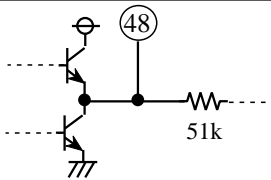
PIN No.	Symbol	Equivalent circuit	Function
33	FE2 - IN		FE2 Amp negative input
34	FG1		FG1 SW
35	FE2 + IN		FE2 Amp positive input
36	FE1		FE1 Amp output
37	FE1 - IN		FE1 Amp negative input
38	OSF		Voltage output for Focus offset adjustment
39	CFSR		Voltage for Focus Search
40	APC OUT		APC(Automatic Laser Power Control)output

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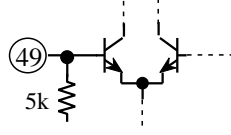

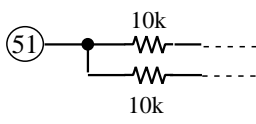
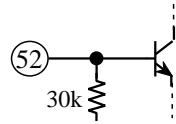
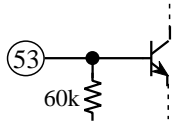
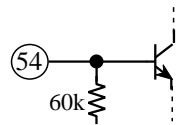
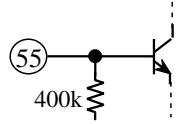
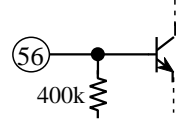
PIN No.	Symbol	Equivalent circuit	Function
41	APC IN		APC(Automatic Laser Power Control)input
42	HFC		HF Capacitor for HF Detector
43	MRC		Hold Capacitor for Mirror Detector
44	COMP IN		Comp Amp input
45	FBO		Focus Balance Amp output
46	FBI		Focus Balance Amp input
47	MR IN		Input of Mirror detector
48	HF OUT		HF Amp output

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PIN No.	Symbol	Equivalent circuit	Function
49	HF - IN		HF Amp negative input
50	GND		Ground
51	AB		A,B output
52	C IN		HF input C for Auxiliary
53	B IN		Focus Servo input B
54	A IN		Focus Servo input A
55	E IN		Track Servo input E
56	F IN		Track Servo input F

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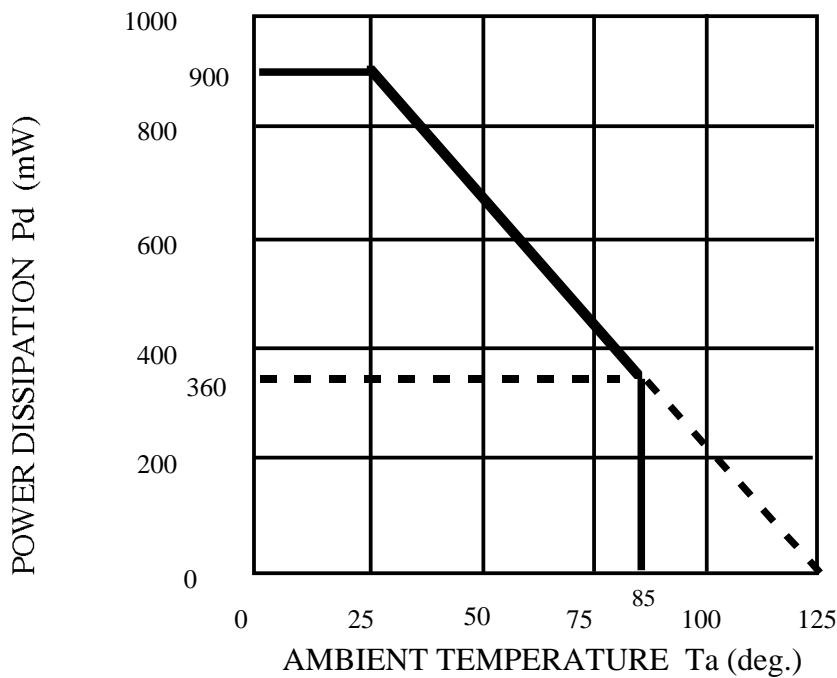
PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

ABSOLUTE MAXIMUM RATING

Ta=25deg., unless otherwise noted

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Maximum Supply Voltage		7	V
VI	Input Voltage		-0.3 -> Vcc+0.3	V
Pd	Power Dissipation		900	mW
Kθ	Thermal Derating	Ta = 25deg.	9.0	mW/deg.
Topr	Operating Temperature		-20 -> +85	deg.
Tstg	Storage Temperature		-40 -> +125	deg.

THERMAL DERATING (MAXIMUM RATING)



RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
Vcc	Supply Voltage		4.5	5.0	5.5	V
VIH	High-level Input Voltage	Pin(23), Pin(24),	Vcc -> 0.7		Vcc	V
VIL	Low-level Input Voltage	Pin(25), Pin(26)				0
fck	Clock frequency				500	kHz

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ELECTRICAL CHARACTERISTICS(1/6)

(Ta=25deg.,Vcc=5V,f=1kHz,DCBA=1000,unless otherwise noted)

No	Symbol	Block	Parameter	Test Conditions	Measurement circuit	Limit			Unit
						Min	Typ	Max	
1	Icc	—	Circuit current	Quiescent		30	55	70	mA
2	VREF		Reference voltage			2.3	2.5	2.7	V
3-1	GVHFAB	IV + HF	Gain for Input A/B	f=500kHz	(1)	3.1	5.1	7.1	dB
3-2	GVHFC		Gain for Input C	f=500kHz	(2)	9.1	11.1	13.1	dB
4-1	fHF1		HF Cut off frequency1	(normal) 3dB down refer to 500kHz	(1)	12.0	16.0	—	MHz
4-2	fHF2		HF Cut off frequency2	(Invert) 3dB down refer to 500kHz	(3)	12.0	16.0	—	MHz
5	VHHF		High output voltage	INPUT Vin= 4.0V	(4)-1	3.5	4.0	—	V
6	VLHF		Low output voltage	INPUT Vin= 1.0V	(4)-1	—	1.0	1.5	V
7	IOHHF		High output current	VOH=4.0V	(4)-2	—	-2	-1	mA
8	IOLHF		Low output current	VOL=1.0V	(4)-2	1	2	—	mA
9	VOSHF		Offset voltage	refer to VREF	(5)	-50	0	50	mV
10-1	RMN-ON		MR	Ratio(nomal)	"Normal"Mode: R0;D5=0	(6)-1	0.31	0.41	0.51
10-2	RMN-OFF	Ratio(nomal)		"Normal"Mode: R0;D5=0	(6)-1	0.37	0.47	0.57	—
10-3	RMN-HYS	Hysteresis(normal)		"Normal"Mode: R0;D5=0	(6)-1	0.03	0.06	0.12	—
11-1	RMJ-ON	Ratio(jump)		"Brake"Mode : R0;D5=1	(6)-1	0.42	0.52	0.62	—
11-2	RMJ-OFF	Ratio(jump)		"Brake"Mode : R0;D5=1	(6)-1	0.48	0.58	0.68	—
11-3	RMJ-HYS	Hysteresis(jump)		"Brake"Mode : R0;D5=1	(6)-1	0.04	0.08	0.16	—
12-1	fMRL	Cut off frequency (Low)		"Normal"Mode: R0;D5=0 , R1;D13=1	(6)-2	30	50	—	kHz
12-2	fMRH	Cut off frequency (High)		"Normal"Mode: R0;D5=0 , R1;D13=0	(6)-2	60	100	—	
13	VTHFOK	HFOK	Threshold	refer to VREF	(7)	-0.26	-0.19	-0.12	V
14	VHHFD	HFD/ DOUT1,2	High output voltage		(7)	3.5	4.0	—	V
15	VHDOUT		High output voltage						
16	VLHFD		Low output voltage		(7)	—	1.0	1.5	V
17	VLDOUT		Low output voltage						
18	IOHHFD		High output current	VOH=4.0V	(8)	—	-100	-70	uA
19	IOHDOUT		High output current	VOH=4.0V					
20	IOLHFD		Low output current	VOL=1.0V	(8)	500	1000	—	uA
21	IOLDOUT	Low output current	VOL=1.0V						

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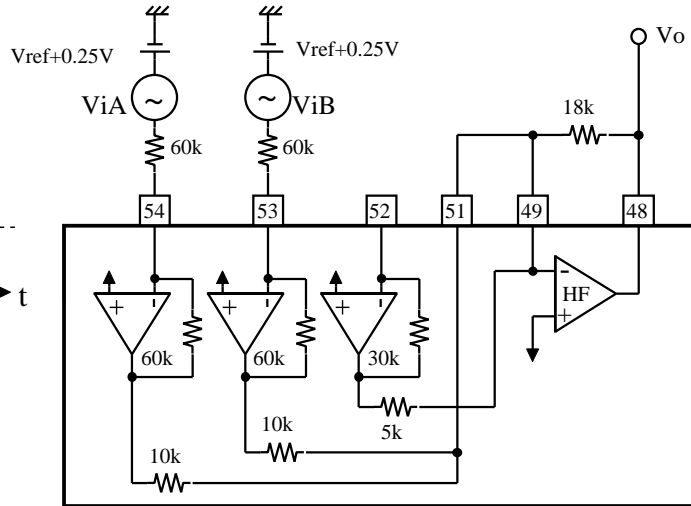
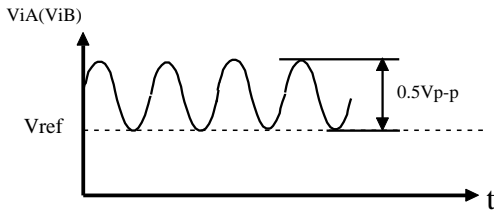
PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

note(1/6)

•IV+HF BLOCK

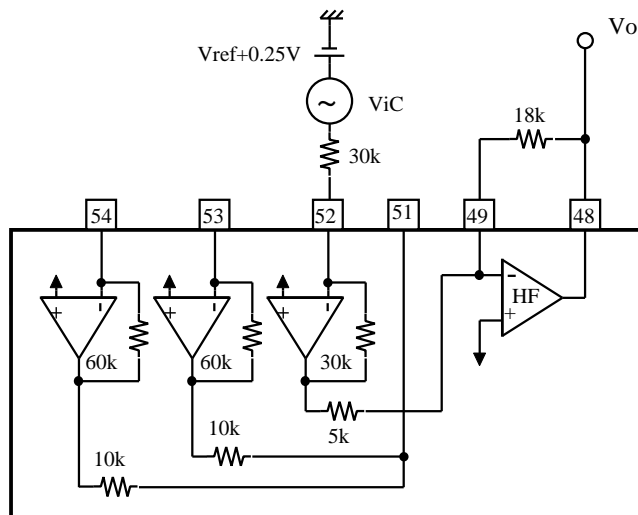
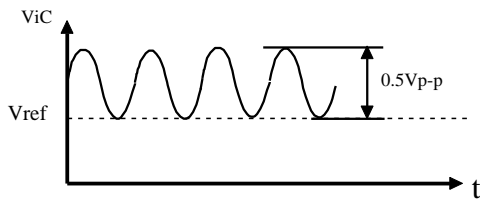
(1)GVHFAB,fHF1;

Input signal ViA (ViB)



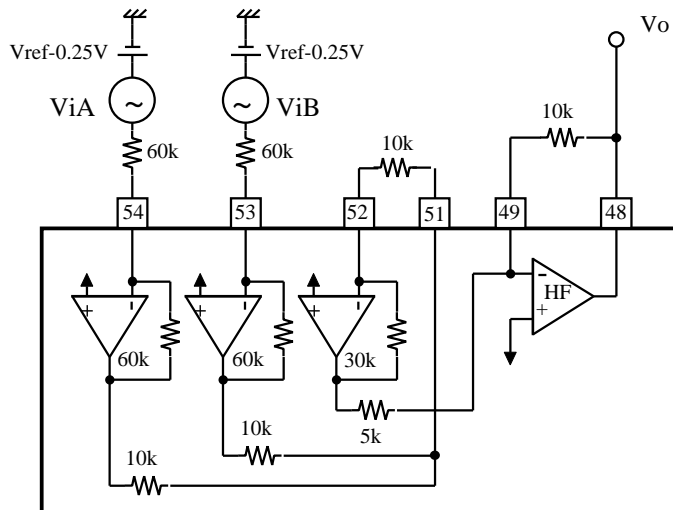
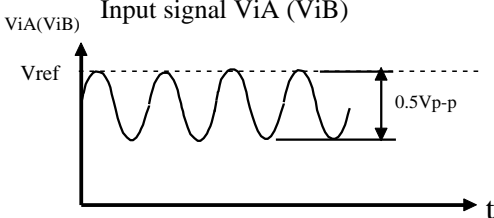
(2)GVHFC;

Input signal ViC



(3)fHF2;

Input signal ViA (ViB)



↓
 VREF=1/2Vcc

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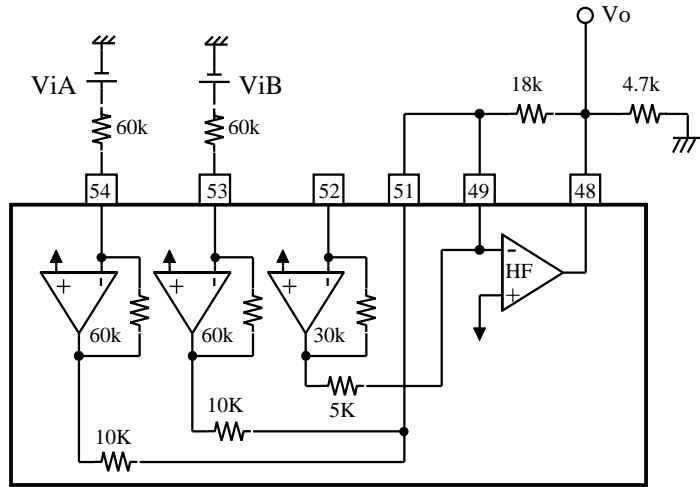
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(4)-1V_{HHF},V_{LHF};

INPUT ViA(ViB)

V_{HHF}:ViA(ViB)=4.0V

V_{LHF}:ViA(ViB)=1.0V

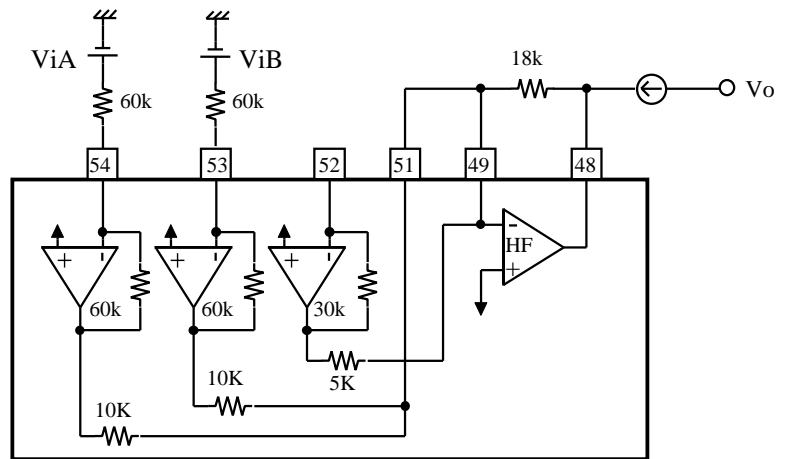


(4)-2V_{HHF},V_{LHF};

INPUT ViA(ViB)

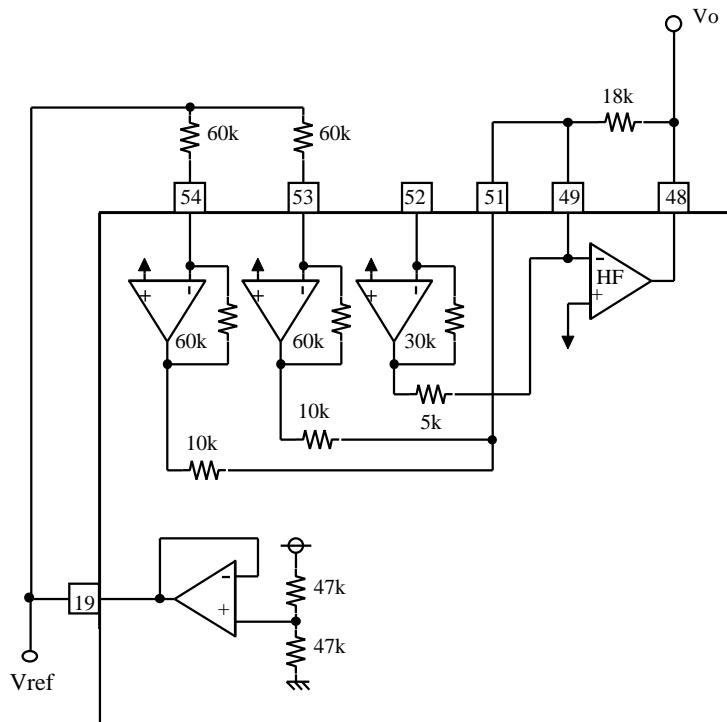
I_{OHHF}:Vo=4.0V

I_{OLHF}:Vo=1.0V



(5)V_{OSHF};

V_{REF}=1/2V_{CC}



PRELIMINARY
 Notice ; This is not a final specification.
 some parametric limits are subject to change.

M62481FP

PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

•MR BLOCK

(6)-1)RMN,RMJ,fMR (High,Low);

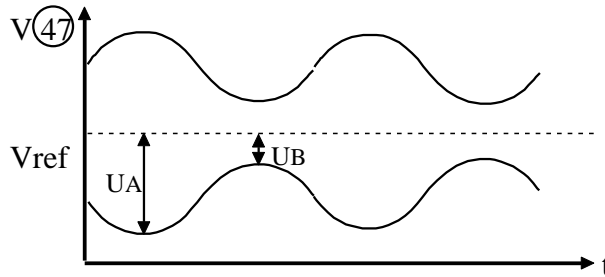
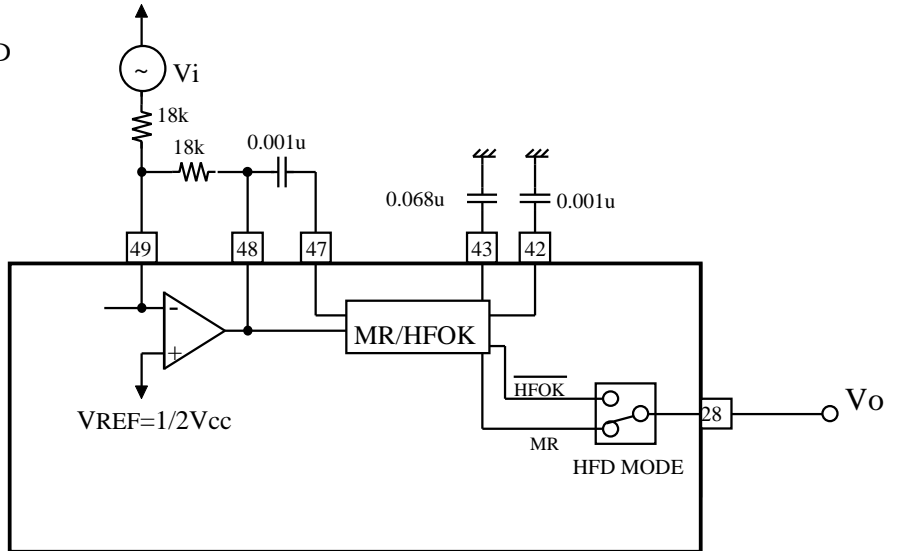
RMN : Mirror detector sensitivity : in normal mode
 (R0;D5(BRAKE)=0)

Test : UB is decrease starting at UB=UA.
 When MR pulses are detected at the HFD pin,RMN is calculated as follow:

$$RMN = \frac{UB}{UA}$$

RMJ : in brake mode
 (R0;D5(BRAKE)=1)

Test : same explanation as above



/BW WIDE=1; fc=500kHz AM fmod=1kHz
 /BW WIDE=0; fc=8.0MHz AM fmod=1kHz
 A= 0.5V

-2)fMR (High,Low);

fMR(Low) : cut off frequency of mirror detector. (R1;D13(BW WIDE)=1)

Test condition : • $\frac{UB}{UA} = 0.3 \rightarrow UB = 0.15V$

•(R0;D5(BRAKE)=0)

Test : fmod is increased. The HFO output is monitored.
 When the MR detector stops operation, the cut off frequency is found.

$$fMR(Low) = fmod$$

fMR(High) : cut off frequency of mirror detector.(R1;D13(BW WIDE)=0)
 (R0;D5(BRAKE)=0)

Test : same explanation as above

PRELIMINARY
 Notice ; This is not a final specification.
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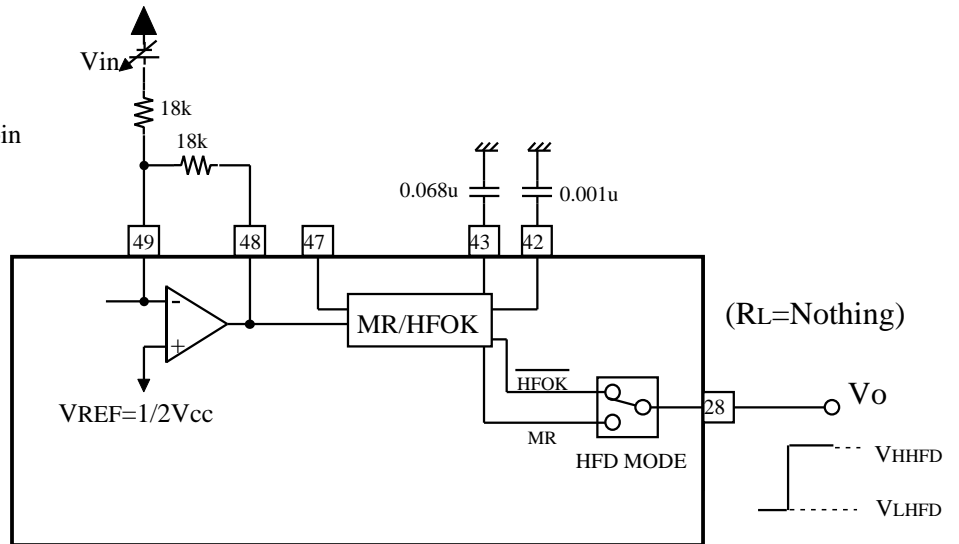
PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

(7) $V_{THHFOK}, V_{HHFD}, V_{LHFD}$;

V_{THHFOK} :

When input voltage V_{in} increase starting from V_{ref} ,

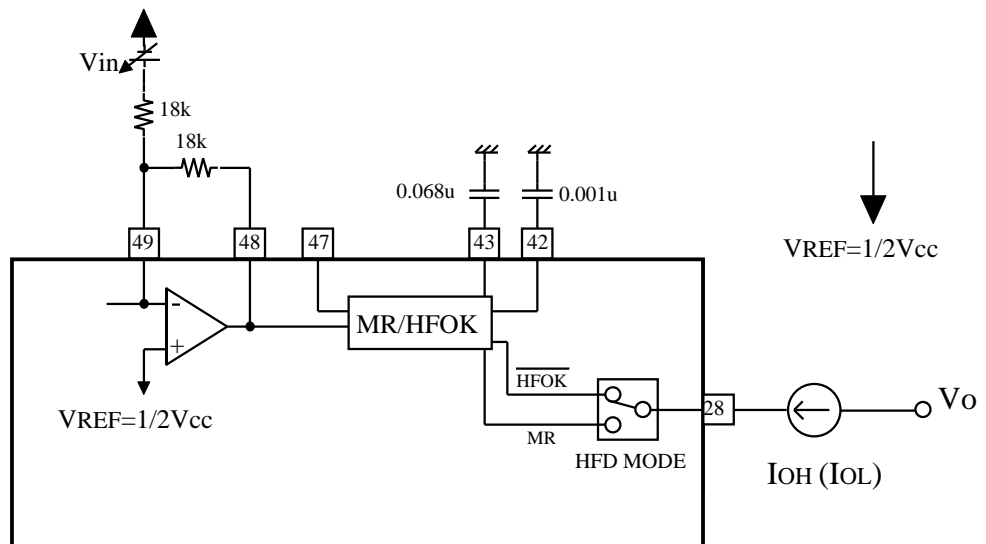
V_o change form "L" to "H" and pin 48 measure voltage(refer to V_{ref}).



(8) I_{OHHFD}, I_{OLHFD} ;

$V_o = 4.0V : I_{OHHFD}$

$V_o = 1.0V : I_{OLHFD}$



PRELIMINARY
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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

ELECTRICAL CHARACTERISTICS(2/6)

(Ta=25deg., Vcc=5V, f=1kHz, DCBA=1000, unless otherwise noted)

	Symbol	Block	Parameter	Test Conditions	Measurement circuit	Limit			Unit
						Min	Typ	Max	
22	GVFE	IV +	Gain	Gain value DCBA=1000(0dB)	(10)	12.0	14.0	16.0	dB
23	VHFE2		High output voltage	INPUT Vin= 4.0V	(11)	3.5	4.0	—	V
24	VLFE2		Low output voltage	INPUT Vin= 1.0V	(11)	—	1.0	1.5	V
25	IOHFE2		High output current	INPUT Vo= 4.0V	(12)	—	-2	-1	mA
26	IOLFE2		Low output current	INPUT Vo= 1.0V	(12)	1	2	—	mA
27	VOSFE2		Offset voltage	refer to VREF, (Focus gain : 0dB Focus balance : 0%)	(13-1)	-40	0	40	mV
28	VOSFE1		Offset voltage	refer to VREF, (Focus gain : 0dB Focus balance : 0%)	(13-1)	-15	0	15	mV
29	VOSFE1adj		Offset voltage	refer to VREF, (Focus gain : -11 -> 9.8dB Focus balance : 0%)	(13-2)	-15	0	15	mV
30	BALFE		Focus balance	R2;DCBA=1000(0%)	(10)	-2	0	+2	%
31	GVFS		FS	Gain		(14)	-2.0	0	2.0
32	VHFS	High output voltage		INPUT Vin= 1.0V	(15)	3.5	4.0	—	V
33	VLFS	Low output voltage		INPUT Vin= 4.5V	(15)	—	1.0	1.5	V
34	IOHFS	High output current		INPUT V0= 4.0V	(16)	—	-6.0	-4.0	mA
35	IOLFS	Low output current		INPUT V0= 1.0V	(16)	4.0	6.0	—	mA
36	VOSFS	Offset voltage		refer to VREF	(17)	-25	0	25	mV
37	VFSR ⊕	Focus Search	Focus search ⊕ voltage	refer to VREF (max)	(18)	1.45	1.67	—	V
38	VFSR ⊖		Focus search ⊖ voltage	refer to VREF (min)	(18)	—	-1.59	-1.40	V
39	VFZC1 ⊕	FZC	Focus zero cross1 ⊕ voltage (Shock detector)	"Shock or FZC" mode refer to VREF	(19-1)	0.07	0.12	0.17	V
40	VFZC1 ⊖		Focus zero cross1 ⊖ voltage (Shock detector)	"Shock or FZC" mode refer to VREF	(19-1)	-0.17	-0.12	-0.07	V
41	VFZC2 ⊕		Focus zero cross2 ⊕ voltage	refer to VREF	(19-2)	0.5	0.7	0.9	V
42	VFZC2 ⊖		Focus zero cross2 ⊖ voltage	refer to VREF	(19-2)	-0.9	-0.7	-0.5	V
43	AFG1§2ON	FG	Attenuation FG1,2 ON	"FG1 SW=FG2 SW=ON", RL=2kohm	(20)	15	20	—	dB
44	AFG1§2OFF		Attenuation FG1,2 OFF	"FG1 SW=FG2 SW=OFF"	(20)	0	—	2	dB

PRELIMINARY
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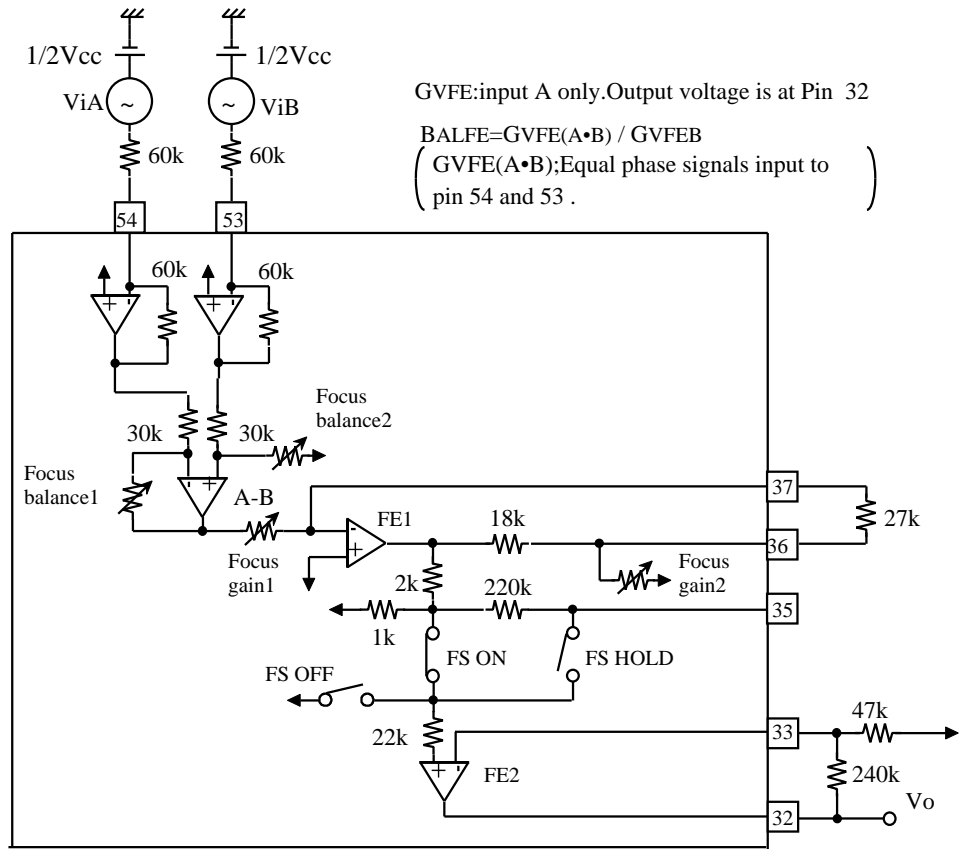
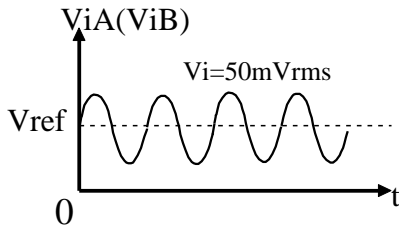
PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

note(2/6)

•IV + FE BLOCK

(10)GVFE,BALFE;

INPUT ViA(ViB)



GVFE:input A only.Output voltage is at Pin 32

$$BALFE = \frac{GVFE(A \cdot B)}{GVFE(B)}$$

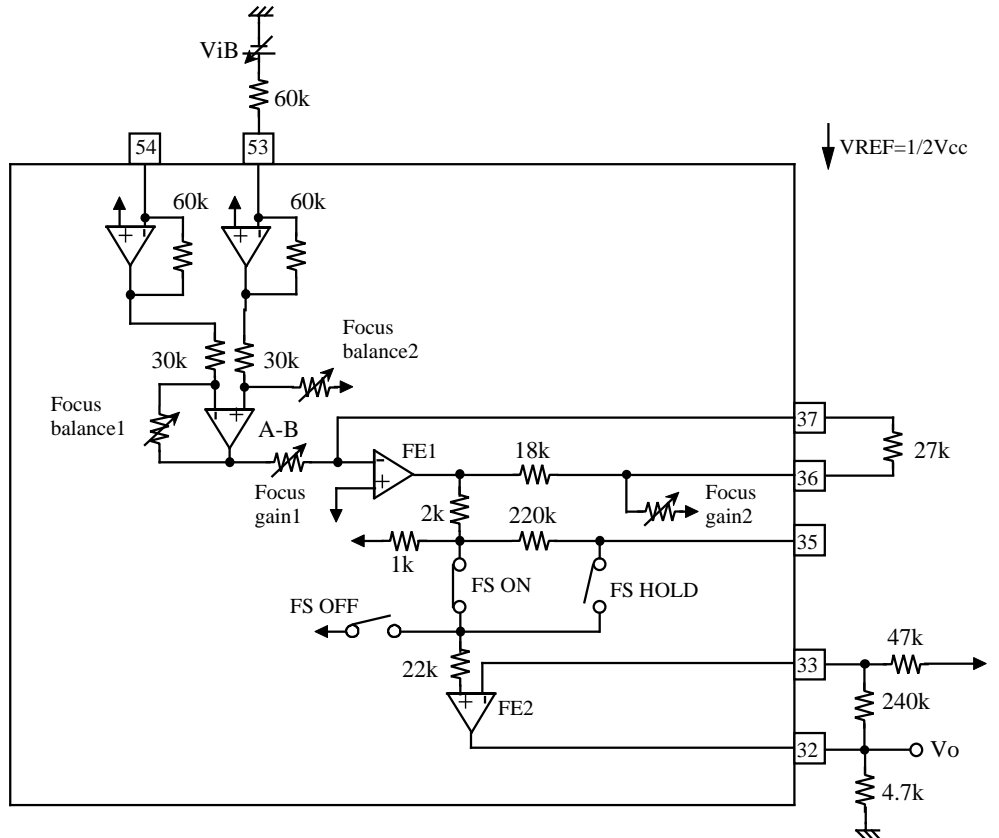
(GVFE(A·B);Equal phase signals input to pin 54 and 53 .)

(11)VHFE2,VLFE2;

INPUT ViA(ViB)

VHFE2:Vi=4.0V

VLFE2:Vi=1.0V



PRELIMINARY
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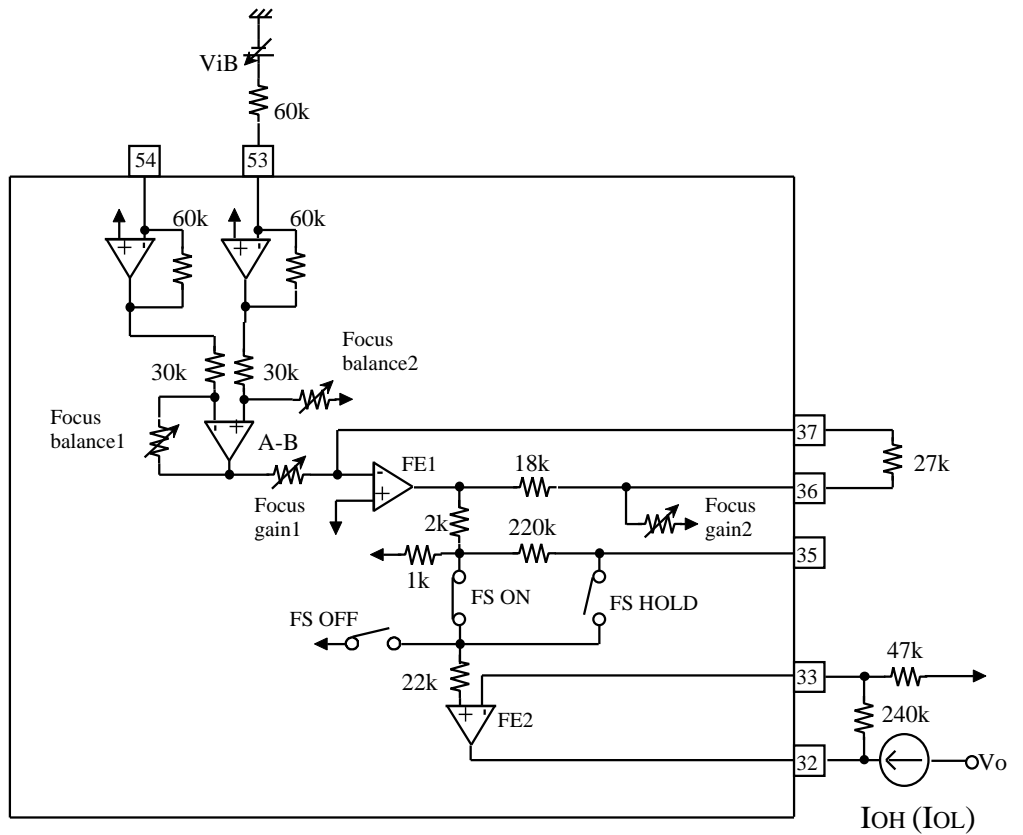
PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

(12) IOHFE2, IOLFE2;

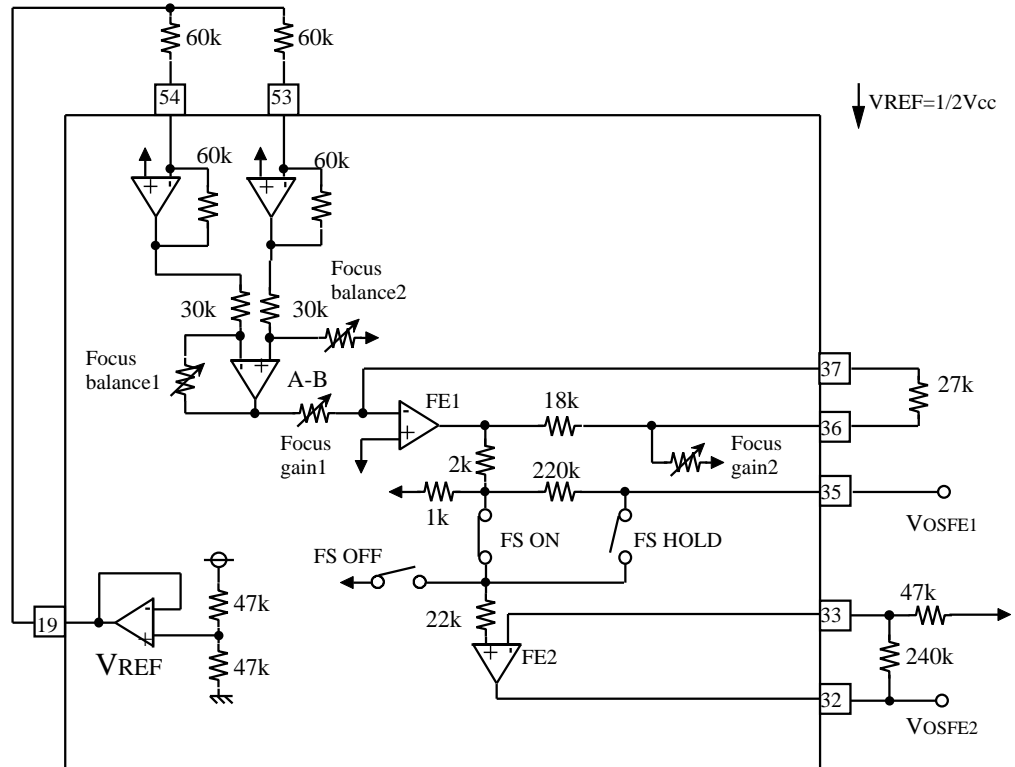
INPUT ViA(ViB)

IOHFE2: Vo=4.0V

IOLFE2: Vo=1.0V



(13)-1VosFE1, VosFE2



PRELIMINARY
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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

(13)-2 VOSFE1adj

- ① . Focus gain (R3;D0->3=1 (9.8dB) Measurement circuit (13)-1

VOSFE1: within +/- 50mV



- ② . Focus gain (R3;D0->3=1 (9.8dB) Measurement circuit (13)-2

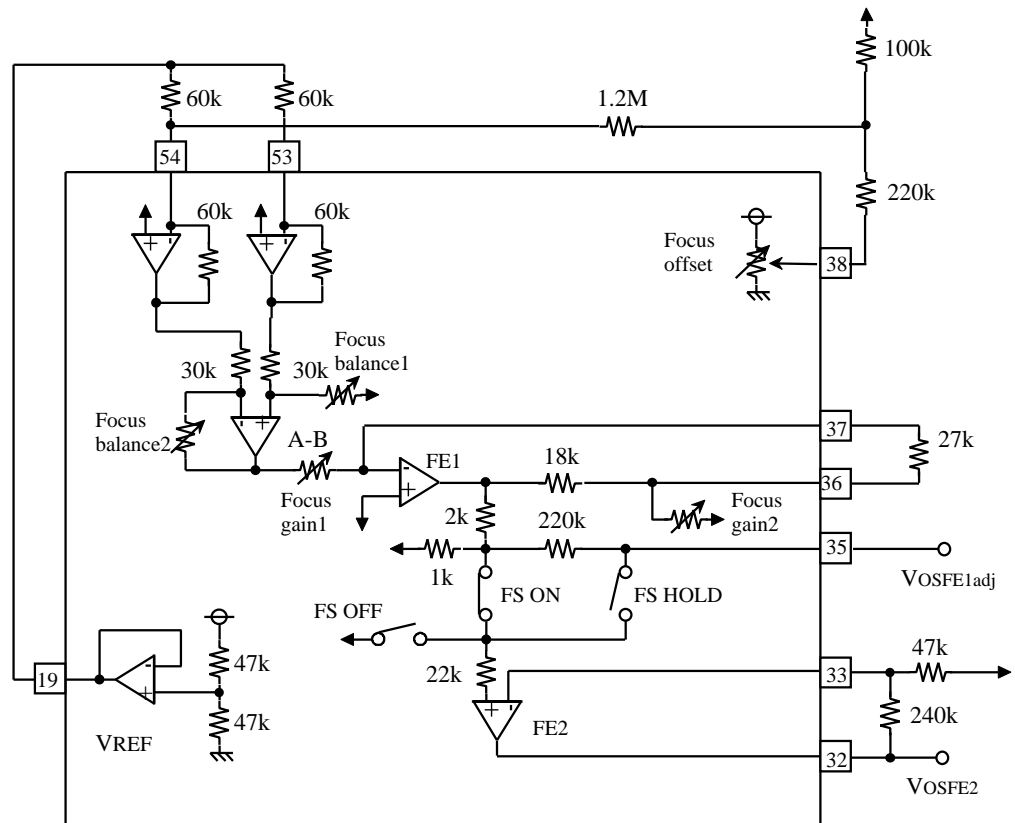
Input pin54 add Va(Offet voltage)

VOSFE1adj is within +/- 15mV by adjusting Va.



- ③ . Focus gain (-11->9.8dB) Measurement circuit (13)-2

VOSFE1adj(pin35) : mesurement



↓ VREF=1/2Vcc

PRELIMINARY
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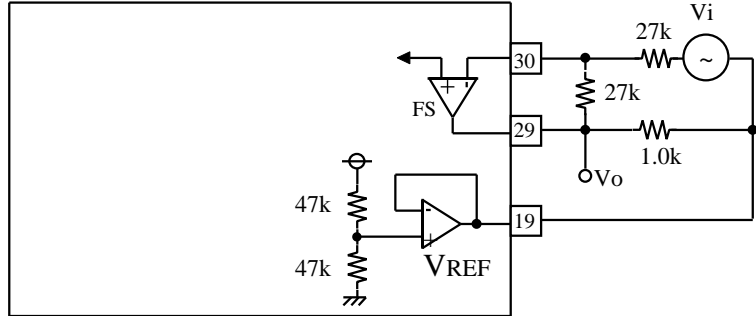
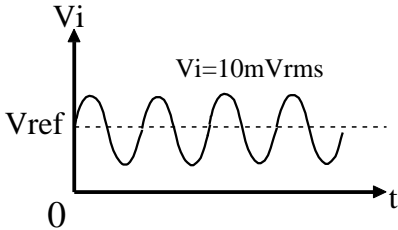
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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

•FS BLOCK

(14)GVFS:input pin 30 ;

$G_{VFS} = V_o / V_i$

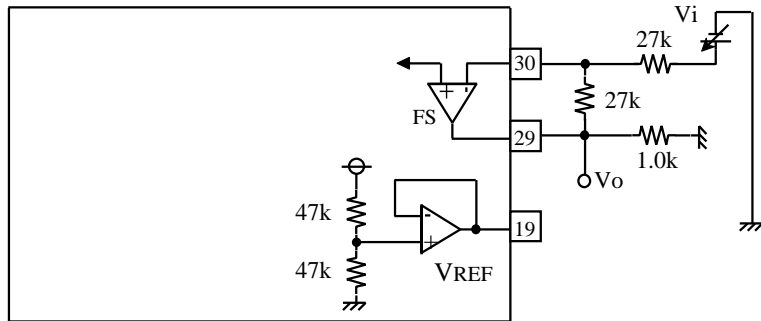


(15) V_{HFS}, V_{LFS} ;

INPUT V_i

$V_{HFS}: V_i = 1.0V$

$V_{LFS}: V_i = 4.0V$

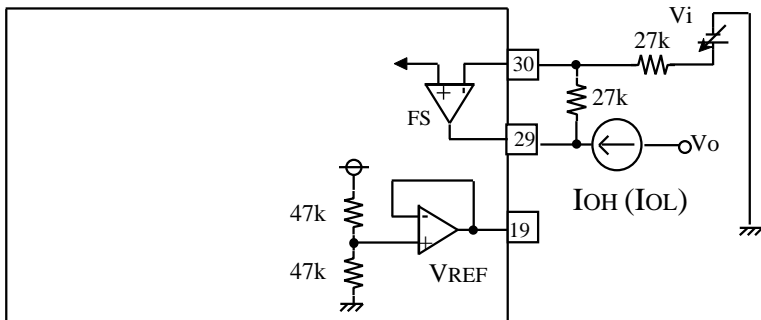


(16) I_{OHFS}, V_{ILFS} ;

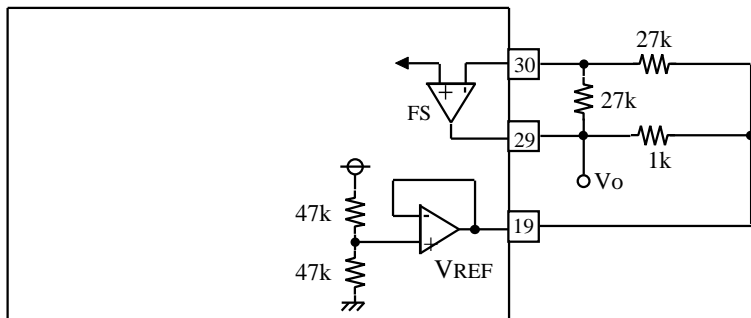
INPUT V_i

$I_{OHFS}: V_o = 4.0V$

$I_{OLFS}: V_o = 1.0V$



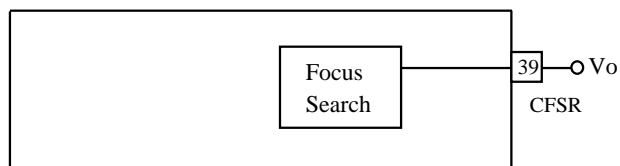
(17) V_{OSFS} ;



(18) $V_{FSR}^{\oplus}, V_{FSR}^{\ominus}$;

$V_{FSR}^{\oplus} (R1:D8=0, D9 \rightarrow D12=1)$

$V_{FSR}^{\ominus} (R1:D8=1, D9 \rightarrow D12=1)$

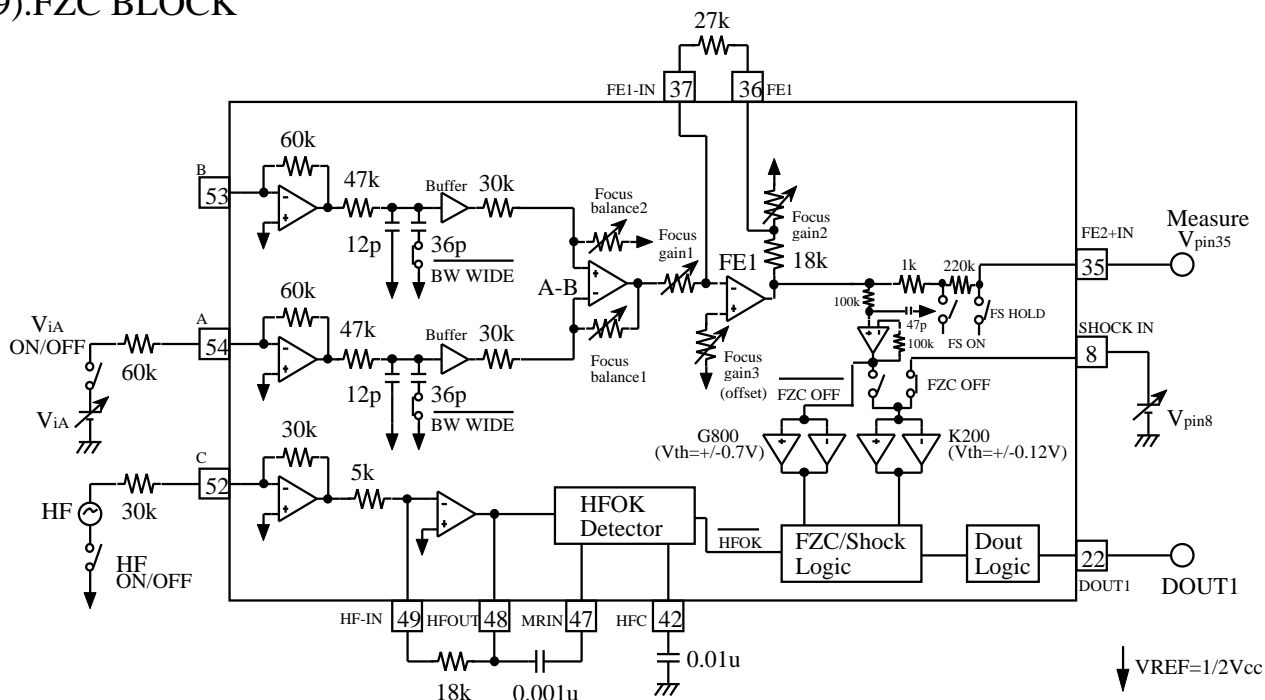


$\downarrow V_{REF} = 1/2V_{cc}$

PRELIMINARY
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(19).FZC BLOCK



(19)-1. $V_{FZC1\oplus}, V_{FZC1\ominus}$ (K200);

1. Set R0,D7 (FZC OFF)=1.
2. Set pin 24 (JP1/SG) to "H".
3. Apply HF signal to pin 52 (C input).
4. R0,D11=R0,D10 (Dout Mode)=0.
5. Apply Vref to pin 8 (Shock in).
6. Increase voltage at pin 8 and monitor the DOUT1 pin.
7. When the voltage at the DOUT1 pin changes, the threshold is found.
8. Threshold voltage can be calculated as follows;

$$V_{FZC1\oplus} = V_{pin8} - V_{ref}$$

9. Apply Vref to pin 8 (Shock in).
10. Decrease voltage at pin 8 and monitor the DOUT1 pin.
11. When the voltage at the DOUT1 pin changes, the threshold is found.
12. Threshold voltage can be calculated as follows;

$$V_{FZC1\ominus} = V_{pin8} - V_{ref}$$

PRELIMINARY
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(19)-2. V_{FZC2+}, V_{FZC2-} (G800);

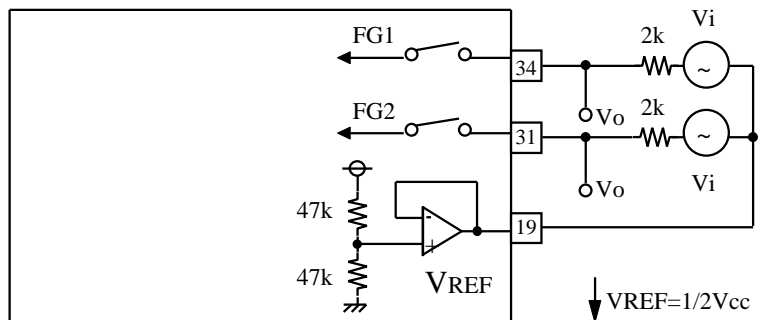
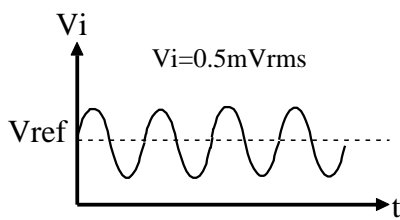
1. Set R0,D7 (FZC OFF)=1.
2. Apply a voltage to pin8 (shock in) which is much above the comparators threshold.
3. Set pin 24 (JP1/SG) to "H"
4. R0,D11=R0,D10 (Dout Mode)=0.

5. Apply Vref and no HF signal to pin 52 (C input).
6. Apply HF signal to pin 52 (C input).
7. Adjust ViA to Vref (=input to pin 53 (A input) via 60kohm resistor).
8. Increase voltage at pin 53 and monitor the DOUT1 pin.
9. When the voltage at the DOUT1 pin changes, the threshold is found.
10. Threshold voltage can be monitored at pin35 (FE2+IN) and calculated as follows;
 $V_{FZC2+} = V_{pin34} - V_{ref}$

11. Apply Vref and no HF signal to pin 52 (C input).
12. Apply HF signal to pin 52 (C input).
13. Adjust ViA to Vref (=input to pin 54 (A input) via 60kohm resistor).
14. Decrease voltage at pin 54 and monitor the DOUT1 pin.
15. When the voltage at the DOUT1 pin changes, the threshold is found.
16. Threshold voltage can be monitored at pin35 (FE2+IN) and calculated as follows;
 $V_{FZC2-} = V_{pin35} - V_{ref}$

(20) AFG1,2ON, AFG1,2OFF;

AFG ON (R0;D8=0,R3;D8=1,R3;D9=0)
 AFG OFF(R0;D8=0,R3;D8=0,R3;D9=0)



PRELIMINARY
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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

ELECTRICAL CHARACTERISTICS(3/6)

(Ta=25deg,Vcc=5V,f=1kHz,DCBA=1000,unless otherwise noted)

	Symbol	Block	Parameter	Test Conditions	Measurement circuit	Limit			Unit
						Min	Typ	Max	
45	GVTE	IV + TE	Gain	gain value : DCBA=1000(0dB)	(21)	12.0	14.0	16.0	dB
46	VHTE2		High output voltage	INPUT Vin= 4.0V	(22)	3.5	4.0	—	V
47	VLTE2		Low output voltage	INPUT Vin= 1.0V	(22)	—	1.0	1.5	V
48	IOHTE2		High output current	INPUT Vo= 4.0V	(23)	—	-2.0	-1.0	mA
49	IOLTE2		Low output current	INPUT Vo= 1.0V	(23)	1.0	2.0	—	mA
50	VOSTE2		Offset voltage	refer to VREF (Track gain : 0dB Track balance : 0%)	(24)-1	-40	0	+40	mV
51	VOSTE1		Offset voltage	refer to VREF (Track gain : 0dB Track balance : 0%)	(24)-1	-15	0	+15	mV
52	VOSTE1adj		Offset voltage	refer to VREF (Track gain : -11 -> 9.8dB Track balance : 0%)	(24)-2	-15	0	+15	mV
53	BALTE		Track balance		(21)	-3.0	0	+3.0	%
54	GVTS		TS	Gain		(25)	-2.0	0	2.0
55	VHTS	High output voltage		INPUT Vin= 1.0V	(26)	3.5	4.0	—	V
56	VLTS	Low output voltage		INPUT Vin= 4.5V	(26)	—	1.0	1.5	V
57	IOHTS	High output current		INPUT Vo= 4.0V	(27)	—	-6.0	-4.0	mA
58	IOLTS	Low output current		INPUT Vo= 1.0V	(27)	4.0	6.0	—	mA
59	VOSTS	Offset voltage		refer to VREF	(28)	-25	0	25	mV
60	VJF	Jump voltage(forward)		"JF"Mode, refer to VREF	(28)	+0.12	+0.15	+0.18	V
61	VJR	Jump voltage(reverse)		"JR"Mode, refer to VREF	(28)	-0.18	-0.15	-0.12	V
62	VTC⊕	TC	Track cross ⊕ voltage	refer to VREF	(29)	+50.0	+62.5	+75.0	mV
63	VTC⊖		Track cross ⊖ voltage	refer to VREF	(29)	-75.0	-62.5	-50.0	mV

PRELIMINARY
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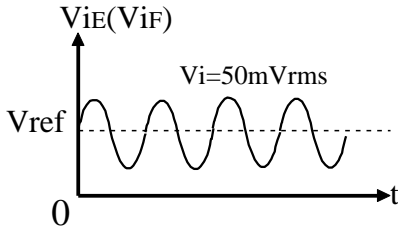
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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

note(3/6)

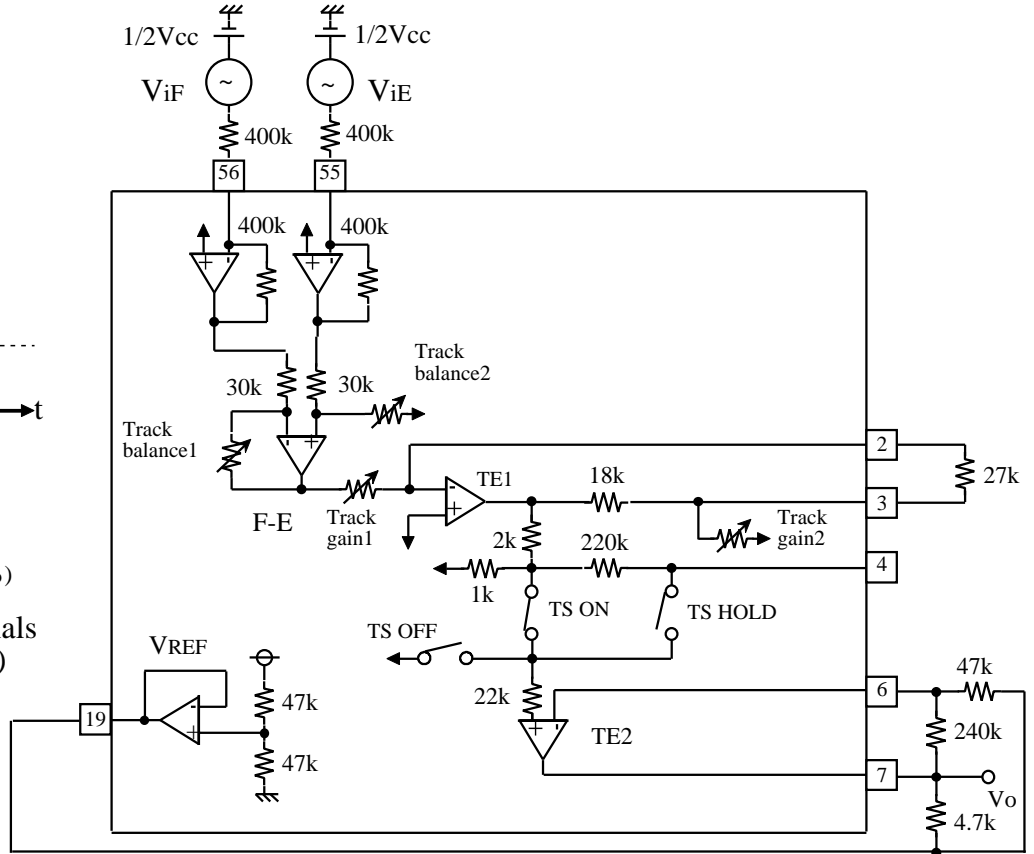
•IV+TE BLOCK

(21)GVTE,BALTE;



$$BALTE = GVTE(E \cdot F) / GVTE (\%)$$

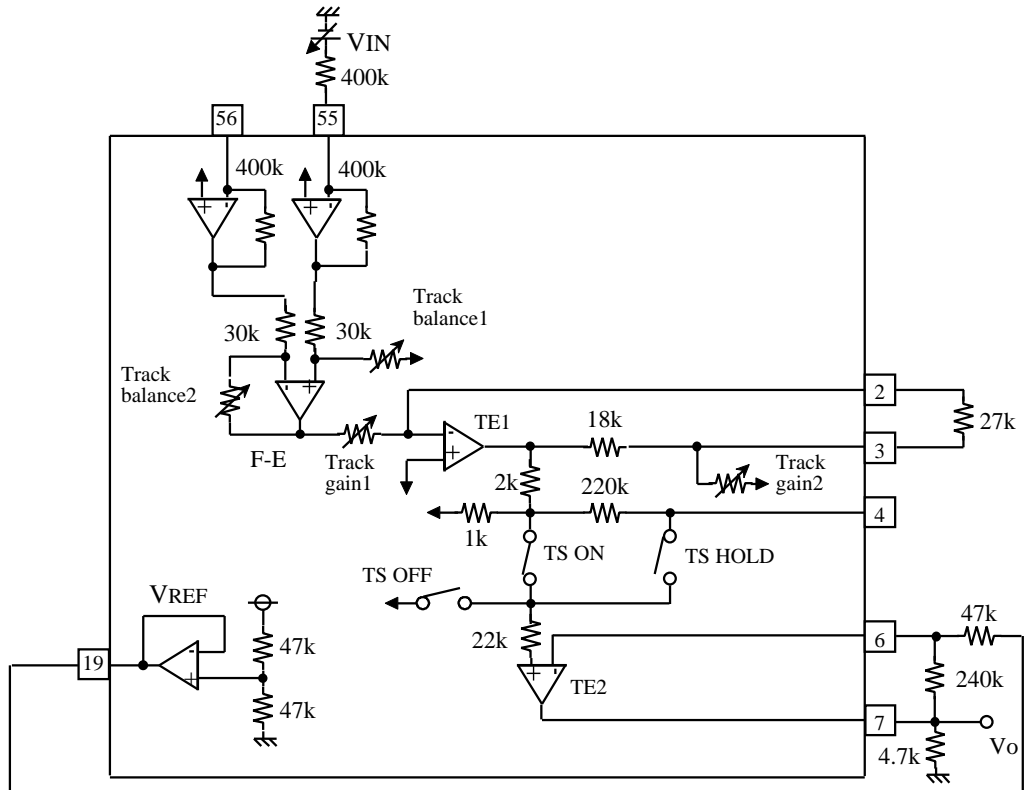
(GVTE(E·F) : Equal Phase signals
 input to pin 56 and 55)



(21)VHTE2,VLTE2;

INPUT VIN
 VHTE2 : VIN=4.0V
 VLTE2 : VIN=1.0V

↓ VREF=1/2Vcc



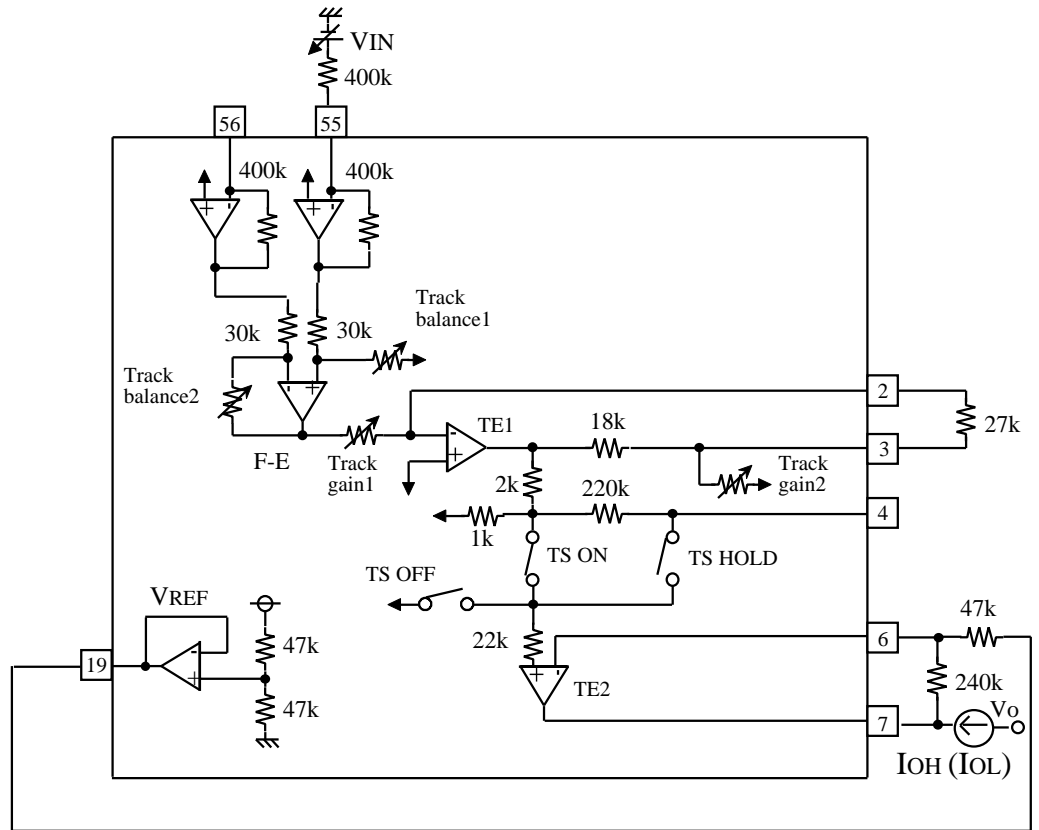
PRELIMINARY
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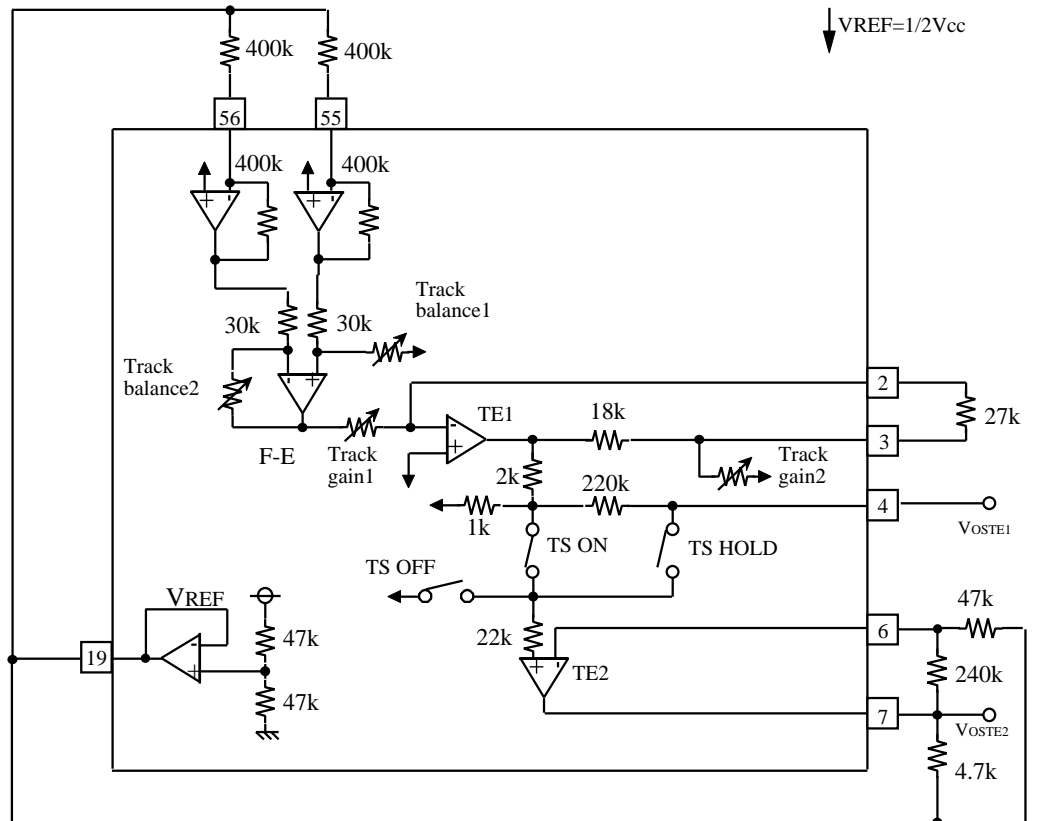
PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

(23)IOHTE2,IOLTE2;

INPUT V_{IN}
 $I_{OHTE2} : V_O=4.0V$
 $I_{OLTE2} : V_O=1.0V$



(24)-1VOSTE2,VOSTE1;



PRELIMINARY
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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

(24)-2 VOSTE1adj

- ① . Track gain (R3;D4->7=1 (9.8dB) Measurement circuit (24)-1

VOSTE1: within +/- 50mV



- ② . Track gain (R3;D4->7=1 (9.8dB) Measurement circuit (24)-2

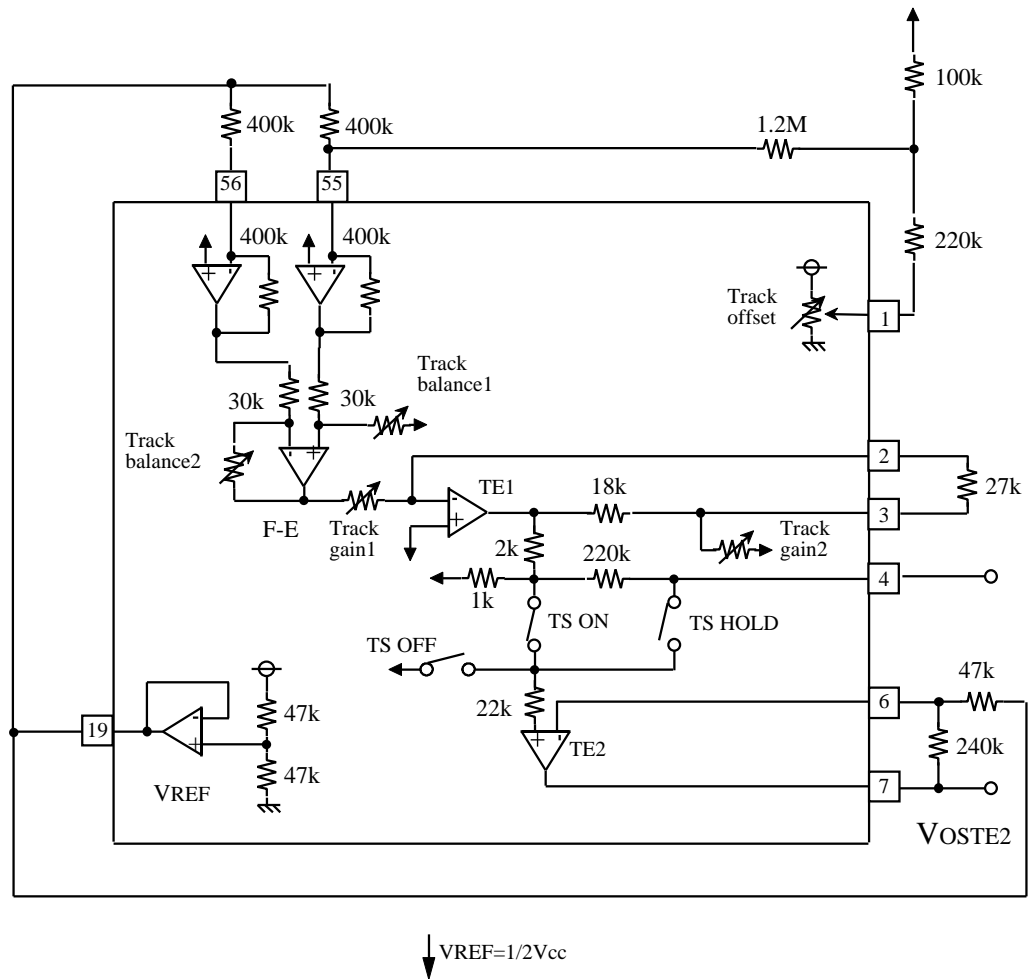
Input pin55 add Va(Offet voltage)

VOSTE1adj is within +/- 15mV by adjusting Va.



- ③ . Track gain (-11->9.8dB) Measurement circuit (24)-2

VOSTE1adj(pin4) : mesurement

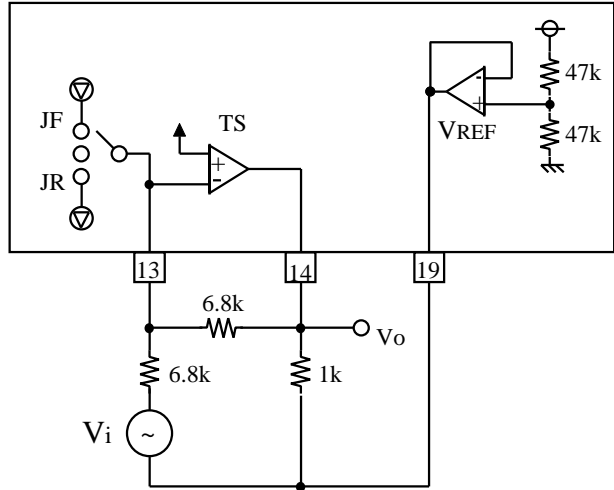
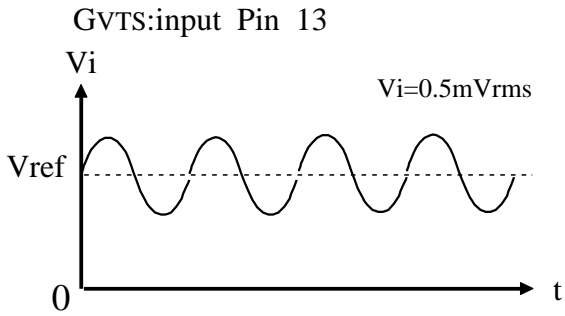


PRELIMINARY
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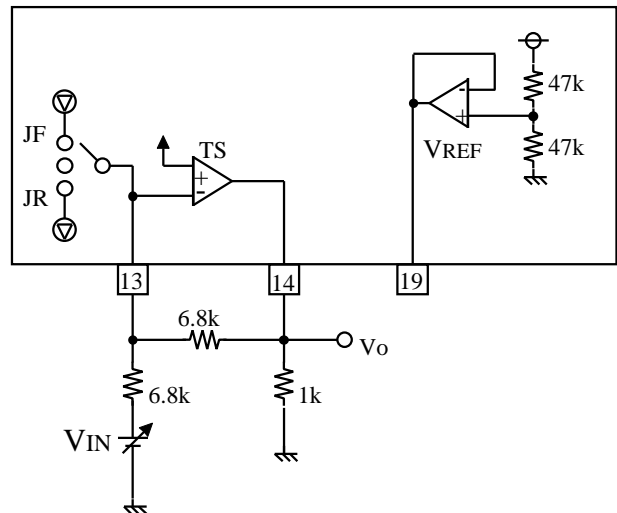
• TS BLOCK

(25)GVTS;



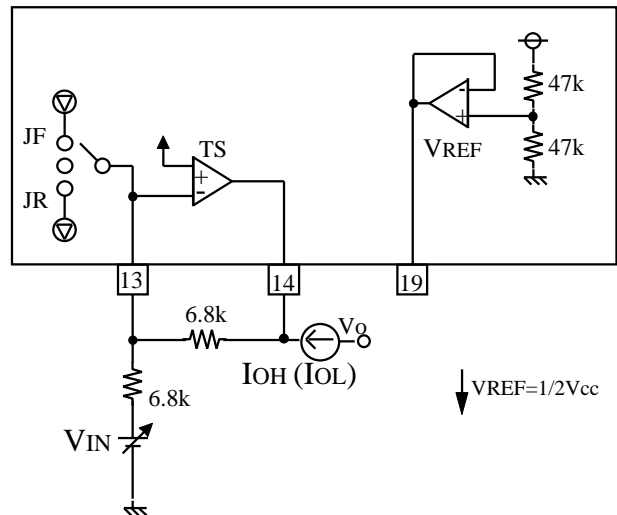
(26)VHTS,VLTS;

INPUT V_{IN}
 VHTS : $V_{IN}=1.0V$
 VLTS : $V_{IN}=4.0V$



(27)IOHTS,IOLTS;

INPUT V_{IN}
 IOHTS : $V_O=4.0V$
 IOLTS : $V_O=1.0V$



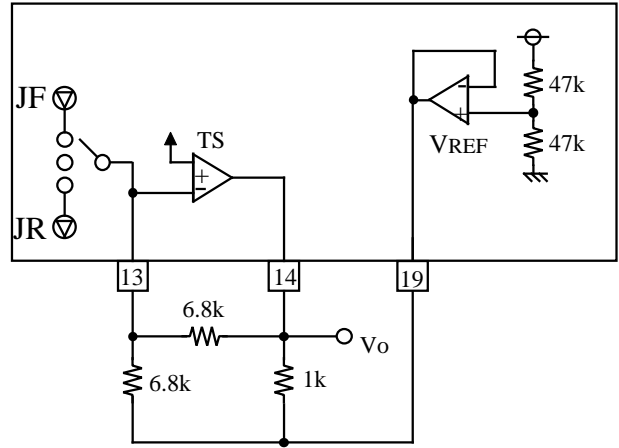
PRELIMINARY
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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

(28) V_{OSTS}, V_{JF}, V_{JR} ;

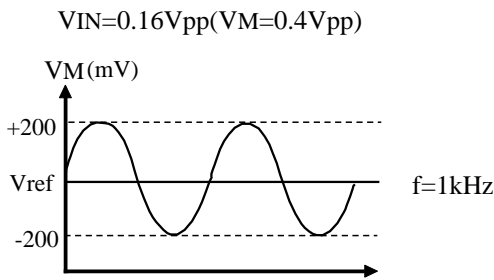
V_{JF} (JP1/SG="X" R0 ; D13=D3=0, D4=1)
 V_{JR} (JP1/SG="X" R0 ; D13=D3=1, D4=0)



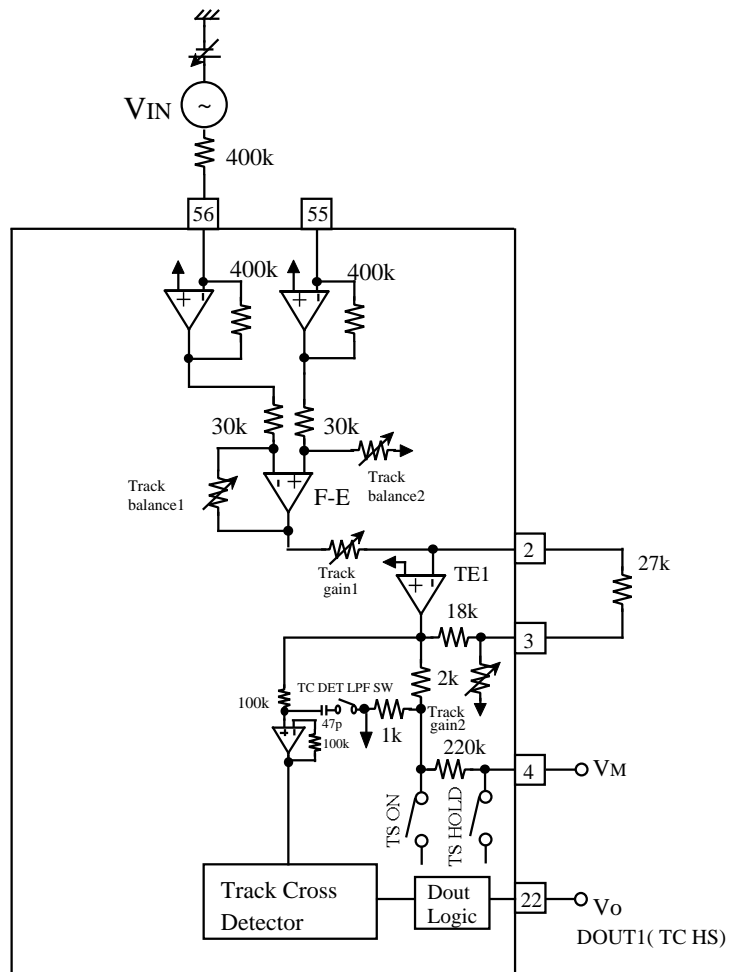
(29) V_{TC+}, V_{TC-} ;

R0 ; D7=0, D11=D10=1

INPUT V_{IN}
 OUTPUT D_{out1}



Test : When D_{out1} is detected "H" and "L"
 , the voltage of pin 4 measure.



$V_{REF} = 1/2 V_{CC}$

PRELIMINARY
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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

ELECTRICAL CHARACTERISTICS(4/6)

(Ta=25deg., Vcc=5V, f=1kHz, DCBA=1000, unless otherwise noted)

	Symbol	Block	Parameter	Test Conditions	Measurement circuit	Limit			Unit
						Min	Typ	Max	
64	ATG1,2ON	TG	Attenuation TG1,2 ON	TG1 SW=TG 2 SW="ON" RL=2kohm	(30)	15	20	—	dB
65	ATG1,2OFF		Attenuation TG1,2 OFF	TG1 SW=TG2 SW="OFF"	(30)	0	—	2	dB
66	ATG3ON		Attenuation TG3 ON	TG3 SW="ON" RL=2kohm	(30)	15	20	—	dB
67	ATG2OFF		Attenuation TG3 OFF	TG3 SW="OFF"	(30)	0	—	2	dB
68	GVSS	SS	Gain		(31)	10	12	14	dB
69	ATTSS		Attenuation at SS OFF		(31)	40	—	—	dB
70	VHSS		High output voltage	INPUT Vin= 4.0V	(32)	3.5	4.0	—	V
71	VLSS		Low output voltage	INPUT Vin= 1.0V	(32)	—	1.0	1.5	V
72	IOHSS		High output current	INPUT Vo= 4.0V	(33)	—	-6.0	-4.0	mA
73	IOLSS		Low output current	INPUT Vo= 1.0V	(33)	4.0	6.0	—	mA
74	VOSSon		Offset voltage SS on	"SS on"Mode, refer to VREF	(34)	-35	0	35	mV
75	VOSSoff		Offset voltage SS off	"SS off"Mode, refer to VREF	(34)	-25	0	25	mV
76	VSF		Slide voltage(forward)	"SF"Mode, refer to VREF	(34)	+0.76	+0.95	+1.14	V
77	VSR		Slide voltage(reverse)	"SR"Mode, refer to VREF	(34)	-1.14	-0.95	-0.76	V
78	VRST	RESET	Reset voltage			2.1	2.3	2.5	V
79	GVAP	APC	Gain	Input Vi= 170 mV	(35)	51	54	57	dB
80	ATTAP		APC OFF voltage		(36)	4.0	4.8	—	v
81	VHAP		High output voltage	Input Vi= 240 mV	(36)	3.5	4.0	—	V
82	VLAP		Low output voltage	Input Vi= 100 mV	(36)	—	1.0	1.5	V
83	IOHAP		High output current	INPUT Vo= 4.0V	(37)	—	-1.0	-0.2	mA
84	IOLAP		Low output current	INPUT Vo= 1.0V	(37)	0.2	1.0	—	mA

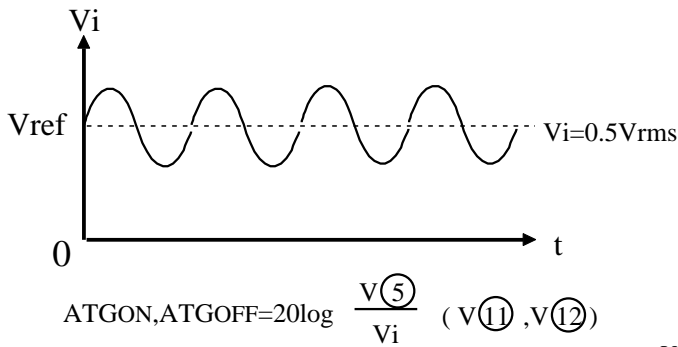
PRELIMINARY
 Notice ; This is not a final specification.
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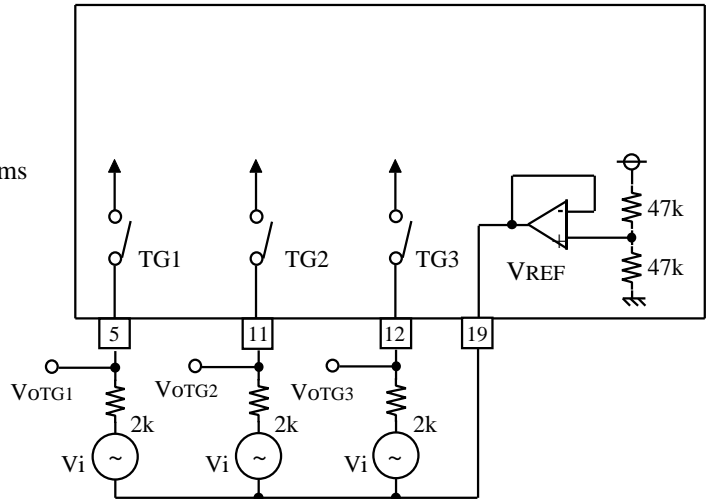
note(4/6)

•TG BLOCK

- (30)ATG ON , ATG OFF;
- ATG1,2 ON (R0;D8=1,R3;D8=1,R3;D9=0)
- OFF (R0;D8=1,R3;D8=0,R3;D9=0)
- ATG3 ON (R3;D10=1)
- OFF (R3;D10=0)

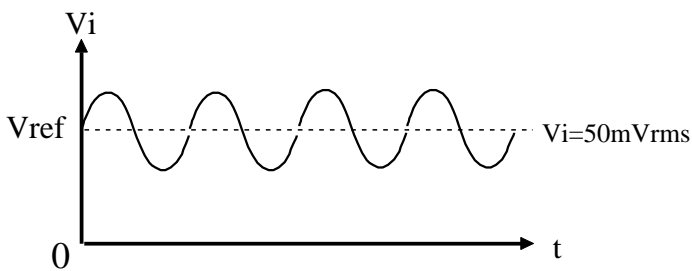


$$ATGON, ATGOFF = 20 \log \frac{V(5)}{V_i} \quad (V(11), V(12))$$

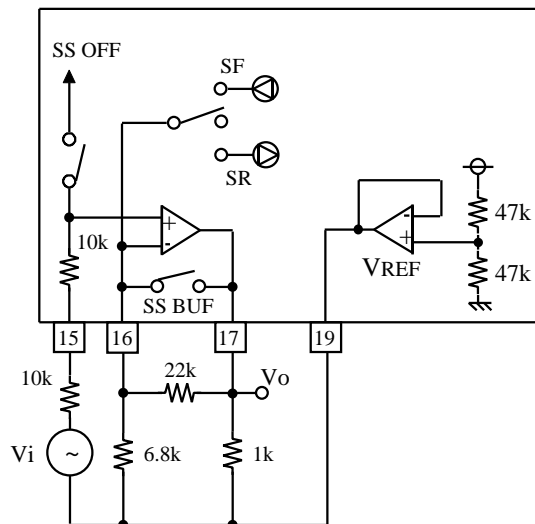


•SS BLOCK

- (31)Gvss, ATTSS; (R1=D0=D1=1)
- INPUT V_i (Pin 15)



$$ATTSS = \frac{G_{vss}(SS \text{ OFF} = \text{OFF})}{G_{vss}(SS \text{ OFF} = \text{ON})}$$



↓ $V_{REF} = 1/2 V_{CC}$

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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

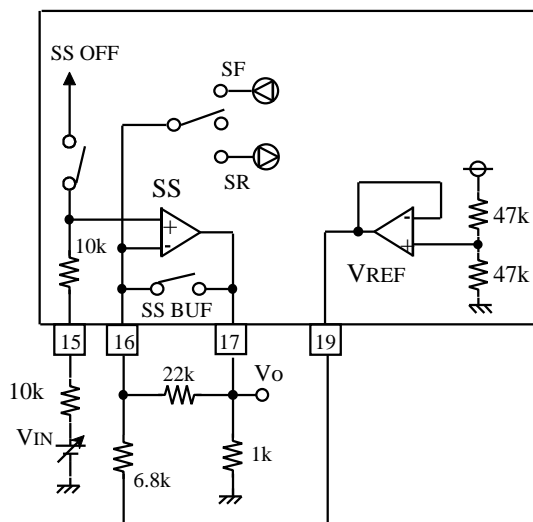
(32) V_{HSS}, V_{LSS} ;

($R1=D0=D1=1$)

INPUT V_{IN}

$V_{HSS} : V_{IN}=4.0V$

$V_{LSS} : V_{IN}=1.0V$



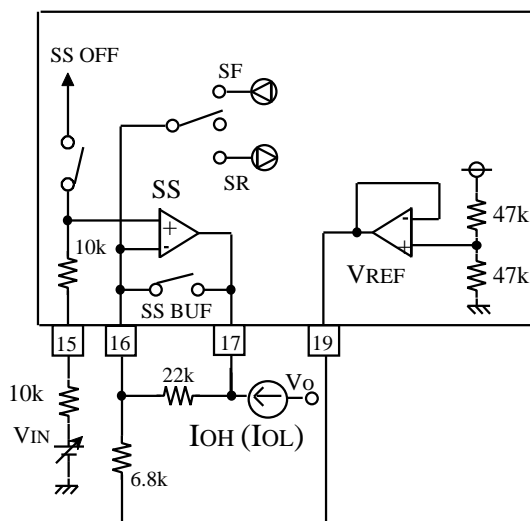
(33) I_{OHSS}, I_{OLSS} ;

($R1=D0=D1=1$)

INPUT V_{IN}

$I_{OHSS} : V_O=4.0V$

$I_{OLSS} : V_O=1.0V$



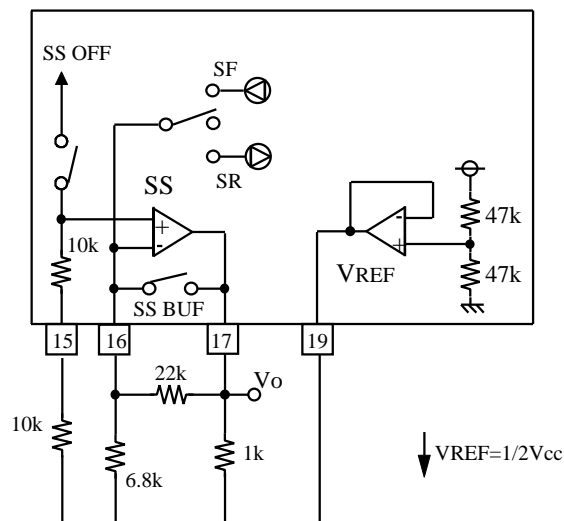
(34) V_{OSSS}, V_{SF}, V_{SR} ;

V_{OSSS1} (JP1/SG=L,R0;D0=0,D1=0,D2=1)

V_{OSSS2} (JP1/SG=L,R0;D0=1,D1=1,D2=0)

V_{SF} (JP1/SG=H,R0;D1=1,D0=0)

V_{SR} (JP1/SG=H,R0;D1=0,D0=1)

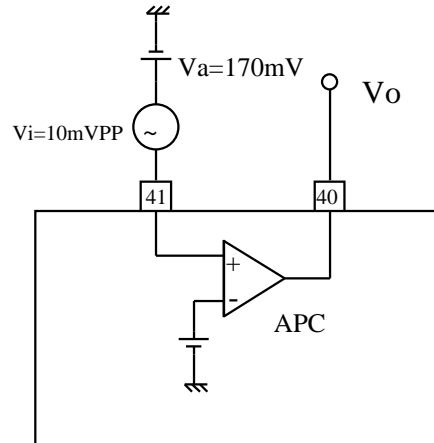
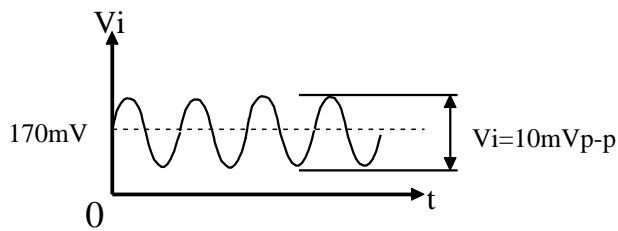


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(35)G_{VAP};

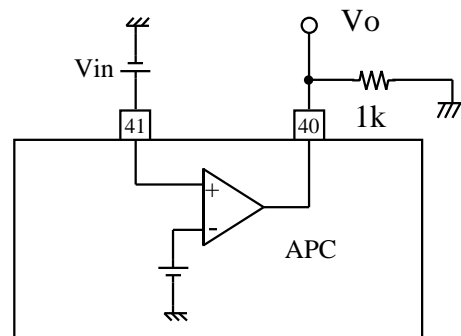
Input signal V_i



(36)ATT_{AP},V_{HAP},V_{LAP};

APC OFF (R1;D4=0) , APC ON (R1;D4=1)

Input V_{in}

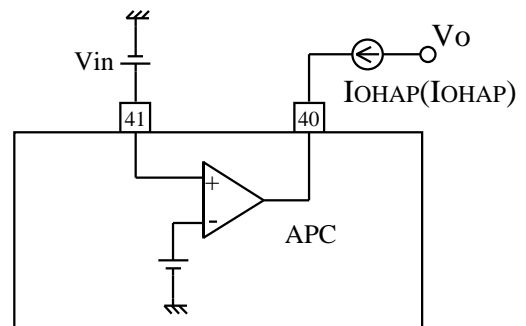


(37)I_{OHAP},I_{OLAP};

APC ON (R1;D4=1)

I_{OHAP}:V_o=4.0V

I_{OHAP}:V_o=1.0V



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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

ELECTRICAL CHARACTERISTICS(5/6)

(Ta=25deg., Vcc=5V, f=1kHz, DCBA=1000, unless otherwise noted)

	Symbol	Block	Parameter	Test Conditions	Measurement circuit	Limit			Unit
						Min	Typ	Max	
85	GVFE(max)	ADJ	max gain(FE)	"Focus gain"Mode DCBA=1111	(10)	+20.0	+23.0	+26.0	dB
86	GVFE(min)		min gain(FE)	"Focus gain"Mode DCBA=0000	(10)	0.0	+3.0	+6.0	dB
87	GVTE(max)		max gain(TE)	"Track gain"Mode DCBA=1111	(21)	+20.0	+23.0	+26.0	dB
88	GVTE(min)		min gain(TE)	"Track gain"Mode DCBA=0000	(21)	0.0	+3.0	+6.0	dB
89	BALFE(max)		max balance(FE)	"Focus balance"Mode DCBA=1111	(10)	+23.4	+26.4	+29.4	%
90	BALFE(min)		min balance(FE)	"Focus balance"Mode DCBA=0000	(10)	-34.8	-31.8	-28.8	%
91	BALTE(max)		max balance(TE)	"Track balance"Mode DCBA=1111	(21)	+23.4	+26.4	+29.4	%
92	BALTE(min)		min balance(TE)	"Track balance"Mode DCBA=0000	(21)	-34.8	-31.8	-28.8	%
93	VPhFE +		Phase error + voltage	"Focus gain" Mode Phase error(90+30)deg.	(42)	3.1	3.3	3.5	V
94	VPhFE -		Phase error - voltage	"Focus gain" Mode Phase error(90-30)deg.	(42)	1.5	1.7	1.9	V
95	VPhTE +		Phase error + voltage	"Track gain" Mode Phase error(90+30)deg.	(43)	3.1	3.3	3.5	V
96	VPhTE -		Phase error - voltage	"Track gain" Mode Phase error(90-30)deg.	(43)	1.5	1.7	1.9	V
97-1	VBAL		Focus Balance output Voltage	Vin=2.0p-p, Refer to VREF	(44-1)	0.4	0.7	—	V _{p0}
97-2	V _{thFBAL+}	FBAL Ajustment comparetor Threshold+	"Focus balance"Mode , Refer to VREF	(44-2)	5	15	25	mV	
97-3	V _{thFBAL-}	FBAL Ajustment comparetor Threshold-	"Focus balance"Mode , Refer to VREF	(44-2)	-25	-15	-5	mV	
98	VBALT +	Balance error + voltage (TE)	"Track balance"Mode ,Ein=Vref-0.2V	(45)	2.8	3.0	3.2	V	
99	VBALT -	Balance error - voltage (TE)	"Track balance"Mode ,Ein=Vref+0.2V	(45)	1.8	2.0	2.2	V	
100	fHADJ	Cut off frequency	C(Pin 18)=2200pF	(46)	0.7	1.0	1.3	kHz	

PRELIMINARY
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note(5/6)

(38)GVFE(max),GVFE(min): refer to GVFE measurement (show to (10))

GVFE(max) ; R3 ; D0->D3=1

GVFE(min) ; R3 ; D0->D3=0

(39)GVTE(max),GVTE(min): refer to GVTE measurement (show to (21))

GVTE(max) ; R3 ; D4->D7=1

GVTE(min) ; R3 ; D4->D7=0

(40)BALFE(max),BALFE(min): refer to BALFE2 measurement (show to (10))

BALFE(max) ; R2 ; D0->D3=1

BALFE(min) ; R2 ; D0->D3=0

(41)BALTE(max),BALTE(min): refer to BALTE2 measurement (show to (21))

BALTE(max) ; R2 ; D4->D7=1

BALTE(min) ; R2 ; D4->D7=0

(42) V_{PhFE+} , V_{PhFE-} ;

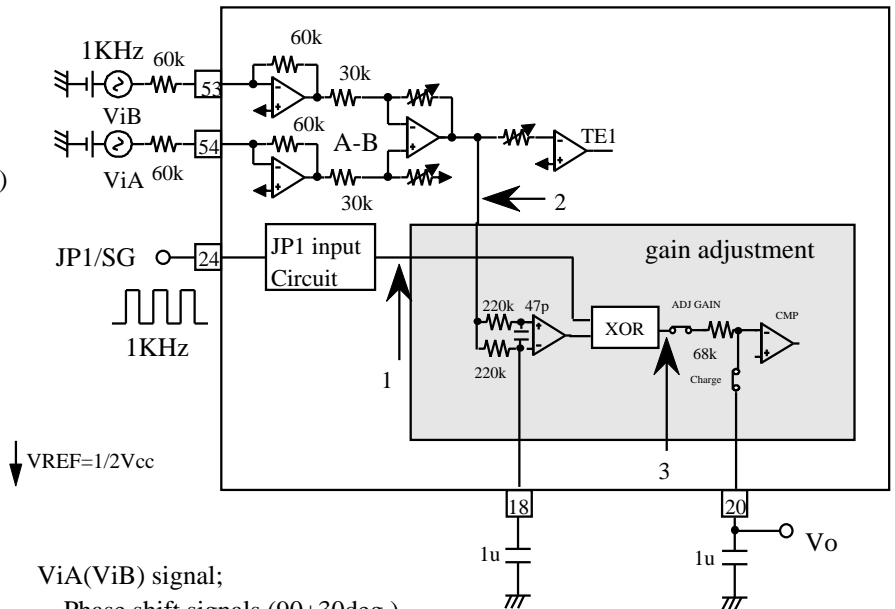
Focus gain adjustment mode (show to (78/88))

(R3;D3=1,D0->D2=0)

ViA(ViB) signal;

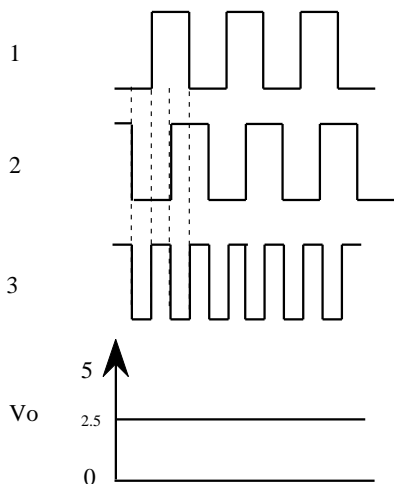
Phase shift signals (90+/-30deg.)

refer to JP1/SG at Focus gain mode.



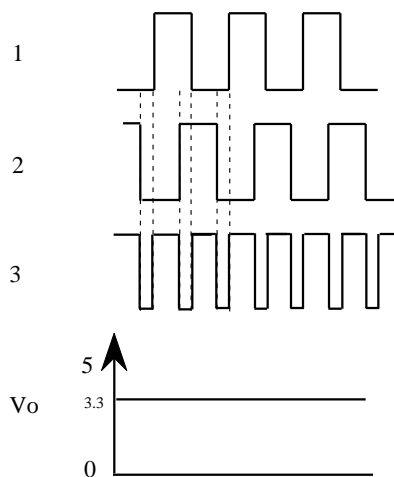
ViA(ViB) signal;

Phase shift signals (90deg.)
 refer to JP1/SG at Focus gain mode.



ViA(ViB) signal;

Phase shift signals (90+30deg.)
 refer to JP1/SG at Focus gain mode.



PRELIMINARY
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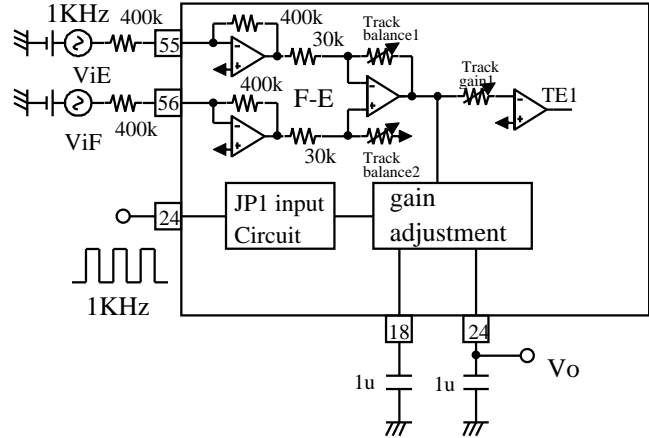
PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

(43) V_{PhTE+} , V_{PhTE-} ;

Track gain adjustment mode (show to ((76/88))
 (R3;D7=1,D4->D6=0)

V_{iE} (V_{iF}) signal;

Phase shift signals (90 \pm 30)deg.
 refer to JP1/SG at Track gain mode.



$V_{REF}=1/2V_{CC}$

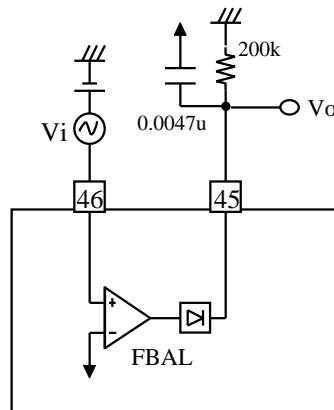
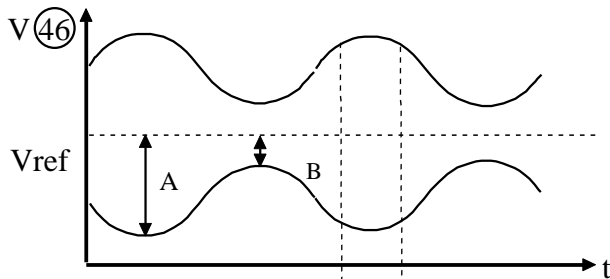
(44-1) V_{BAL} ;

Focus balance adjustment mode (show to (74/88))

(R2;D3=1,D0->D2=0)

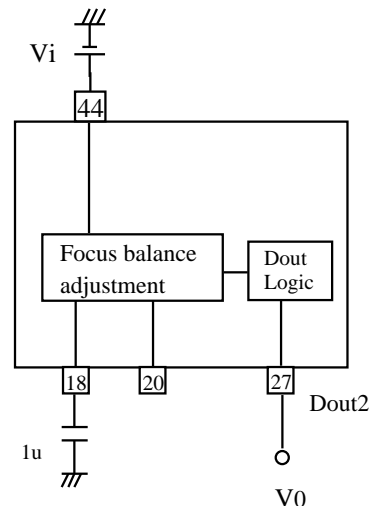
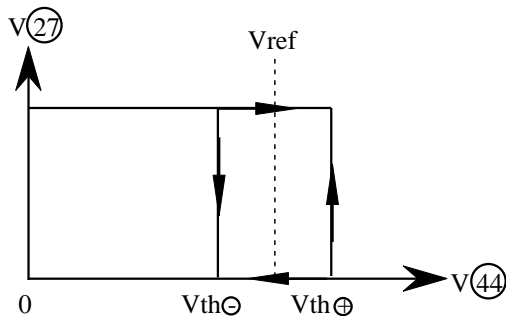
INPUT V_i (Pin 46):

$f_c=12\text{MHz}$ AM $f_{mod}=500\text{Hz}$
 $A=1.0\text{V}$, $B=0.8\text{V}$



(44-2) $V_{thFBAL+,-}$

INPUT pin44(COMP IN)



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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

(45)VBALT + , VBALT -;

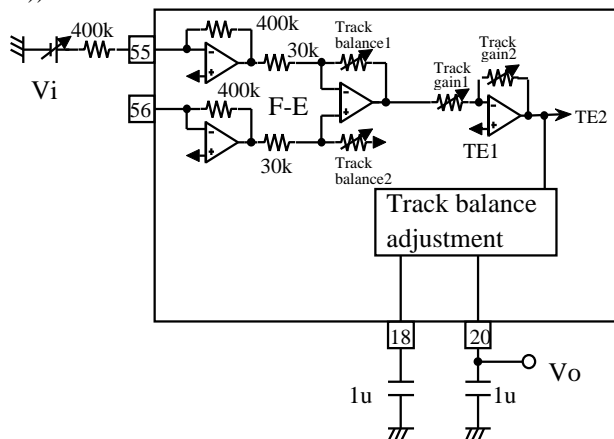
Track balance adjustment mode (show to (72/88))

(R2;D7=1,D4->D6=0)

INPUT Vi (Pin 55).

VBALT⊕:Vi=Vref-0.2V

VBALT⊖:Vi=Vref+0.2V



(46)fHADJ;

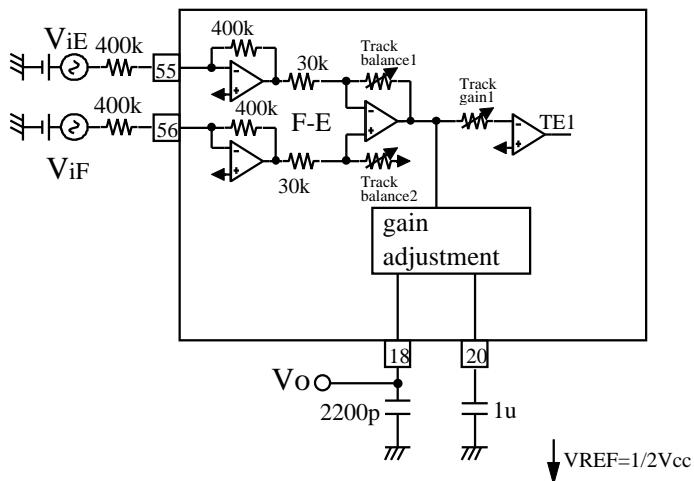
Track gain adjustment mode (show to (76/88))

(R3;D7=1,D4->D6=0)

INPUT ViE(ViF)

$$GVADJ = \frac{V_o}{V_{iE} (V_{iF})}$$

fHADJ ; 3dB down (refer to 500Hz)



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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

ELECTRICAL CHARACTERISTICS(6/6)

(Ta=25deg., Vcc=5V, f=1kHz, CBA=100, D=0, unless otherwise noted)

	Symbol	Block	Parameter	Test Conditions	Measurement circuit	Limit			Unit
						Min	Typ	Max	
101	Vthc1+	CMP	Threshold	refer to VREF (CMP OFFSET SW=ON)	(47)	3	10	17	mV
102	Vthc1-		Threshold	refer to VREF (CMP OFFSET SW=ON)	(47)	-17	-10	-3	mV
103	Vhy1s		Hysteris	refer to VREF (CMP OFFSET SW=ON)	(47)	8	20	32	mV
104	Vthc2+		Threshold	refer to VREF (CMP OFFSET SW=OFF)	(47)	5	15	25	mV
105	Vthc2-		Threshold	refer to VREF (CMP OFFSET SW=OFF)	(47)	-25	-15	-5	mV
106	Vhy2s		Hysteris	refer to VREF (CMP OFFSET SW=OFF)	(47)	15	30	45	mV
107	fLC		Cut off frequency	C(Pin 20)=4.7nF	(48)	0.7	1.0	1.3	kHz
108	UAO	UA	Output	refer to VREF	(49)	-10	0	+10	mV
109	V _{COMPOF}	ADJ	Comp input offset	refer to VREF	(50)	-25.0	-13.0	-4.0	mV

PRELIMINARY
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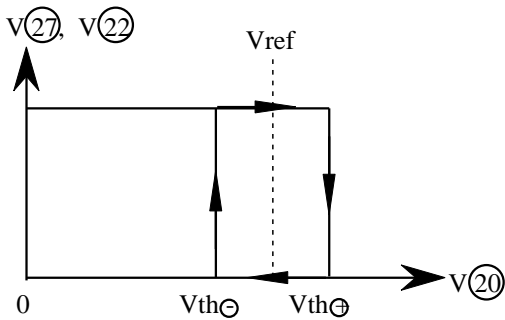
M62481FP

note(6/6)

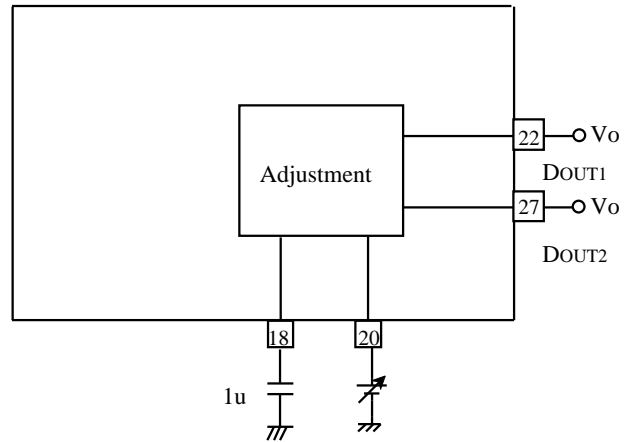
(47) $V_{thc1,2+}$, $V_{thc1,2-}$, $V_{hy1,2s}$;

V_{thc1+} , V_{thc1-} , V_{hy1s} ;CMP OFFSET=ON (Focus offset1 adjustment mode (show to (83/88)))

V_{thc2+} , V_{thc2-} , V_{hy2s} ;CMP OFFSET=OFF (Focus gain adjustment mode (show to (78/88)))



$$V_{hy1,2s} = V_{thc1,2+} - V_{thc1,2-}$$



(48) f_{LC};

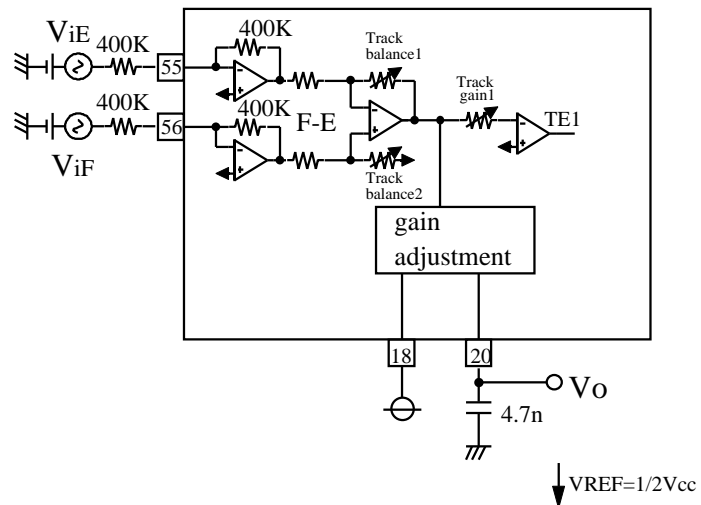
Track gain adjustment mode (show to (72/88))

(R3;D7=1,D4->D6=0)

INPUT $V_{iE}(V_{iF})$

$$G_{VADJ} = \frac{V_o}{V_{iE}(V_{iF})}$$

f_{HADJ} ; 3dB down (refer to 500Hz)



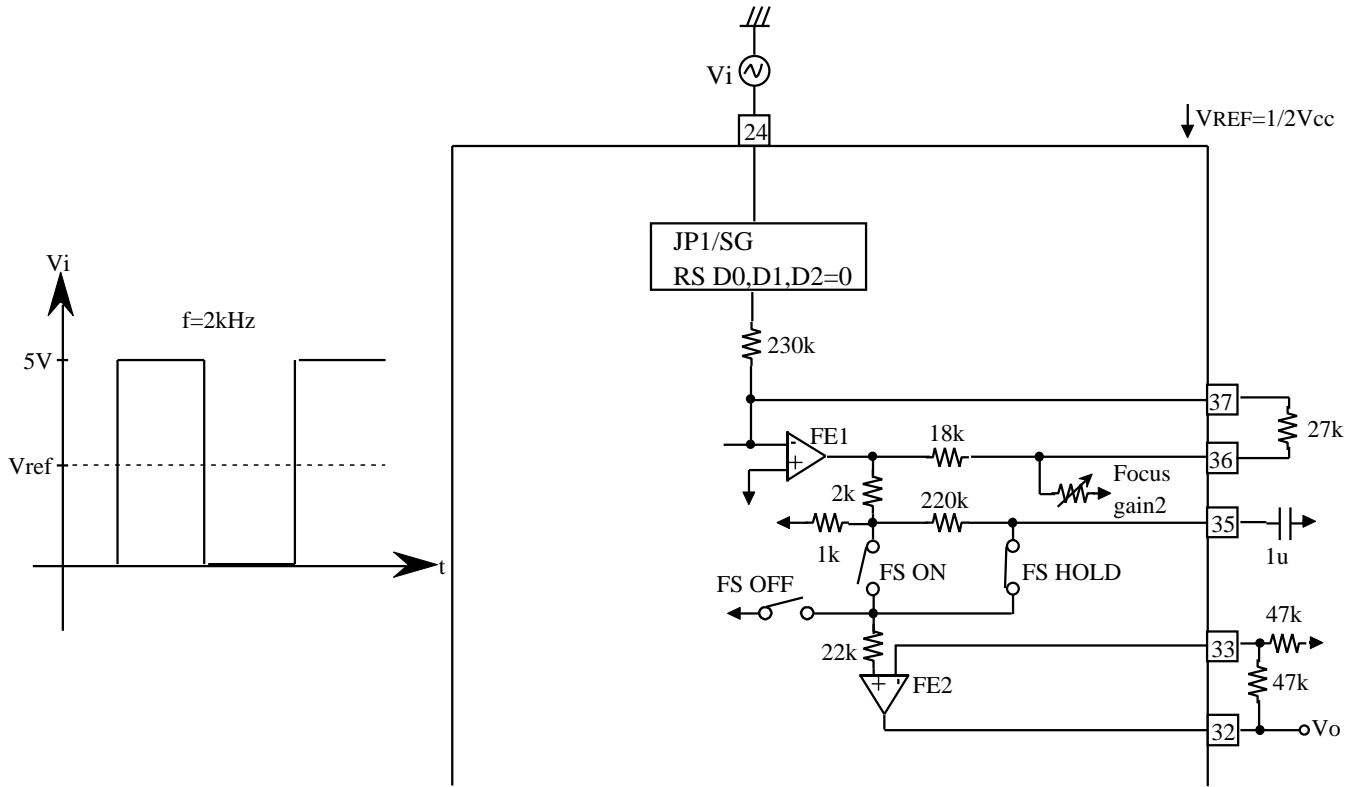
PRELIMINARY
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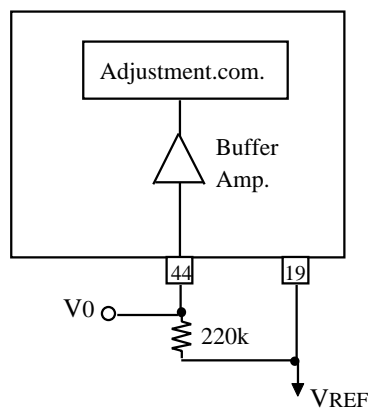
PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

(49)U_{AO}

Focus servo hold mode AUT FSON(R1 D5)=0,FS HOLD (R1 D6)=0,FS OFF (R1 D7)=0,
 Focus gain adjustment mode FGAIN (R3 D13)=1,
 Amplitude of adjustment U_A signal RS D0=0,RS D1=0,RS D2=0,



(50)V_{COMPOF}

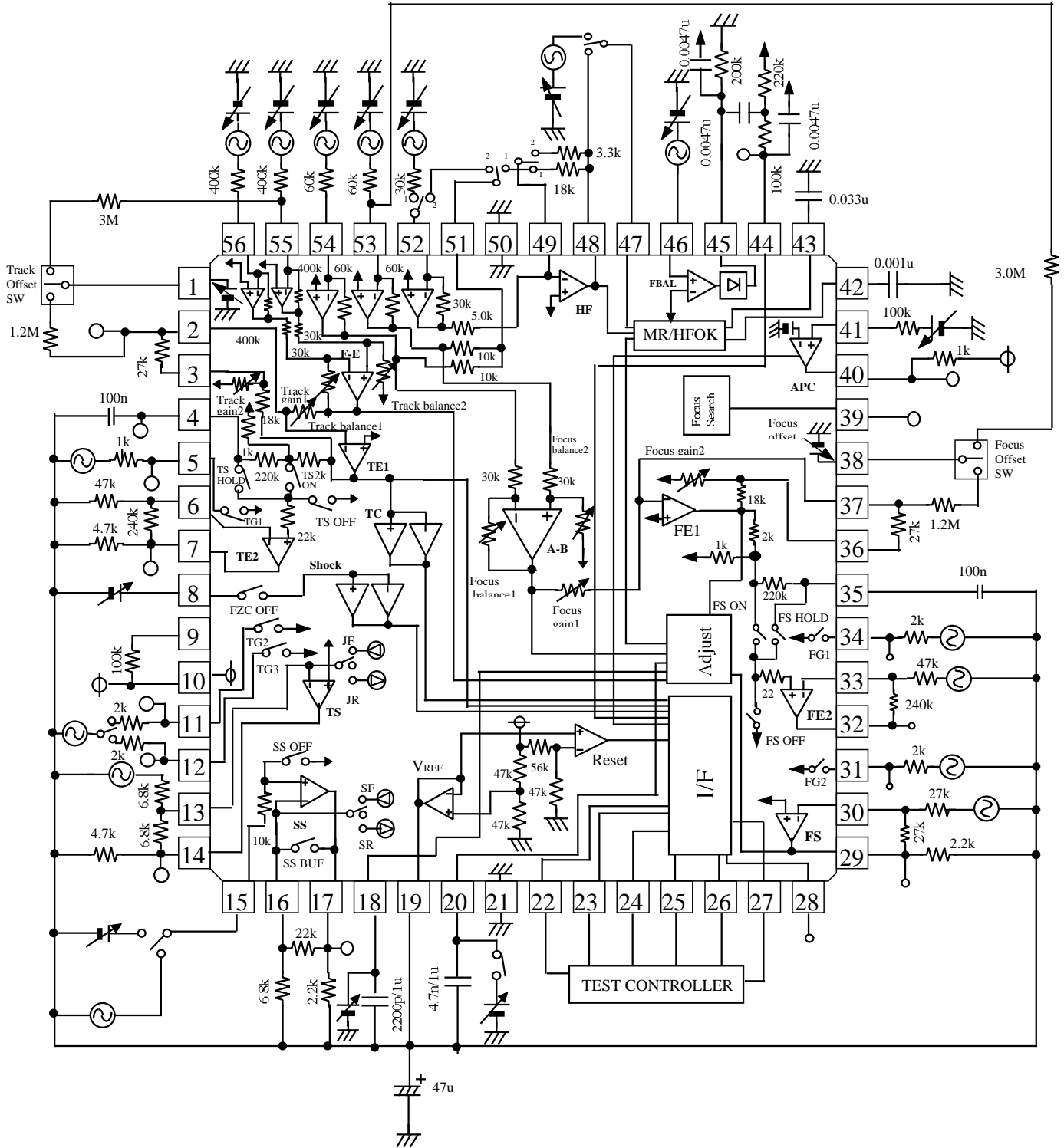


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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

TEST CIRCUIT



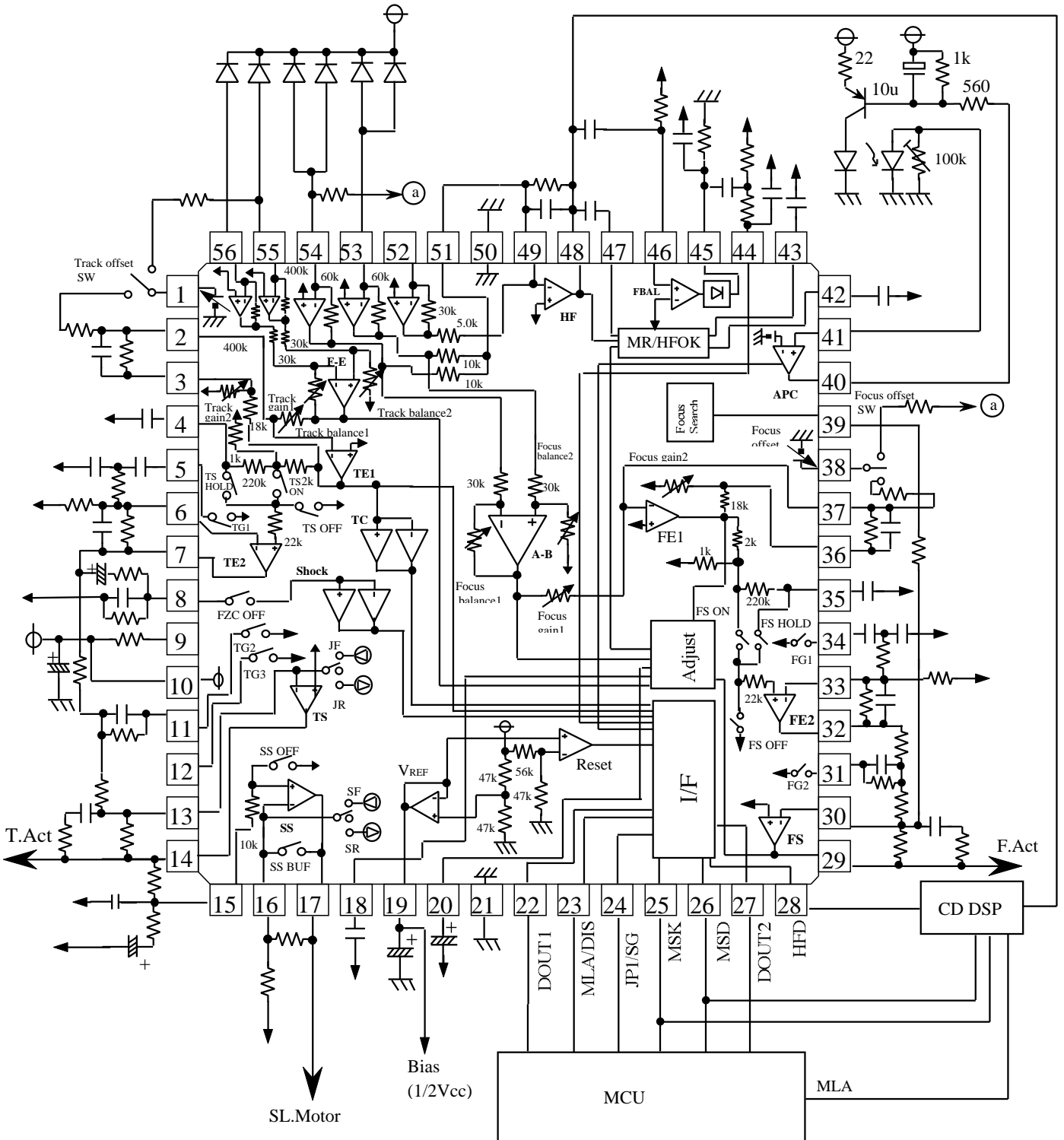
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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

APPLICATION CIRCUIT



Units Resistance : Ohm
 Capacitance:F

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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

Functional Description

of M62481FP

- MCU Interface
- Servo Circuit
- Basic control software

(Note)

This description is based on the typical use of M62481FP.

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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

SERVO CONTROL COMMAND TABLE

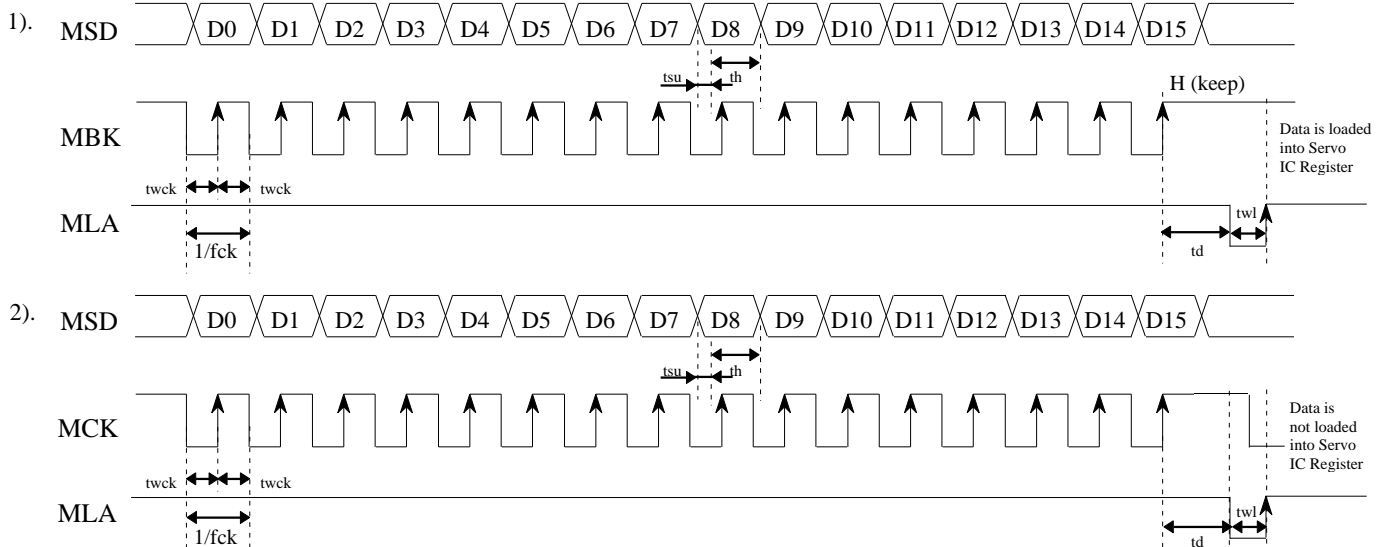
•Command Table

Register	D15	D14	D13	D12	D11	D10	D9	D8
RS	X	X	X	X	X	X	X	X
R0	0	0	KICK DIS	HFD MODE	DOUT MODE		TBAL	SHOCK EN
R1	0	1	BW WIDE	Focus Search				
				FS4	FS3	FS2	FS1	FS0
R2	1	0	Track offset (3bit)			Focus offset (3bit)		
R3	1	1	FGAIN	TGAIN	FBAL	TG3	G2 INV	HI GAIN

Register	D7	D6	D5	D4	D3	D2	D1	D0
RS	X	X	X	X	X	ADJ AMP2	ADJ AMP1	ADJ AMP0
R0	FZC OFF	TS HOLD	BRAKE	TS SERVO		SS PLAY	SS SERVO	
R1	FS OFF	FS HOLD	AUT FSON	LASER ON	ADJ FO1	ADJ FO2	ADJ TO1	ADJ TO2
R2	Track Balance (4bit)				Focus Balance (4bit)			
R3	Track gain (4bit)				Focus gain (4bit)			

(RS: Shift resistor, X : not used)

• Command Timing Chart



Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
fck	Clock frequency		—	125	500	kHz
twck	Clock width		2	4	—	u sec
tsu	Set-up time		0.1	0.2	—	u sec
th	Hold time		2	4	—	u sec
td	Delay time		2	4	—	u sec
twl	Latch width		1	4	—	u sec

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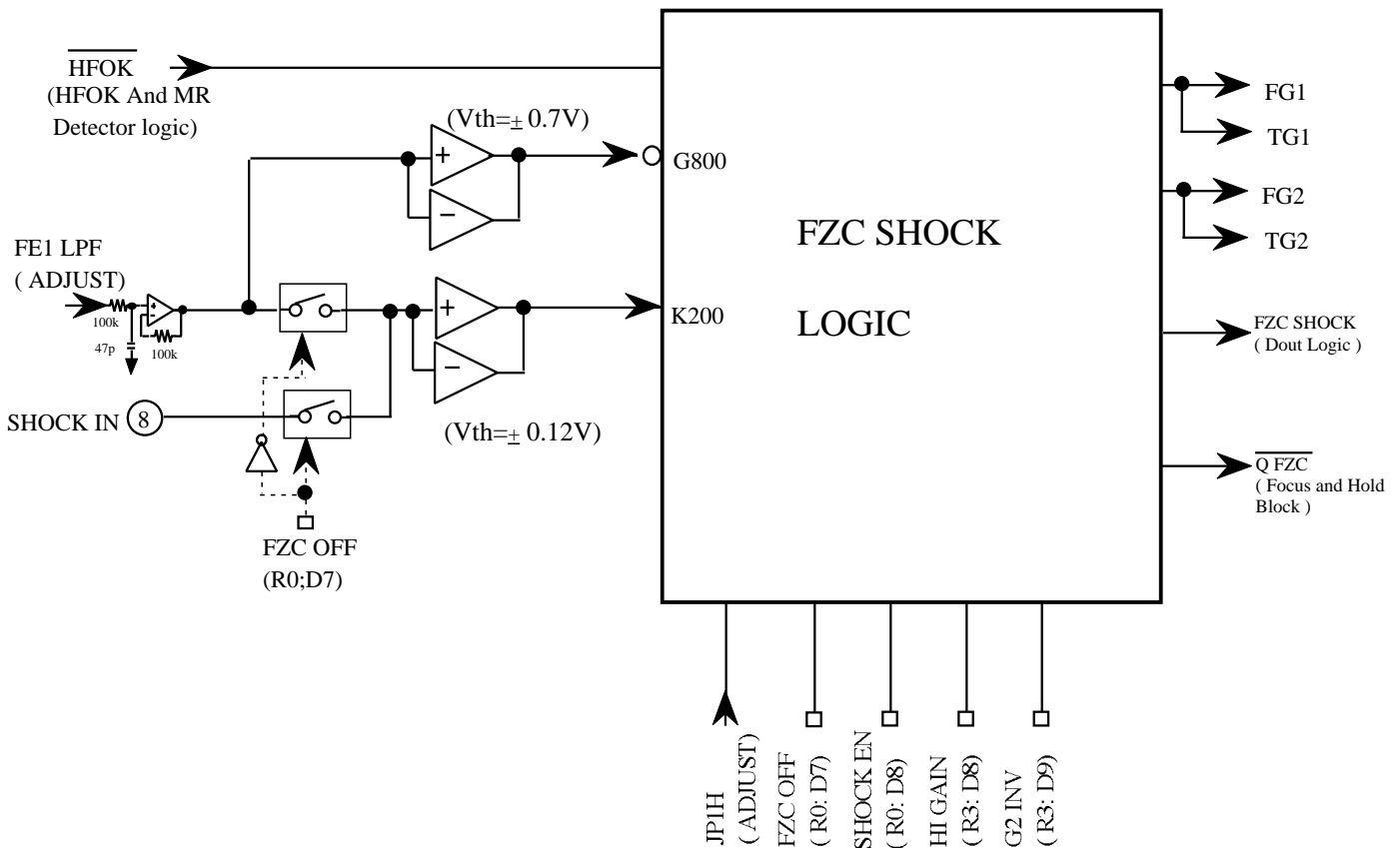
SERVO CONTROL

(1). FOCUS

• LASER ON

MODE	R1; D4 LASER ON	FUNCTION
Laser OFF	0	•APC Amp OFF
Laser ON	1	•APC Amp ON

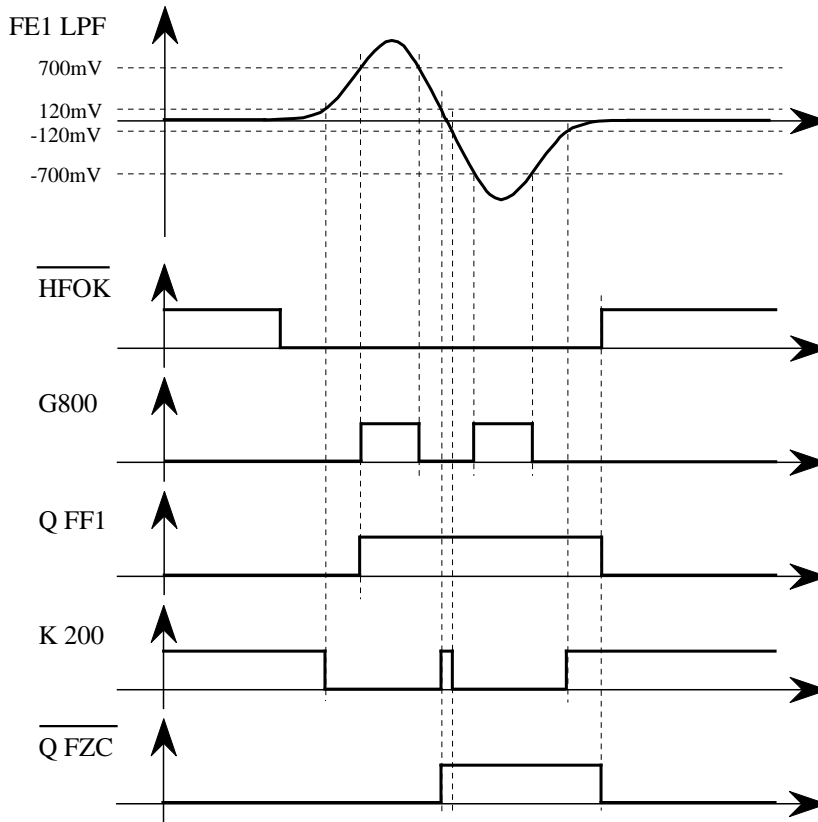
•F-1). FZC Shock Circuit



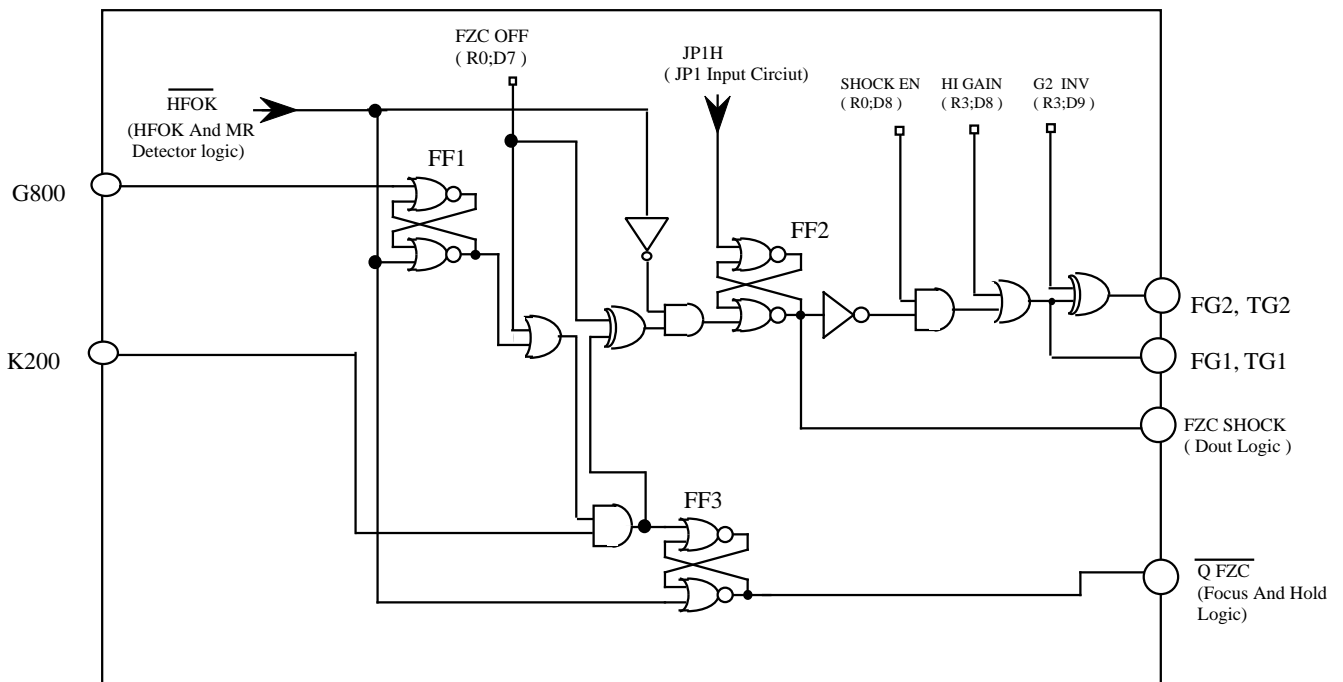
PRELIMINARY
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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT



F-1-1) FZC Shock Logic



PRELIMINARY
 Notice ; This is not a final specification.
 some parametric limits are subject to change.

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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

● F-2). Focus and Hold Logic

Q FZC	HFOK	R1; D6 FS HOLD	R1; D5 AUTO FSON	R1; D7 FS OFF	Switches			Function
					FS OFF	FS ON	FS HOLD	
X	X	0	0	0	Open	Open	Close	Forced Hold
X	X	0	0	1	Close	Open	Close	Open loop
X	1	0	1	0	Close	Open	Close	Auto Focus Wait (open loop)
0	0	0	1	0	Close	Open	Close	Auto Focus Wait (open loop)
1	0	0	1	0	Open	Close	Open	Auto Focus Caught (closed loop)
X	X	0	1	1	Close	Open	Open	Not Used
X	1	1	0	0	Open	Open	Close	Hold active
X	0	1	0	0	Open	Close	Open	Close loop with Hold Enable
X	1	1	0	1	Open	Open	Close	Holded with Auto Focus wait
0	X	1	0	1	Open	Open	Close	Holded with Auto Focus wait
1	0	1	0	1	Open	Close	Open	Auto Focus Caught closed Loop
X	X	1	1	0	Open	Close	Open	Close loop forced
X	X	1	1	1	Close	Open	Open	Open loop/keep Hold Voltage

PRELIMINARY
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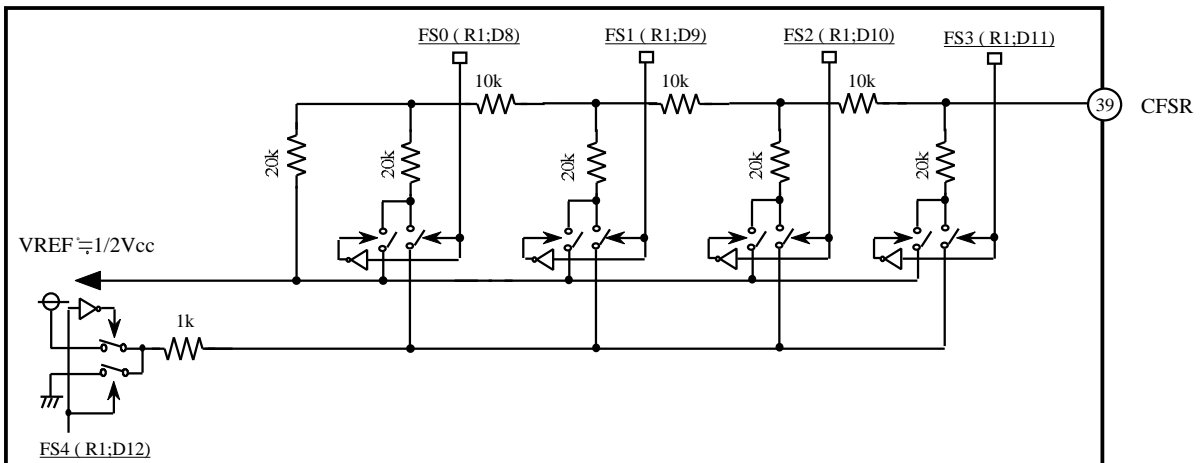
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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

•F-3). Focus Search Circuit (R1; D8 -> D12)

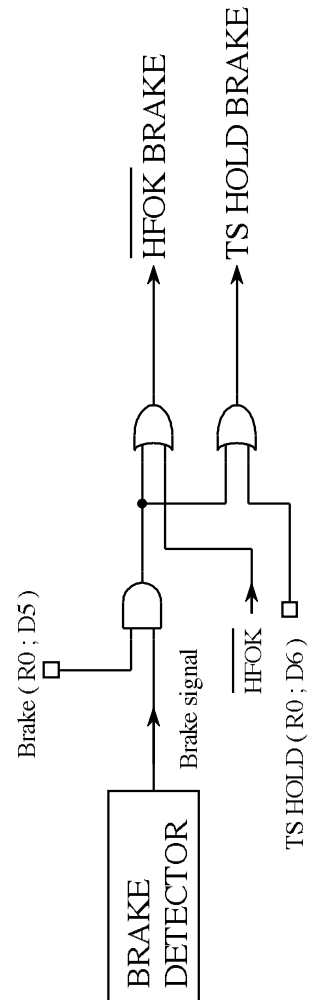
Pin ③⑨ VCFSR ; Voltage : 2.5 -> 5.0 V (16 steps) 156 mV/step (R1; D12=1)
 0 -> 2.5 V (16 steps) - 156 mV/step (R1; D12=0)

FS4 (D12)	FS3 (D11)	FS2 (D10)	FS1 (D9)	FS0 (D8)	Pin ③⑨ VCFSR(V)
0	1	1	1	1	0.908
0	1	1	1	0	1.009
0	1	1	0	1	1.111
0	1	1	0	0	1.214
0	1	0	1	1	1.321
0	1	0	1	0	1.424
0	1	0	0	1	1.529
0	1	0	0	0	1.635
0	0	1	1	1	1.754
0	0	1	1	0	1.856
0	0	1	0	1	1.961
0	0	1	0	0	2.067
0	0	0	1	1	2.178
0	0	0	1	0	2.283
0	0	0	0	1	2.391
0	0	0	0	0	2.500
1	0	0	0	0	2.500
1	0	0	0	1	2.611
1	0	0	1	0	2.723
1	0	0	1	1	2.834
1	0	1	0	0	2.946
1	0	1	0	1	3.058
1	0	1	1	0	3.169
1	0	1	1	1	3.280
1	1	0	0	0	3.393
1	1	0	0	1	3.505
1	1	0	1	0	3.616
1	1	0	1	1	3.727
1	1	1	0	0	3.838
1	1	1	0	1	3.949
1	1	1	1	0	4.060
1	1	1	1	1	4.169



T-1). Track Hold Logic

	HFOK BRAKE	R0;D4		R0;D3		Switches			Function
		TS HOLD BRAKE	TS SERVO	TS SERVO	R0;D3	TS OFF	TS ON	TS HOLD	
1)	X	0	0	0	0	Open	Close	Open	Close Loop
	X	0	0	1	1	Open	Close	Open	JR-with Close Loop
	X	0	1	0	0	Open	Close	Open	JF-with Close Loop
	X	0	1	1	1	Open	Open	Close	Forced Hold
1)	X	1	0	0	0	Close	Open	Open	Open loop
	X	1	0	1	1	Close	Open	Open	JR-with Open loop
	X	1	1	0	0	Close	Open	Open	JF-with Open loop
2)	0	1	1	1	1	Open	Close	Open	Close loop with Hold Enable
2)	1	1	1	1	1	Open	Open	Close	Hold active



- 1). Brake function switches between "Close Loop" and "Open Loop".
- 2). Brake function switches between "Close Loop with Hold enable" and "Hold Active".

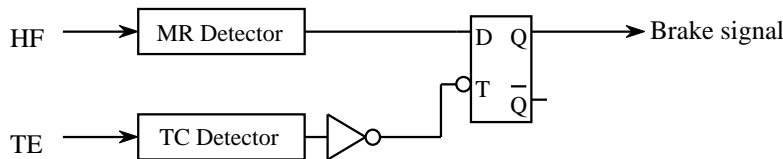
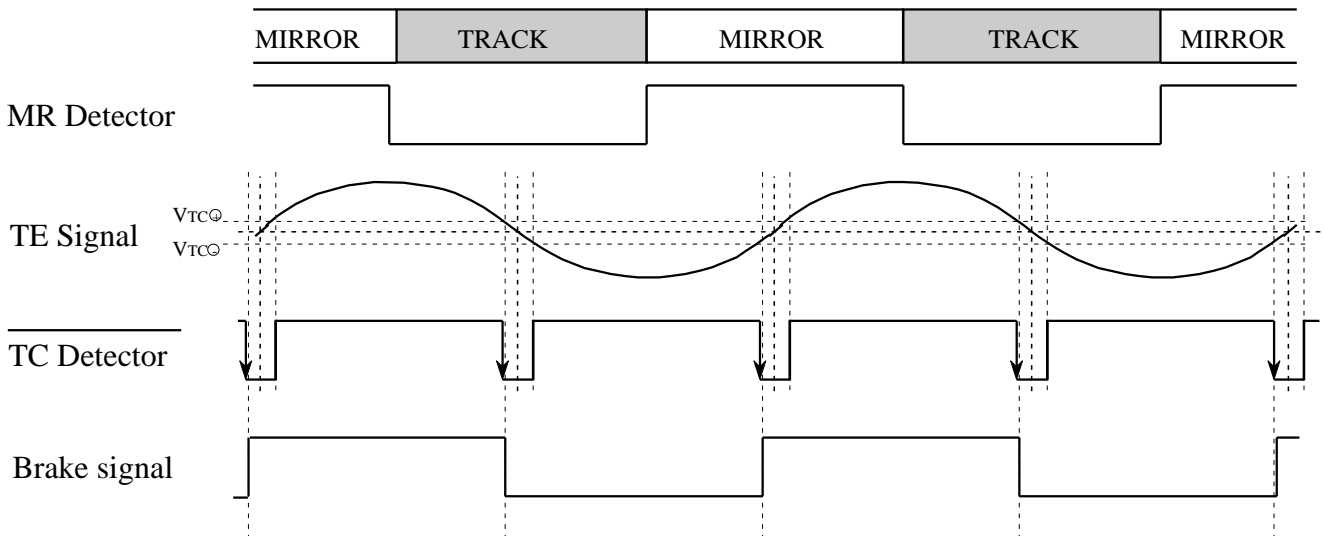
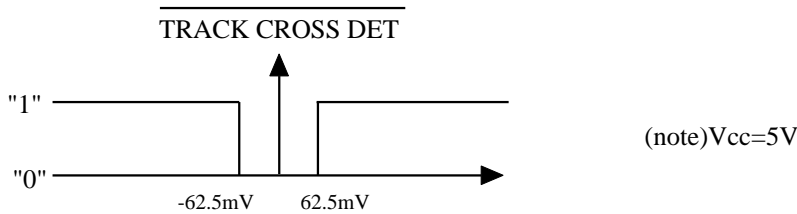
PRELIMINARY
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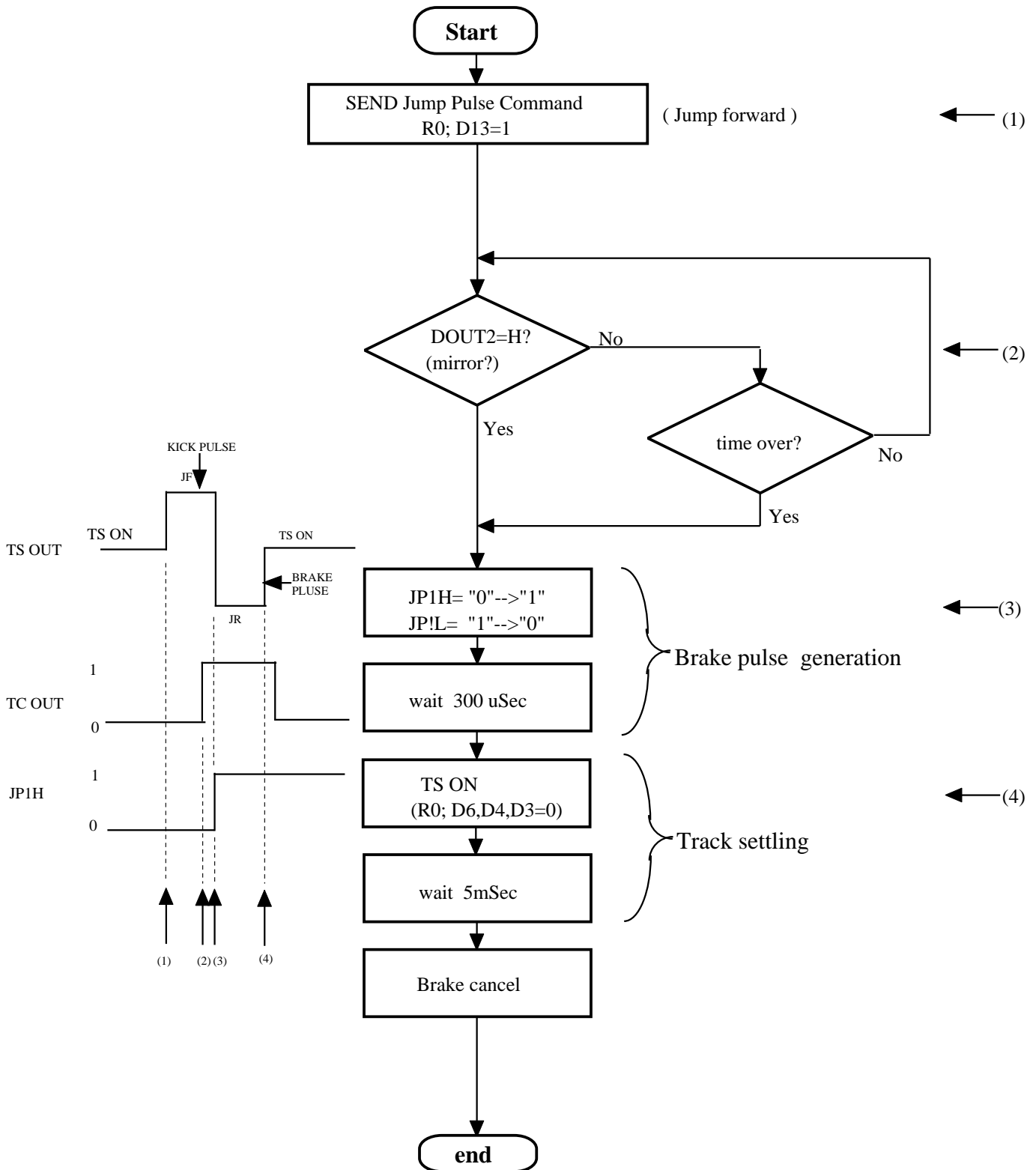
•T-2). BRAKE DETECTOR (R0; D5=1)

Jump Brake operation

INPUT CONDITION		OUTPUT
MIRROR	TC Detector	Brake signal
1 ("Mirror")		OPEN
0 ("Track")		CLOSE



(example)Single track jump



PRELIMINARY
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•T-3). Track Kick Logic (R0 ;)

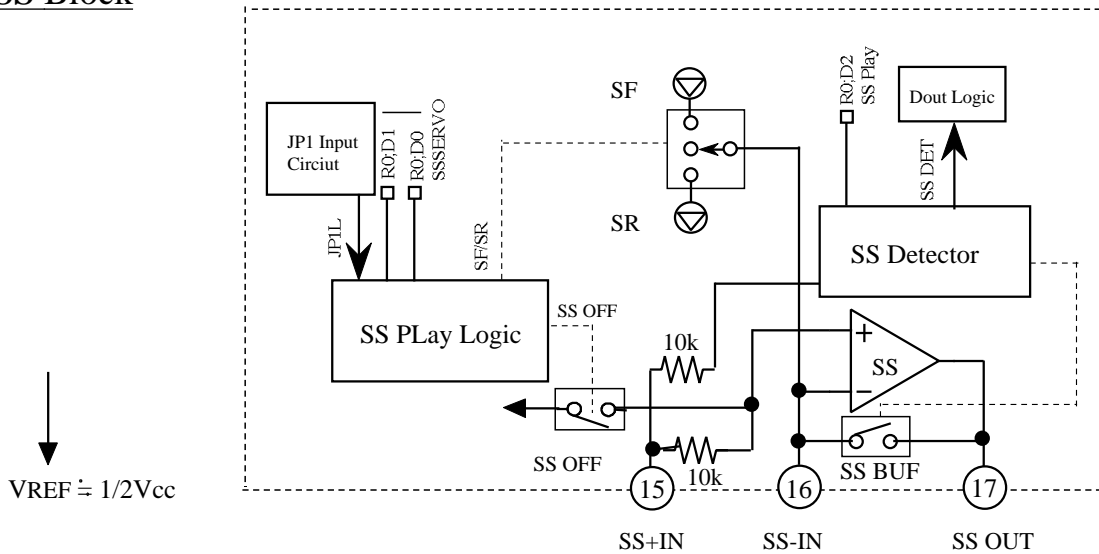
Internal JP1H	Internal JP1L	D13 KICK DIS	D4	D3	Switches		Function
			TS SERVO		JF	JR	
0	0	1	X	X	open	open	No Track Jump
0	1	1	X	X	close	open	JP1-Track Jump Forward
1	0	1	X	X	open	close	JP1-Track Jump Reverse
0	X	0	0	0	open	open	No Track Jump
0	X	0	0	1	open	close	Track Jump Reverse
0	X	0	1	0	close	open	Track Jump Forward
0	X	0	1	1	open	open	No Track Jump
1	0	0	0	0	open	open	No Track Jump
1	0	0	0	1	close	open	JP1 Direct Command
1	0	0	1	0	open	close	JP1 Direct Command
1	0	0	1	1	open	open	No Track Jump

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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

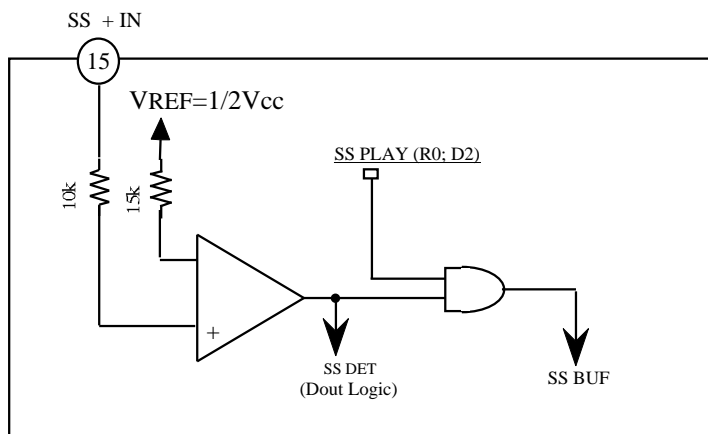
S). SS Block



•S-1). SS PLAY Logic (R0;)

Internal JP1L	D1	D0	Switches			Function
	SS SERVO		SS OFF	SF	SR	
X	0	0	close	open	open	Sledge Servo OFF
0	0	1	close	open	close	Sledge Move Reverse
1	0	1	close	open	open	Sledge Move disabled
0	1	0	close	close	open	Sledge Move Forward
1	1	0	close	open	open	Sledge Move disabled
X	1	1	open	open	open	Sledge Servo ON

•S-2). SS Detector

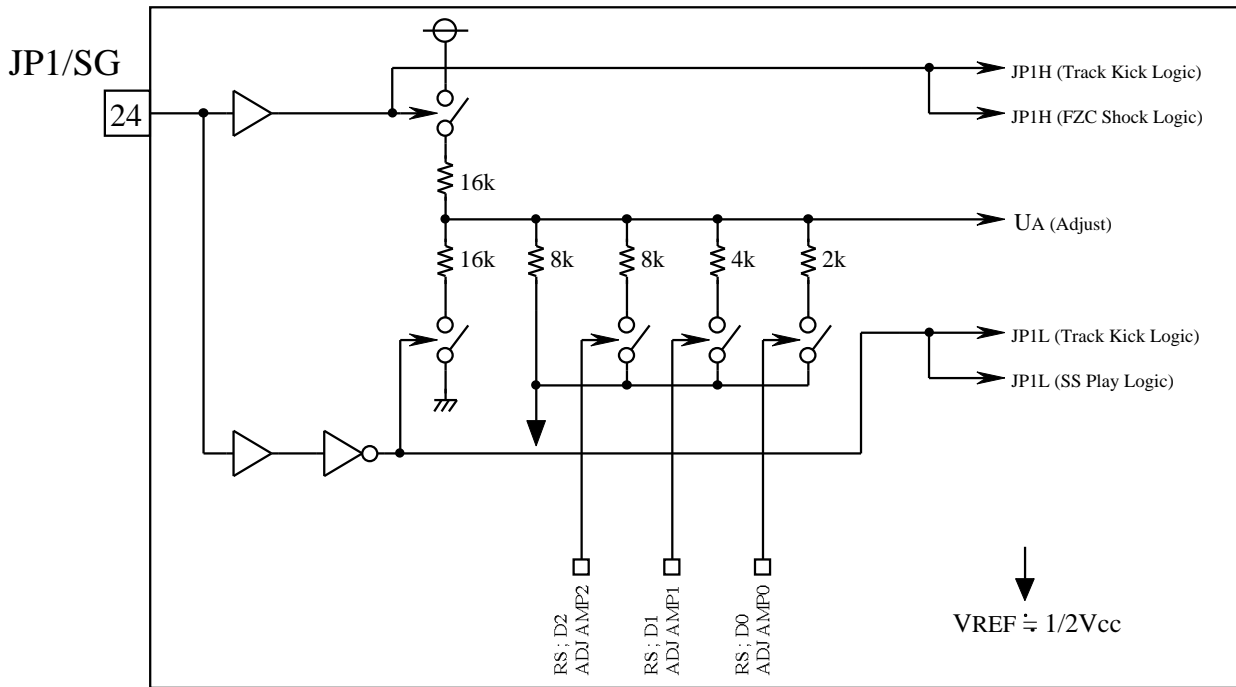


SS+IN Pin 15	R0:D2 SS PLAY	Switch	SS DET (Dout Logic)
		SS BUF	
0	0	open	L
0	1	open	L
1	0	open	H
1	1	close	H

PRELIMINARY
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•A-1). JP1 INPUT Circuit



UA: SG(Internal)

	RS;D0	RS;D1	RS;D2	Ua(V)
0	0	0	0	±0.83
1	0	0	1	±0.5
2	0	1	0	±0.36
3	0	1	1	±0.28
4	1	0	0	±0.23
5	1	0	1	±0.19
6	1	1	0	±0.17
7	1	1	1	±0.15

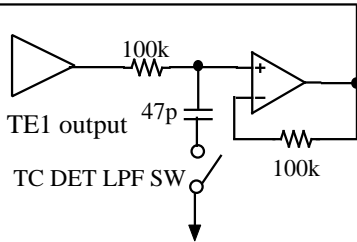
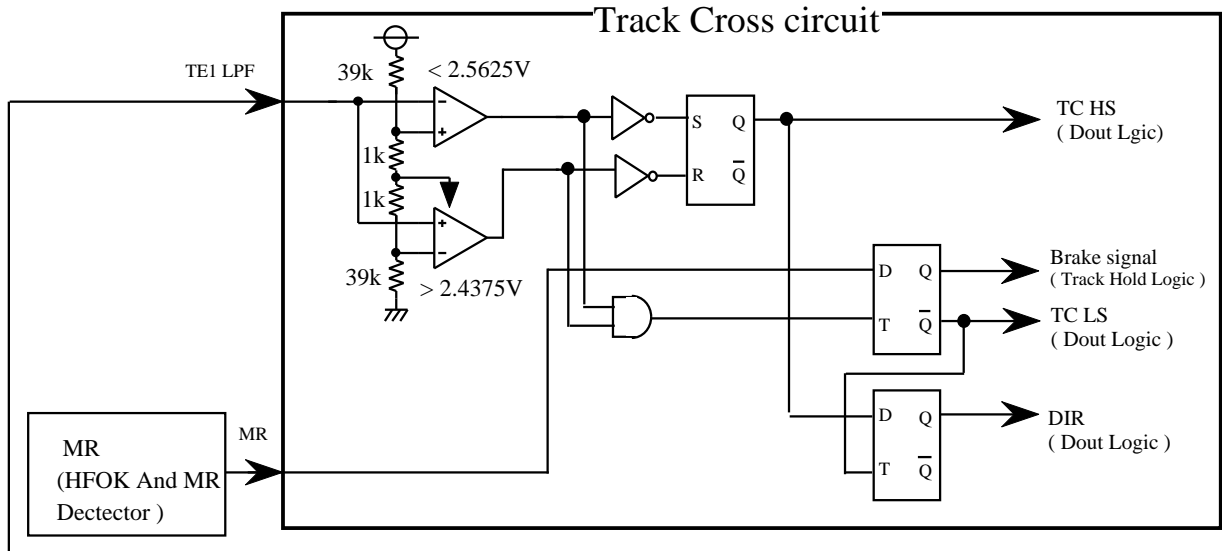
(Vref (Standard))

Pin24;JP1/SG	JP1H	JP1L
0	0	1
1	1	0
Tristate	0	0

PRELIMINARY
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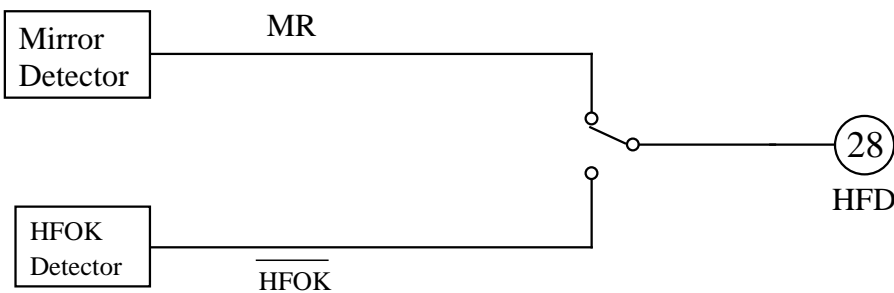
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•T-4). Track Cross Detector Block



R3;D11 FBAL	TC DET LPF SW
0	open
1	close

•L-1).HFD MODE (R0;D12)



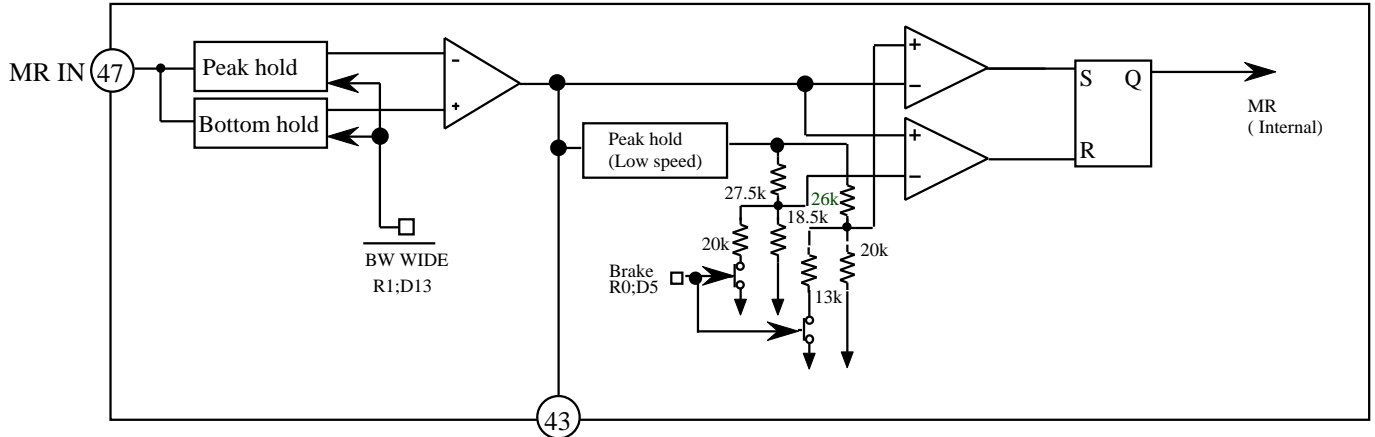
R0;D12 HFD MODE	HFD OUTPUT
0	$\overline{\text{HFOK}}$
1	MR

PRELIMINARY
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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

•Mirror Detector Circuit



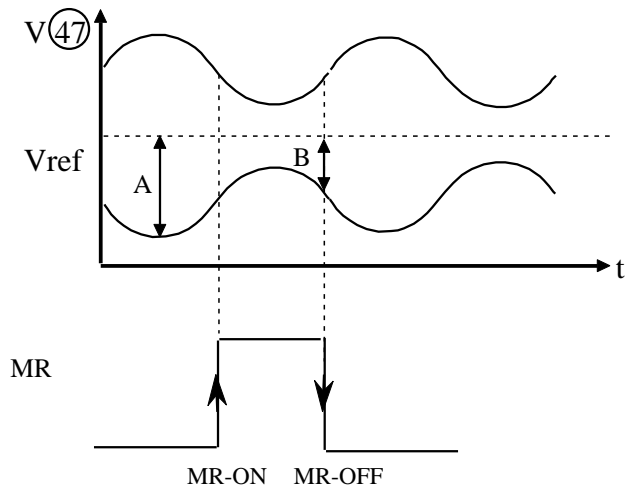
MRC

↓ VREF ≐ 1/2Vcc

Brake Bit

• MR ratio

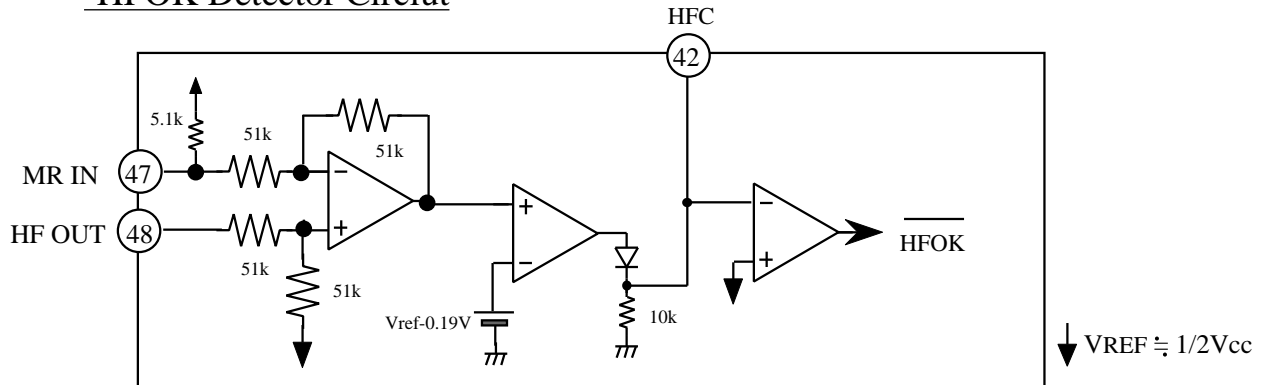
Brake (R0; D5)	Switch	MR(Ratio)
0	Close	0.41 :MR-ON 0.47 :MR-OFF
1	Open	0.52 :MR-ON 0.58 :MR-OFF



$$MR(\text{Ratio}) = \frac{B}{A} = 0.41 :MR-ON, 0.47 :MR-OFF \text{ (normal)}$$

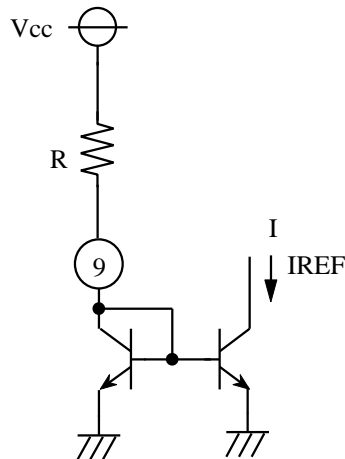
$$= 0.52 :MR-ON, 0.58 :MR-OFF \text{ (brake)}$$

•HFOK Detector Circuit



PRELIMINARY
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•L-2). Jump/Sledge Pulse Current



<Jump Pulse Current>

$$I_{JF}, I_{JR} = \frac{V_{cc} - V_{BE}}{2R}$$

<Sledge Pulse Current>

$$I_{SF}, I_{SR} = \frac{V_{cc} - V_{BE}}{R}$$

(example)

$$V_{cc}=5(V), V_{BE}=0.7(V), R=100(k \quad)$$

$$I_{JF}, I_{JR}=21.5 \text{ (}\mu\text{A)}$$

$$I_{SF}, I_{SR}=43.0 \text{ (}\mu\text{A)}$$

PRELIMINARY
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• L-3). BW WIDE (R1 ; D13)

D13	<u>BW WIDE</u>	Track LPF (kHz)	Focus LPF(kHz)	MR Detector Cut off Frequency(kHz)
1	1 time speed	66	70	30
0	8 times speed	265	280	100

• L-4).TG3 (R3; D10)

D10	TG3 SW
0	OFF
1	ON

PRELIMINARY
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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

● L-5). Dout Logic

R0; D7 FZC OFF	R0; D11	R0; D10	PIN 22 DOUT1	PIN 27 DOUT2
	DOUT MODE			
0	0	0	FZC SHOCK ₁₎	ADJ CMP
0	0	1	ADJ AMPO ₃₎	TC HS
0	1	0	ADJ CMP	TC LS
0	1	1	TC HS	DIR
1	0	0	FZC SHOCK ₂₎	ADJ CMP
1	0	1	FZC SHOCK ₂₎	SS DET
1	1	0	TC LS	$\overline{\text{MR}}$
1	1	1	TC LS	DIR

1)...FZC : Signal is available

2)...SHOCK

3)...ADJ AMPO=RS;D0

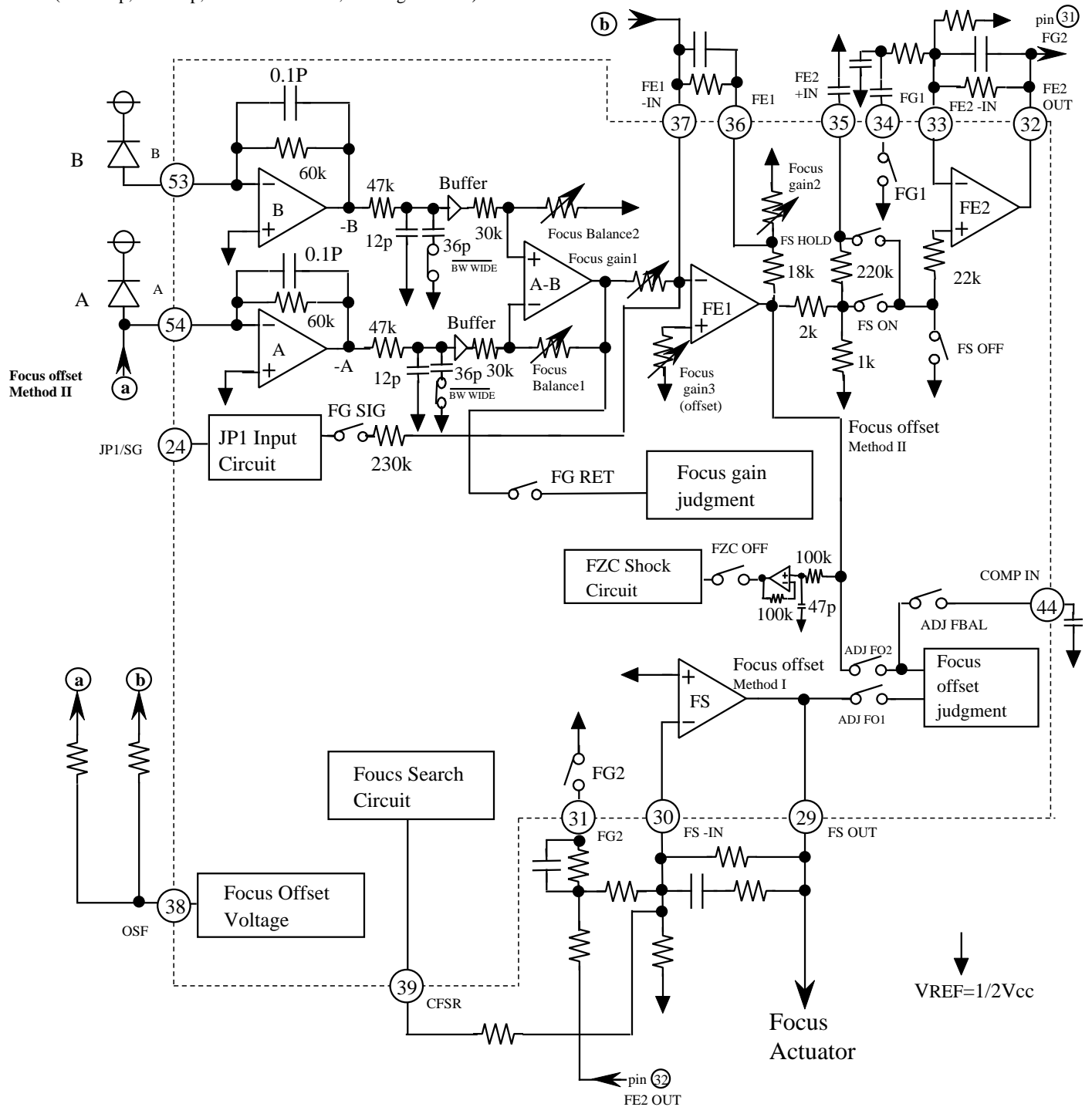
PRELIMINARY
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Focus Servo System1

(FE Amp, FS Amp, Focus offset ADJ, Focus gain ADJ)

Focus offset Method I

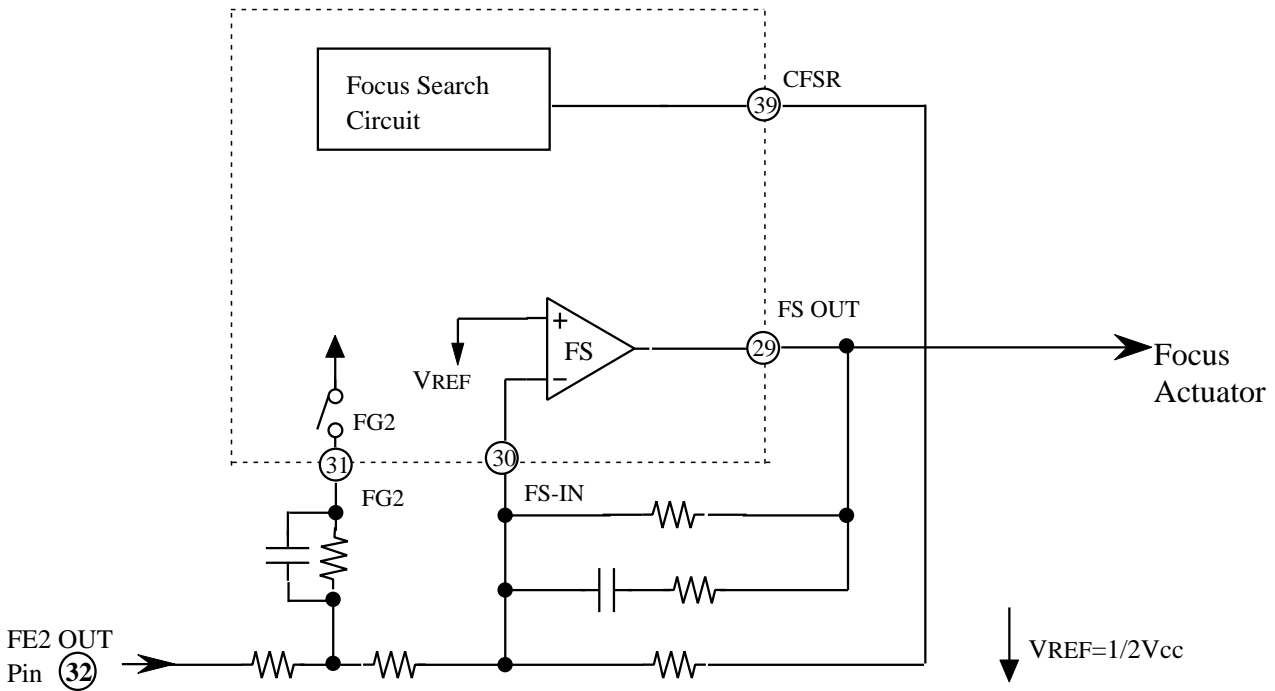


(Note) Resistors and Capacitors without value are externals.

PRELIMINARY
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Focus Search Circuit



(note)Resistors and Capacitors without value are externals except the resistor for the adjustment.

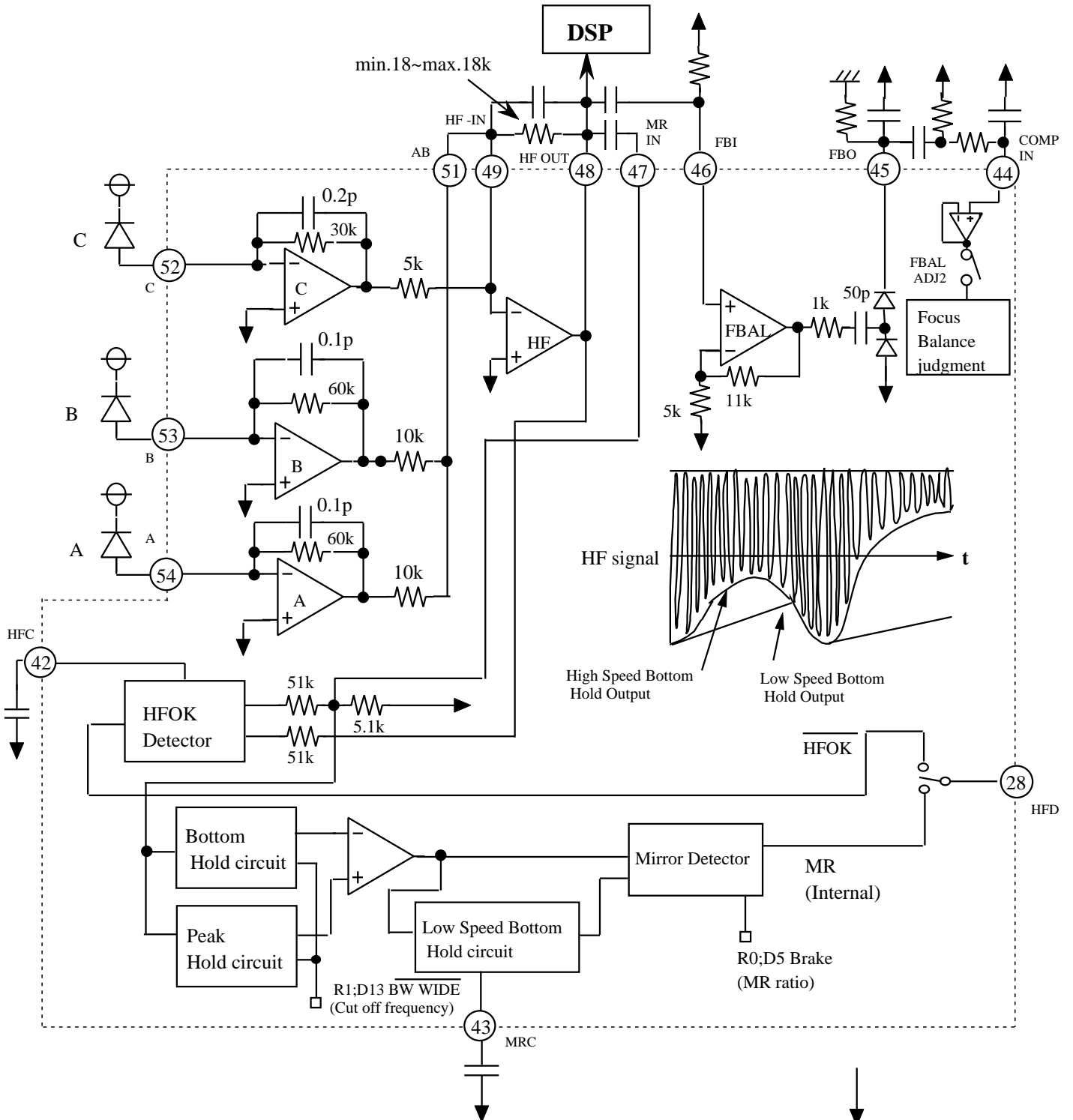
PRELIMINARY
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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

Focus Servo System2

(HF Amp, Focus Balance Detector)



(Note) Resistors and Capacitors without value are externals.

VREF=1/2Vcc

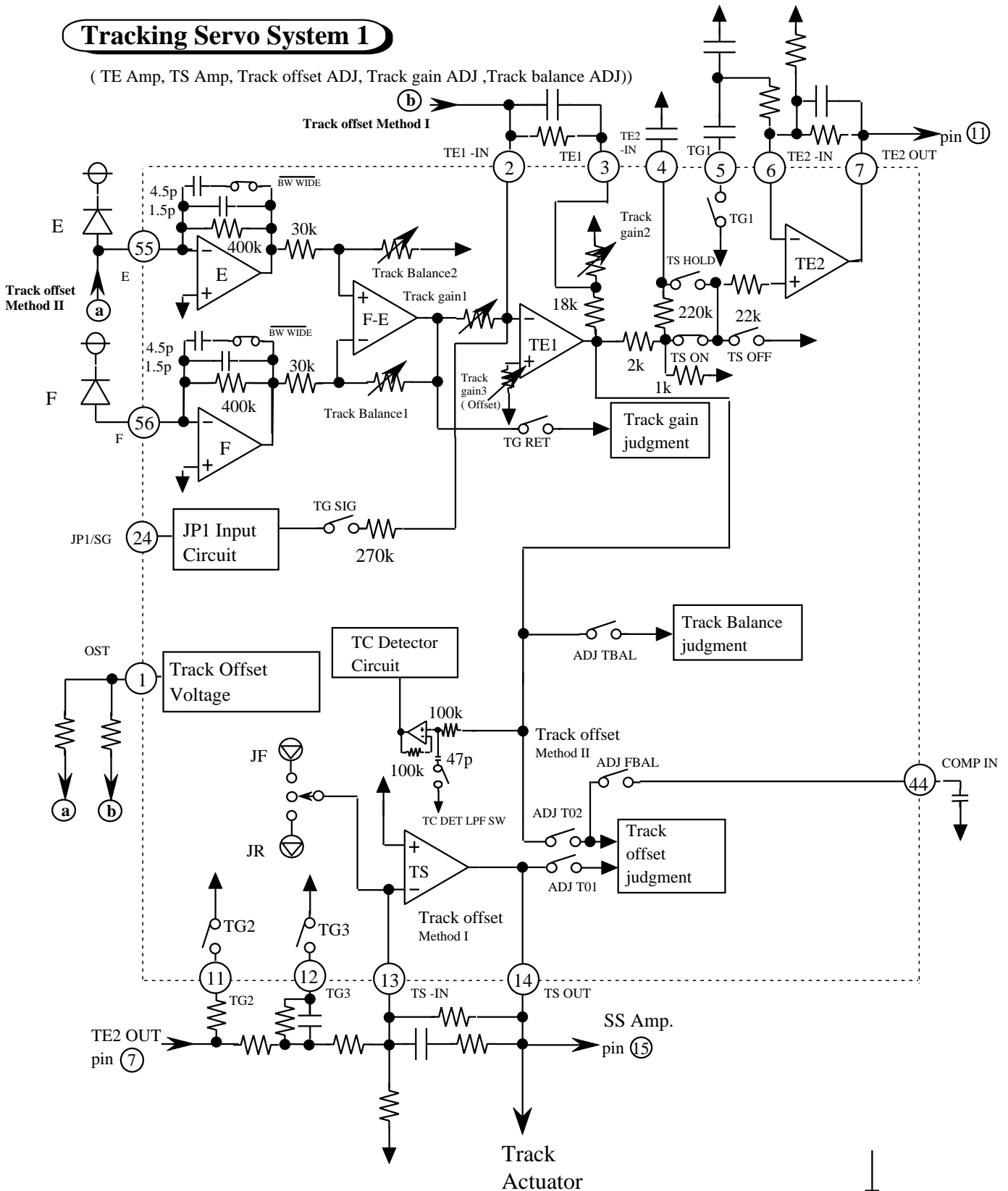
PRELIMINARY
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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

Tracking Servo System 1

(TE Amp, TS Amp, Track offset ADJ, Track gain ADJ, Track balance ADJ)



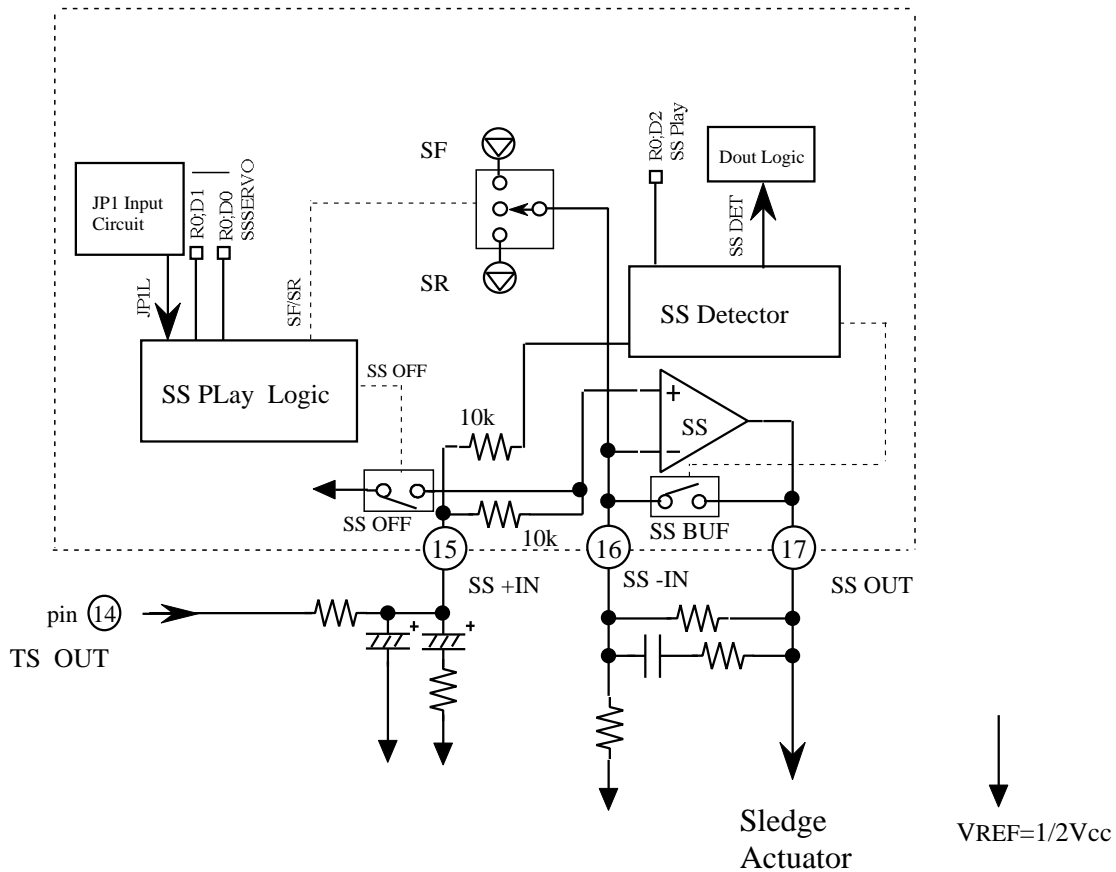
(Note) Resistors and Capacitors without value are externals.

VREF=1/2Vcc

PRELIMINARY
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Tracking Servo System 2

(SS Amp, S-1).SS Play Block and S-2). SS Detector Block)



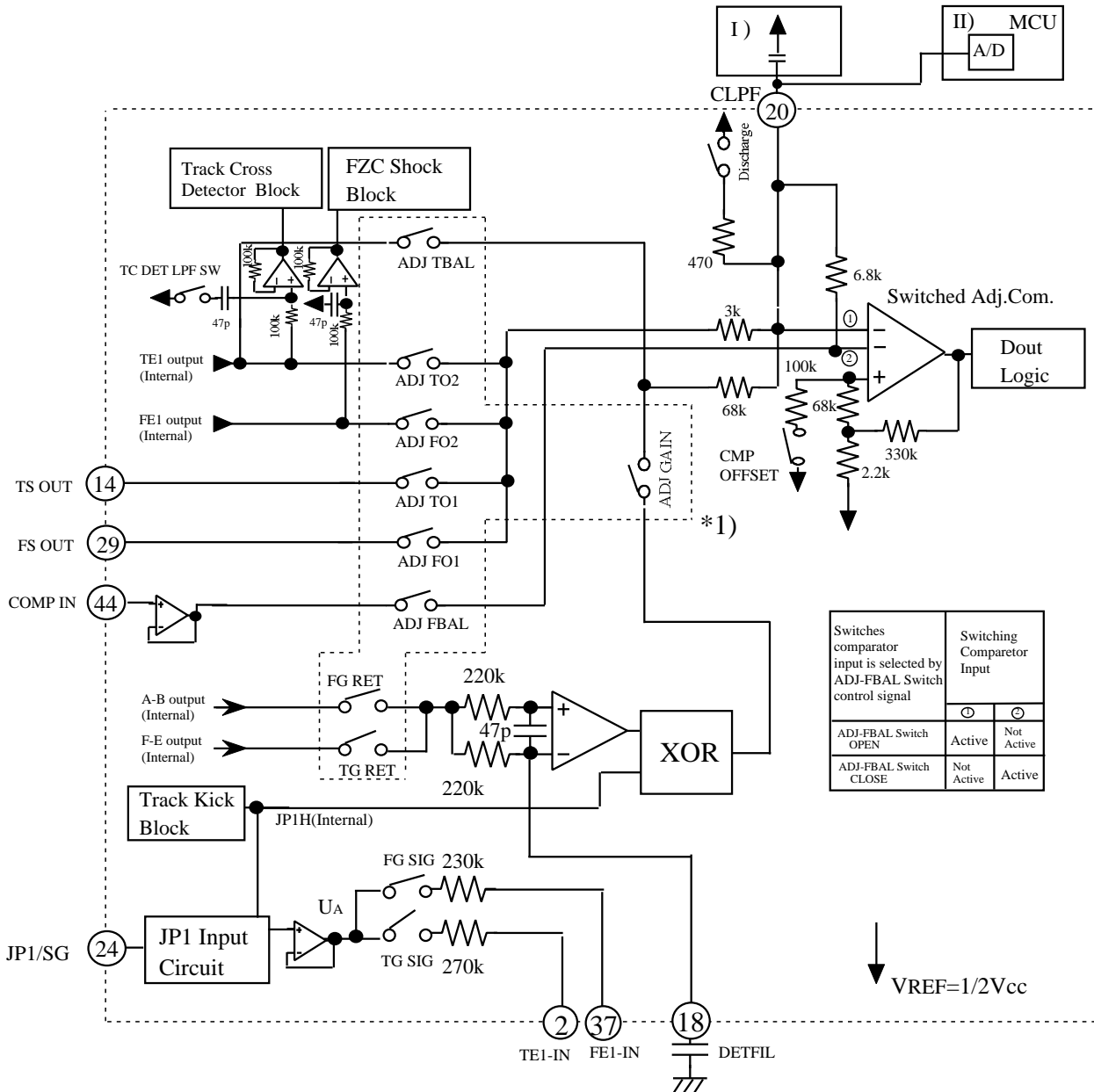
(Note) Resistors and Capacitors without value are externals.

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Adjustment Block

- I) All adjustment are done via internal Adj Comp.
- II) No capacitor at CLPF pin, MCU A/D convertor at CLPF pin. All adjustment are done via A/D in MCU. All adjustment signals (Focus offset method 1.2 , Track offset method 1.2, Focus balance , Track balance , Focus gain and Track gain) are aviable at CLPF pin .



*1) The IC is protected , if more than one of the switches (ADJ GAIN,ADJ TBAL, ADJ TO2,ADJ FO2,ADJ TO1,ADJ FO1,ADJ FBAL FG RET or TG RET) are closed at the same time.

It is not a resonable and specified adjustment mode,if more than one of the switches ADJ GAIN,ADJ TBAL,ADJ TO2,ADJ FO2,ADJ TO1,ADJ FO1,ADJ FBAL are closed at the same time.

(Note) Resistors and Capacitors without value are externals.

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Adjustment Switch

• ADJ FO1 (R1;D3)

BIT	SWITCH	Remark
R1 ; D3 ADJ FO1	ADJ FO1	
0	OPEN	———
1	CLOSE	Focus offset I adjustment

• ADJ FO2 (R1;D2)

BIT	SWITCH	Remark
R1 ; D2 ADJ FO2	ADJ FO2	
0	OPEN	———
1	CLOSE	Focus offset II adjustment

• ADJ TO1 (R1;D1)

BIT	SWITCH	Remark
R1 ; D1 ADJ TO1	ADJ TO1	
0	OPEN	———
1	CLOSE	Track offset I adjustment

• ADJ TO2 (R1;D0)

BIT	SWITCH	Remark
R1 ; D0 ADJ TO2	ADJ TO2	
0	OPEN	———
1	CLOSE	Track offset II adjustment

PRELIMINARY
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Recommended Adjustment Function

Control bits				Switches				Remark
R1:D3 ADJ FO1	R1:D2 ADJ FO2	R1:D1 ADJ TO1	R1:D0 ADJ TO2	ADJ FO1	ADJ FO2	ADJ TO1	ADJ TO2	
0	0	0	0	open	open	open	open	—
1	0	0	0	close	open	open	open	Focus offset method1 adjustment.
0	1	0	0	open	close	open	open	Focus offset method2 adjustment.
0	0	1	0	open	open	close	open	Track offset method1 adjustment.
0	0	0	1	open	open	open	close	Track offset method2 adjustment.

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PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

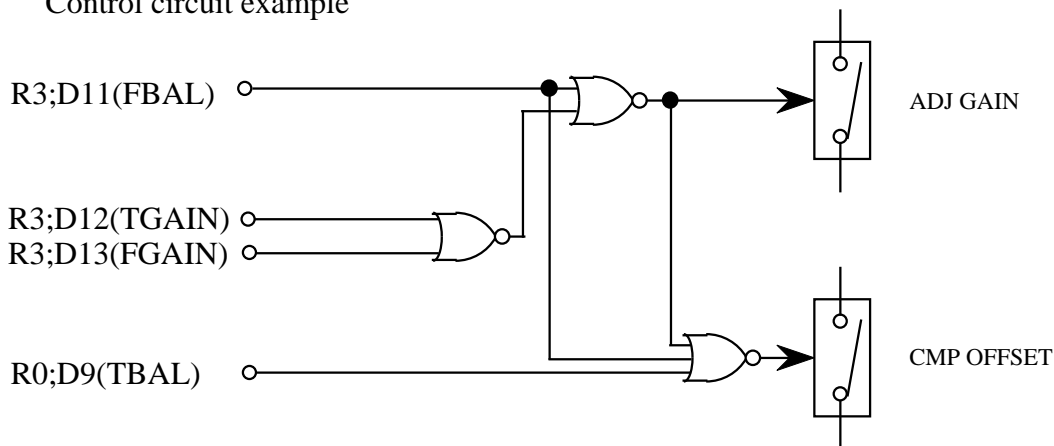
• TBAL (R0; D9)

Control bit		Remark
R0; D9 TBAL	ADJ TBAL	
0	open	————
1	close	Track Balance adjustment

•FBAL (R3; D11), FGAIN (R3; D13), TGAIN (R3; D12)

Control bit			Switches						Remark
R3; D11 FBAL	R3; D13 FGAIN	R3; D12 TGAIN	FG SIG	FG RET	TG SIG	TG RET	ADJ GAIN	ADJ FBAL	
0	0	0	open	open	open	open	open	open	————
0	0	1	open	open	close	close	close	open	Track Gain adjustment
0	1	0	close	close	open	open	close	open	Focus Gain adjustment
0	1	1	close	close	close	close	close	open	————
1	0	0	open	open	open	open	open	open	————
1	0	1	open	open	close	close	open	open	————
1	1	0	close	close	open	open	open	close	Focus Balance adjustment
1	1	1	close	close	close	close	open	close	————

Control circuit example



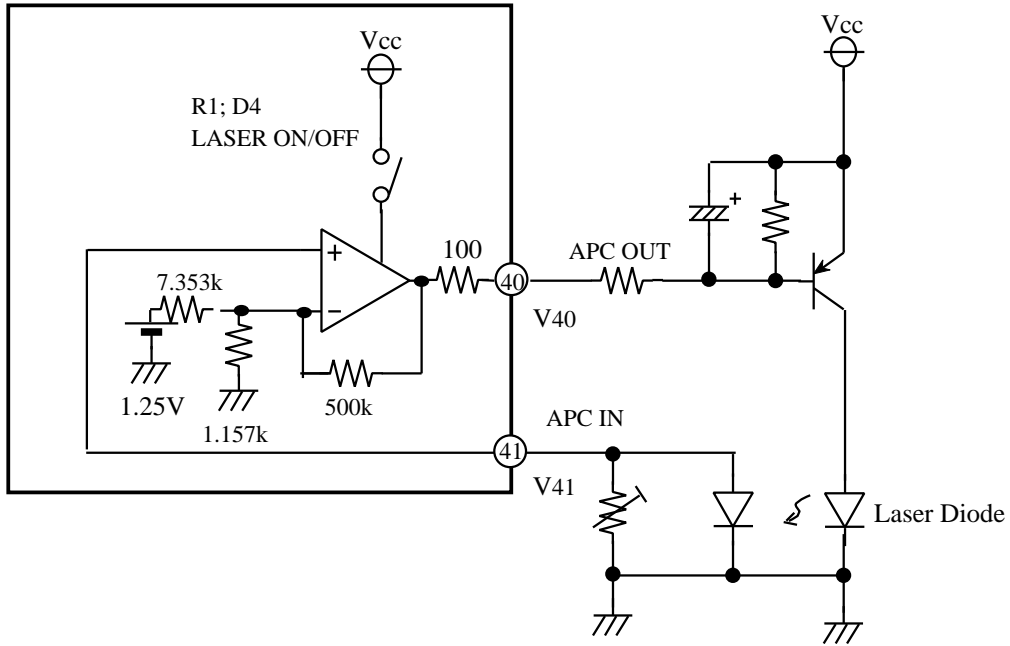
• MLA/DIS pin(23) (Discharge)

MLA/DIS	discharge	Remark
0	close	————
1	open	————

PRELIMINARY
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APC System

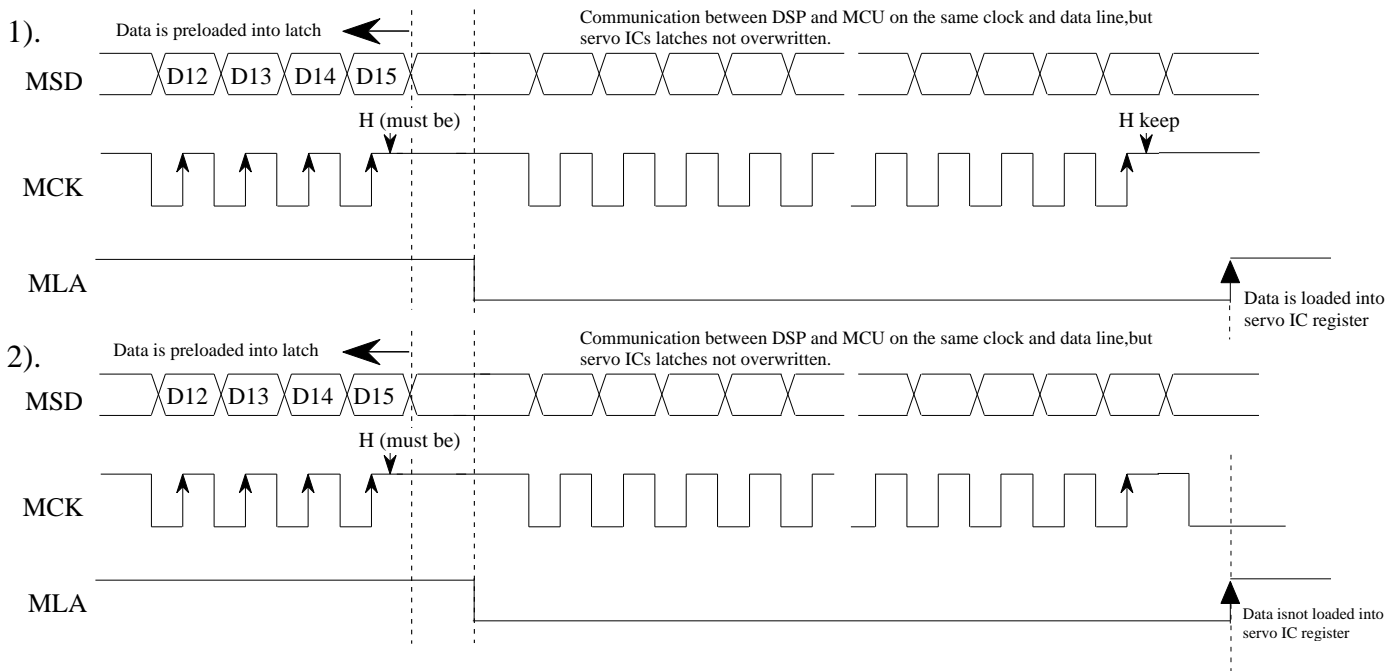
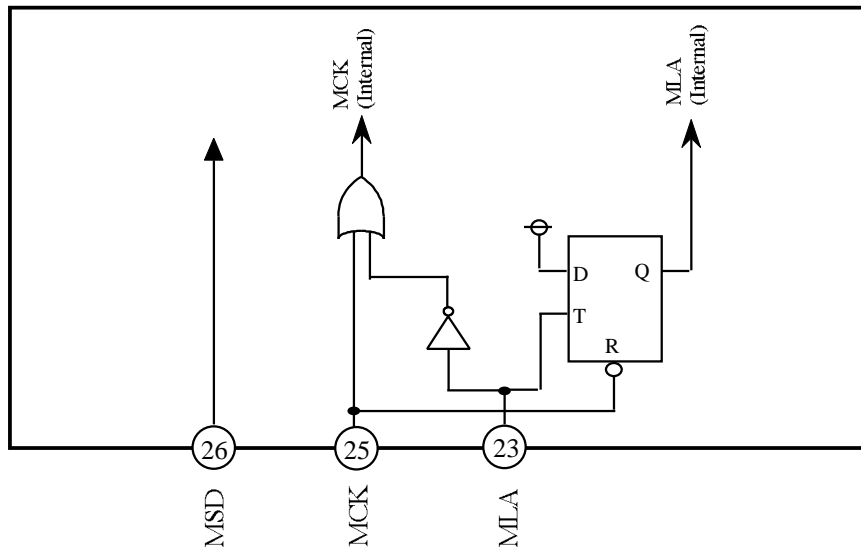


(note1)Resistors and Capacitors without value are externals.

$$(V_{41}=170\text{mV} \rightarrow V_{40}=2.50\text{V})$$

PRELIMINARY
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REGISTER LOADING



Reset Command Condition

Power on reset condition

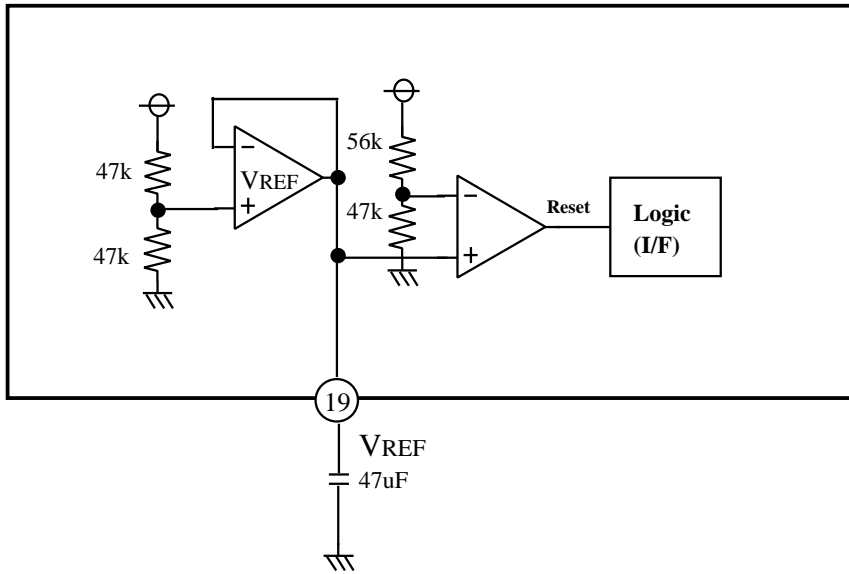
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	—	—	0	0	0	0	0	0	0	1	0	0	0	0	0	0
R1	—	—	0	0	0	0	0	0	1	0	0	0	0	0	0	0
R2	—	—	1	0	0	1	0	0	1	0	0	0	1	0	0	0
R3	—	—	0	0	0	0	0	0	1	0	0	0	1	0	0	0

PRELIMINARY
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Bias amp and Reset

Power on reset



PRELIMINARY
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ADJUSTMENT

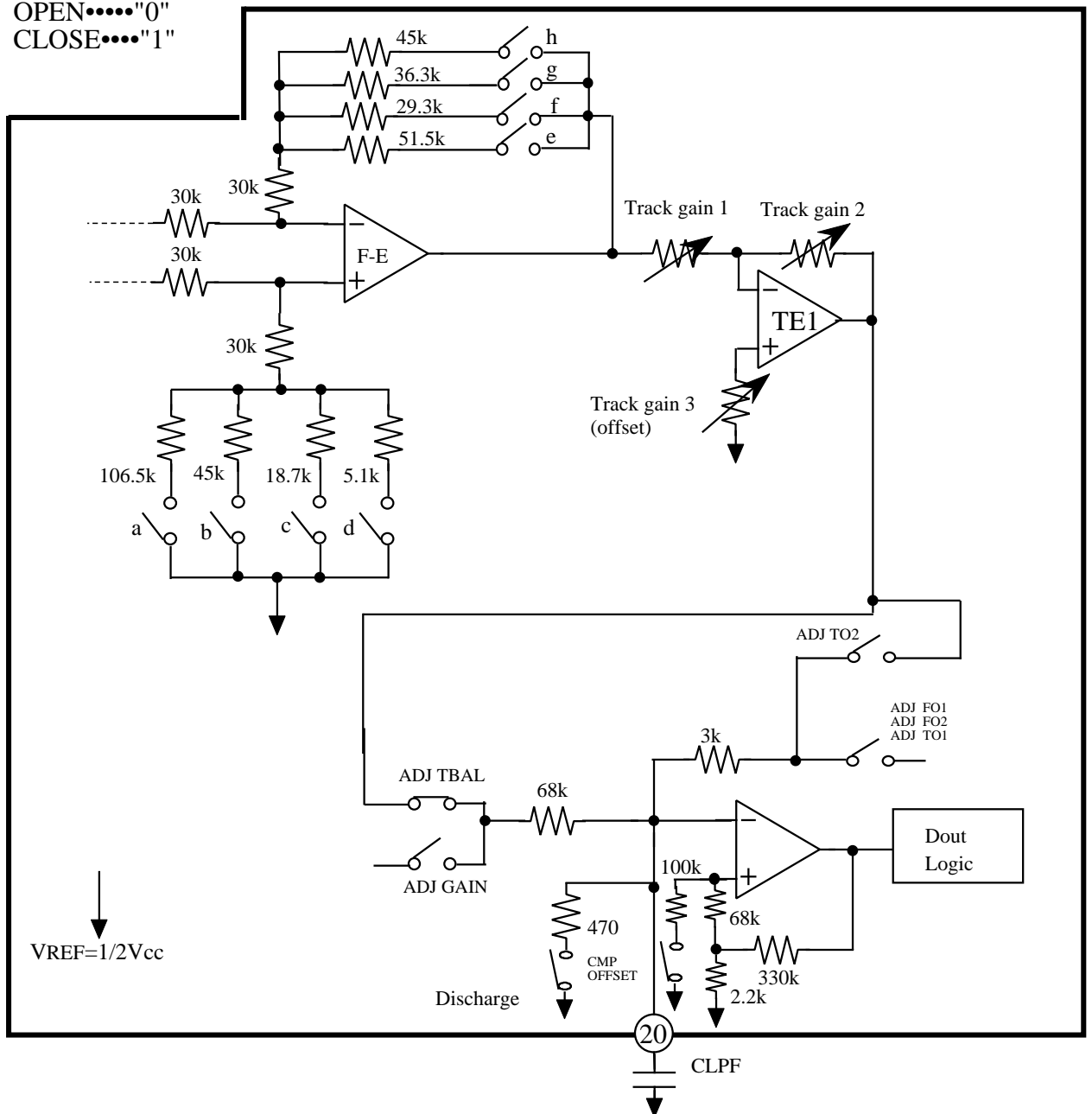
• (1) TRACK BALANCE (16steps , 3.75%step) Recommended Register Settings

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	1	X	0	0	1	X	X	X	X	X	X	X	X	X
R1	0	1	X	X	X	X	X	X	X	X	X	X	0	0	0	0
R2	1	0	X	X	X	X	X	X	D	C	B	A	X	X	X	X
R3	1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X

(note) SW control

OPEN....."0"

CLOSE....."1"



PRELIMINARY
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MITSUBISHI SOUND PROCESSOR LSI

M62481FP

PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

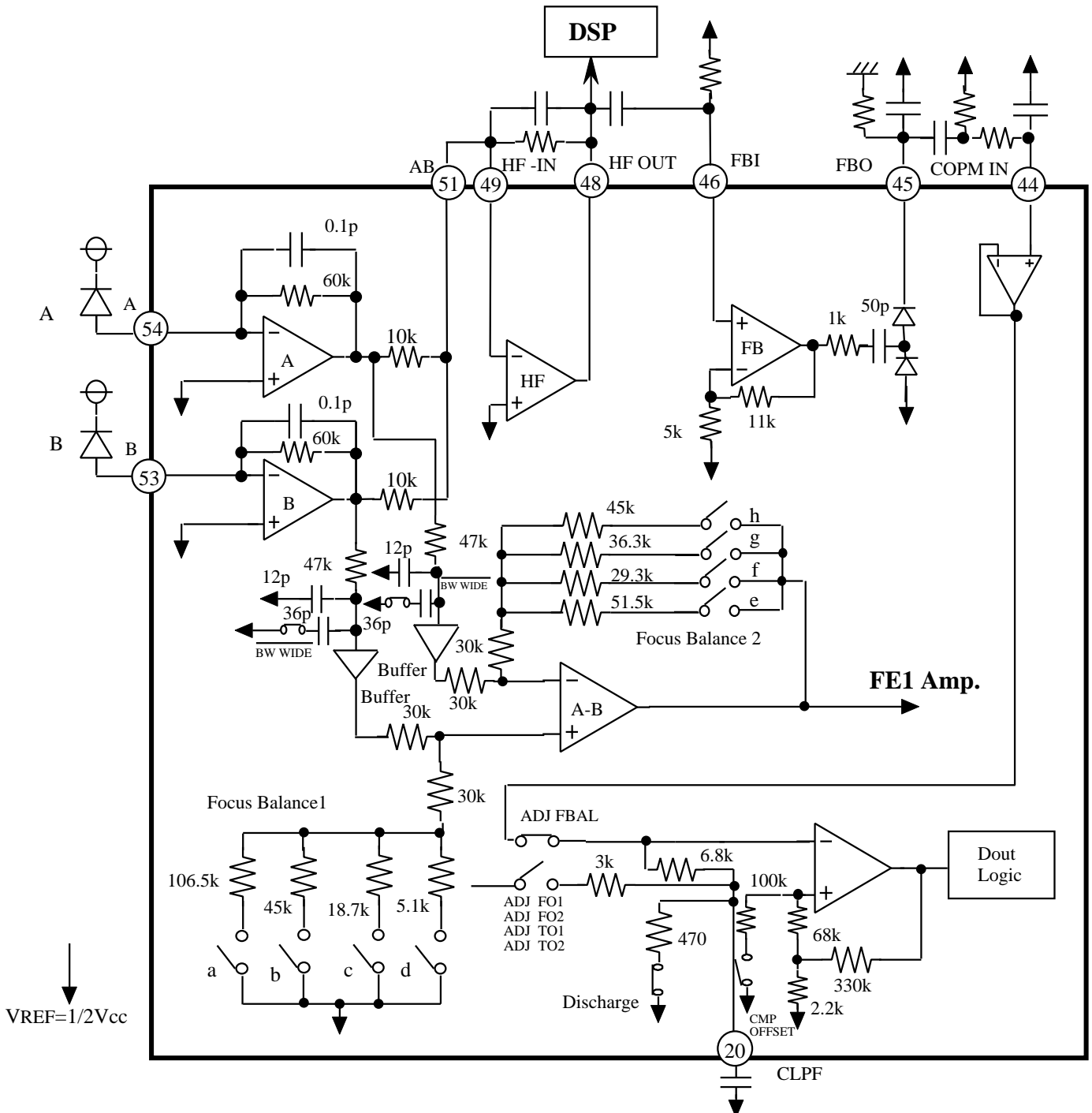
(2) .Track Balance (R2;)

R2;D7	R2;D6	R2;D5	R2;D4	a	b	c	d	e	f	g	h	rate(%)
D	C	B	A									
0	0	0	0	0	0	0	1	0	0	0	1	-31.8
0	0	0	1	0	0	0	1	0	0	1	0	-27.0
0	0	1	0	0	0	0	1	0	1	0	0	-22.4
0	0	1	1	0	0	0	1	1	0	0	1	-18.6
0	1	0	0	0	0	1	0	0	0	0	1	-15.4
0	1	0	1	0	0	1	0	0	0	1	0	-11.3
0	1	1	0	0	0	1	0	0	1	0	0	- 7.2
0	1	1	1	0	0	1	0	1	0	0	1	- 3.9
1	0	0	0	0	1	0	0	0	0	0	1	0
1	0	0	1	0	1	0	0	0	0	1	0	3.6
1	0	1	0	0	1	0	0	0	1	0	0	7.1
1	0	1	1	0	1	0	0	1	0	0	1	9.5
1	1	0	0	0	1	0	0	0	1	1	0	15.1
1	1	0	1	1	0	0	0	0	1	0	0	19.5
1	1	1	0	1	0	0	0	1	0	0	1	21.9
1	1	1	1	1	0	0	0	0	1	1	0	26.4

PRELIMINARY
 Notice ; This is not a final specification.
 some parametric limits are subject to change.

•FOCUS BALANCE (16steps) Recommended Register Settings

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	X	0	0	0	X	X	X	X	X	X	X	X	X
R1	0	1	X	X	X	X	X	X	X	X	X	X	0	0	0	0
R2	1	0	X	X	X	X	X	X	X	X	X	X	D	C	B	A
R3	1	1	1	0	1	X	X	X	X	X	X	X	X	X	X	X



PRELIMINARY
 Notice ; This is not a final specification.
 some parametric limits are subject to change.

(2) .Focus Balance (R2;)

R2;D3	R2;D2	R2;D1	R2;D0	a	b	c	d	e	f	g	h	rate(%)
D	C	B	A									
0	0	0	0	0	0	0	1	0	0	0	1	-31.8
0	0	0	1	0	0	0	1	0	0	1	0	-27.0
0	0	1	0	0	0	0	1	0	1	0	0	-22.4
0	0	1	1	0	0	0	1	1	0	0	1	-18.6
0	1	0	0	0	0	1	0	0	0	0	1	-15.4
0	1	0	1	0	0	1	0	0	0	1	0	-11.3
0	1	1	0	0	0	1	0	0	1	0	0	-7.2
0	1	1	1	0	0	1	0	1	0	0	1	-3.9
1	0	0	0	0	1	0	0	0	0	0	1	0
1	0	0	1	0	1	0	0	0	0	1	0	3.6
1	0	1	0	0	1	0	0	0	1	0	0	7.1
1	0	1	1	0	1	0	0	1	0	0	1	9.5
1	1	0	0	0	1	0	0	0	1	1	0	15.1
1	1	0	1	1	0	0	0	0	1	0	0	19.5
1	1	1	0	1	0	0	0	1	0	0	1	21.9
1	1	1	1	1	0	0	0	0	1	1	0	26.4

PRELIMINARY
 Notice ; This is not a final specification.
 some parametric limits are subject to change.

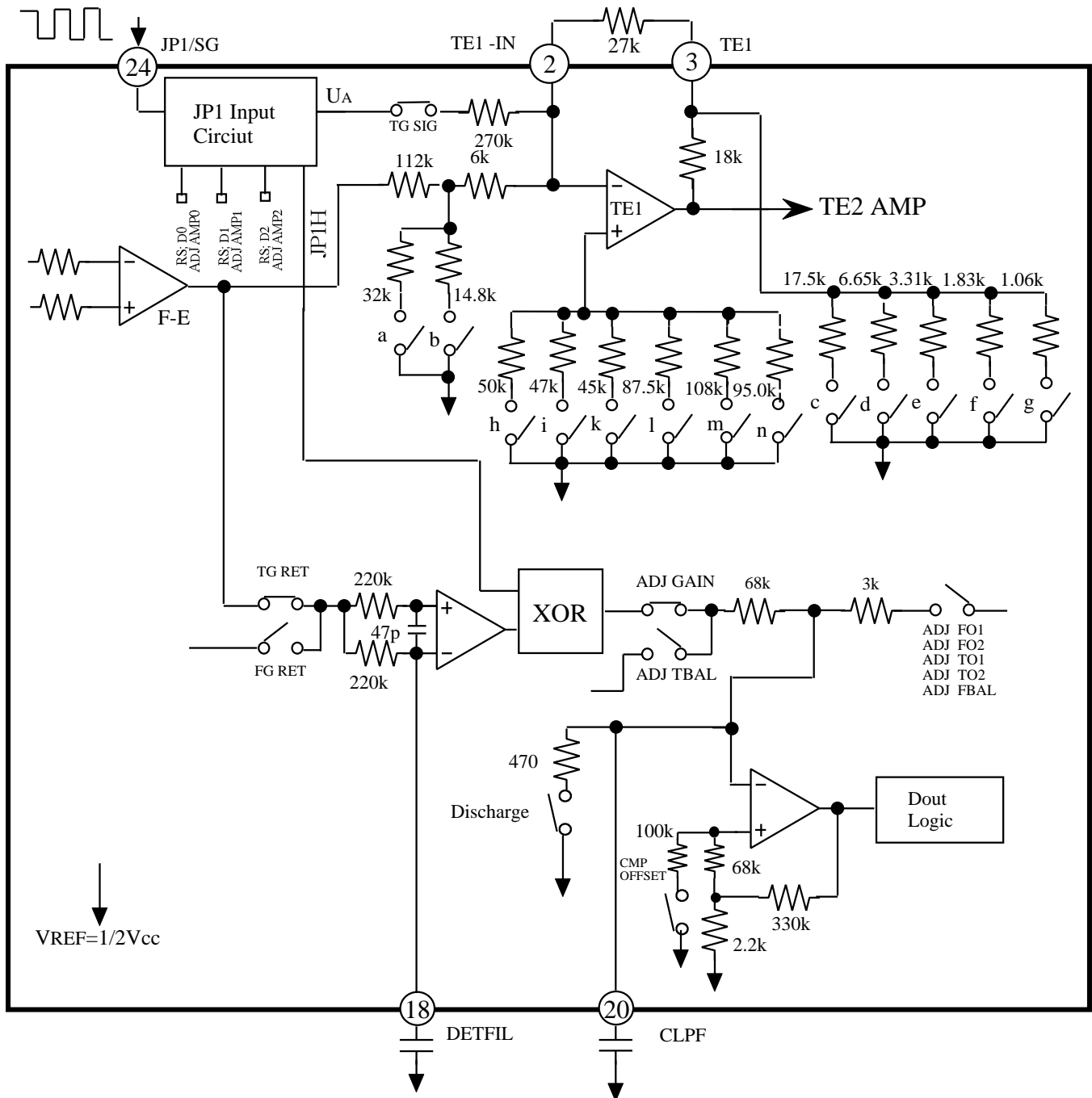
MITSUBISHI SOUND PROCESSOR LSI

M62481FP

PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

•TRACK GAIN (16steps , 1.4dBstep) Recommended Register Settings

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	X	0	0	0	X	X	X	X	X	X	X	X	X
R1	0	1	X	X	X	X	X	X	X	X	X	X	0	0	0	0
R2	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X
R3	1	1	0	1	0	X	X	X	D	C	B	A	X	X	X	X



<Adjustment Method>Set phase shift at 90 deg by reference signal from JP1 (PIN 24)

PRELIMINARY
 Notice ; This is not a final specification.
 some parametric limits are subject to change.

(2) -2.Track Gain

R3;D7	R3;D6	R3;D5	R3;D4	a	b	c	d	e	f	g	gain(dB)
D	C	B	A								
0	0	0	0	0	1	0	0	0	0	0	-11.2
0	0	0	1	1	0	0	0	0	0	0	-9.8
0	0	1	0	0	0	0	0	0	0	0	-8.4
0	0	1	1	0	1	1	0	0	0	0	-7.0
0	1	0	0	1	0	1	0	0	0	0	-5.6
0	1	0	1	0	0	1	0	0	0	0	-4.2
0	1	1	0	0	1	0	1	0	0	0	-2.8
0	1	1	1	1	0	0	1	0	0	0	-1.4
1	0	0	0	0	0	0	1	0	0	0	0
1	0	0	1	0	1	0	0	1	0	0	1.4
1	0	1	0	1	0	0	0	1	0	0	2.8
1	0	1	1	0	0	0	0	1	0	0	4.2
1	1	0	0	0	1	0	0	0	1	0	5.6
1	1	0	1	1	0	0	0	0	1	0	7.0
1	1	1	0	0	0	0	0	0	1	0	8.4
1	1	1	1	0	1	0	0	0	0	1	9.8

R3;D7	R3;D6	R3;D5	R3;D4	h	i	k	l	m	n
D	C	B	A						
0	0	0	0	1	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0
0	0	1	0	0	0	1	0	0	0
0	0	1	1	1	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0
0	1	0	1	0	0	1	0	0	0
0	1	1	0	1	0	0	0	0	0
0	1	1	1	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0
1	0	0	1	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1
1	0	1	1	0	0	0	1	0	0
1	1	0	0	0	0	0	0	1	0
1	1	0	1	0	0	0	0	0	1
1	1	1	0	0	0	0	1	0	0
1	1	1	1	0	0	0	0	1	0

PRELIMINARY
 Notice ; This is not a final specification.
 some parametric limits are subject to change.

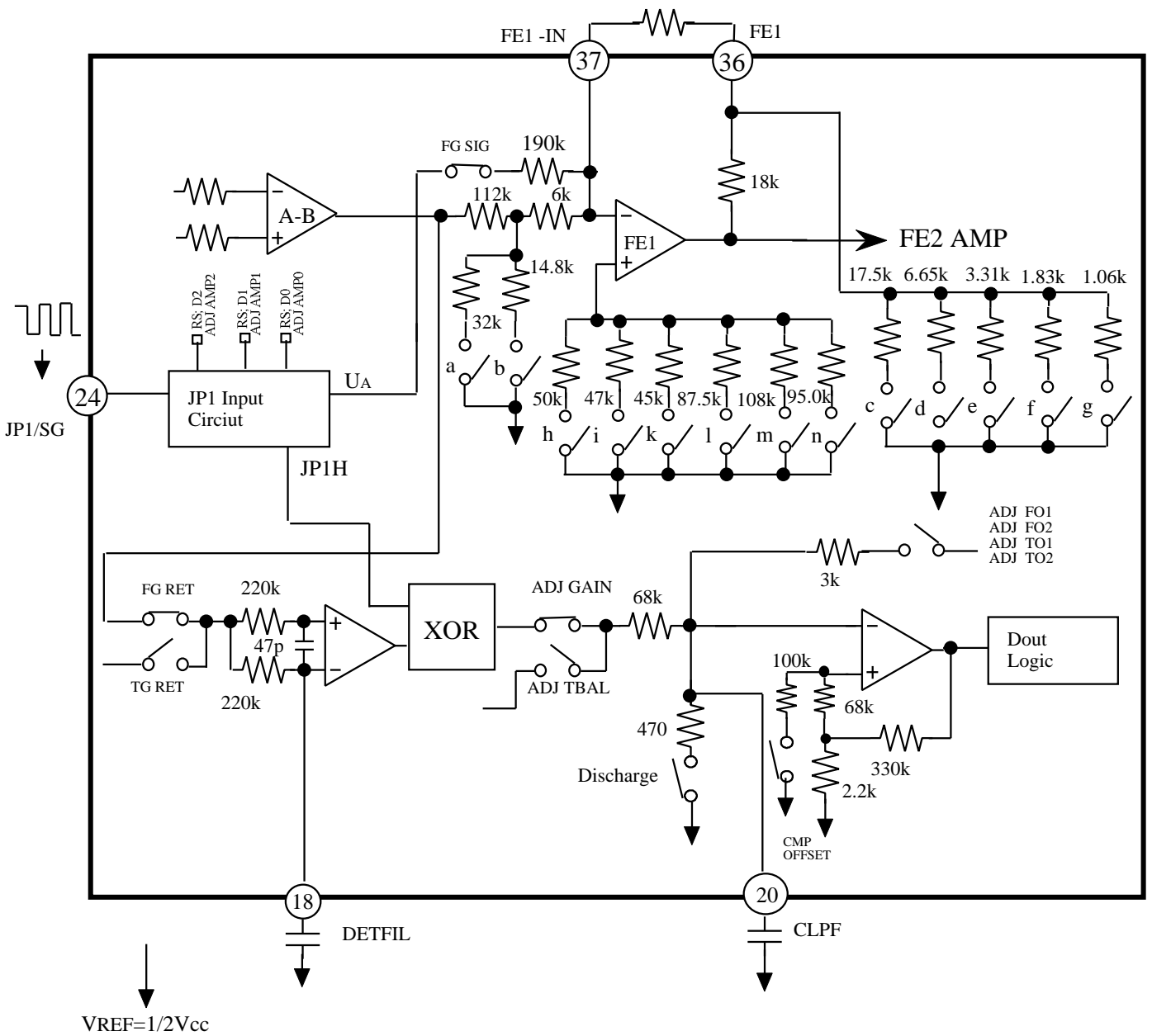
MITSUBISHI SOUND PROCESSOR LSI

M62481FP

PICKUP SERVO SYSTEM WITH AUTOMATIC ADJUSTMENT

•FOCUS GAIN (16steps , 1.4dBstep) Recommended Register Settings

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	X	0	0	0	X	X	X	X	X	X	X	X	X
R1	0	1	X	X	X	X	X	X	X	X	X	X	0	0	0	0
R2	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X
R3	1	1	1	0	0	X	X	X	X	X	X	X	D	C	B	A



<Adjustment Method>Set phase shift at 90deg.by reference signal from JP1 (PIN 24)

PRELIMINARY
 Notice ; This is not a final specification.
 some parametric limits are subject to change.

(2) -2.Focus Gain (R3;)

R3;D3	R3;D2	R3;D1	R3;D0	a	b	c	d	e	f	g	gain(dB)
D	C	B	A								
0	0	0	0	0	1	0	0	0	0	0	-11.2
0	0	0	1	1	0	0	0	0	0	0	-9.8
0	0	1	0	0	0	0	0	0	0	0	-8.4
0	0	1	1	0	1	1	0	0	0	0	-7.0
0	1	0	0	1	0	1	0	0	0	0	-5.6
0	1	0	1	0	0	1	0	0	0	0	-4.2
0	1	1	0	0	1	0	1	0	0	0	-2.8
0	1	1	1	1	0	0	1	0	0	0	-1.4
1	0	0	0	0	0	0	1	0	0	0	0
1	0	0	1	0	1	0	0	1	0	0	1.4
1	0	1	0	1	0	0	0	1	0	0	2.8
1	0	1	1	0	0	0	0	1	0	0	4.2
1	1	0	0	0	1	0	0	0	1	0	5.6
1	1	0	1	1	0	0	0	0	1	0	7.0
1	1	1	0	0	0	0	0	0	1	0	8.4
1	1	1	1	0	1	0	0	0	0	1	9.8

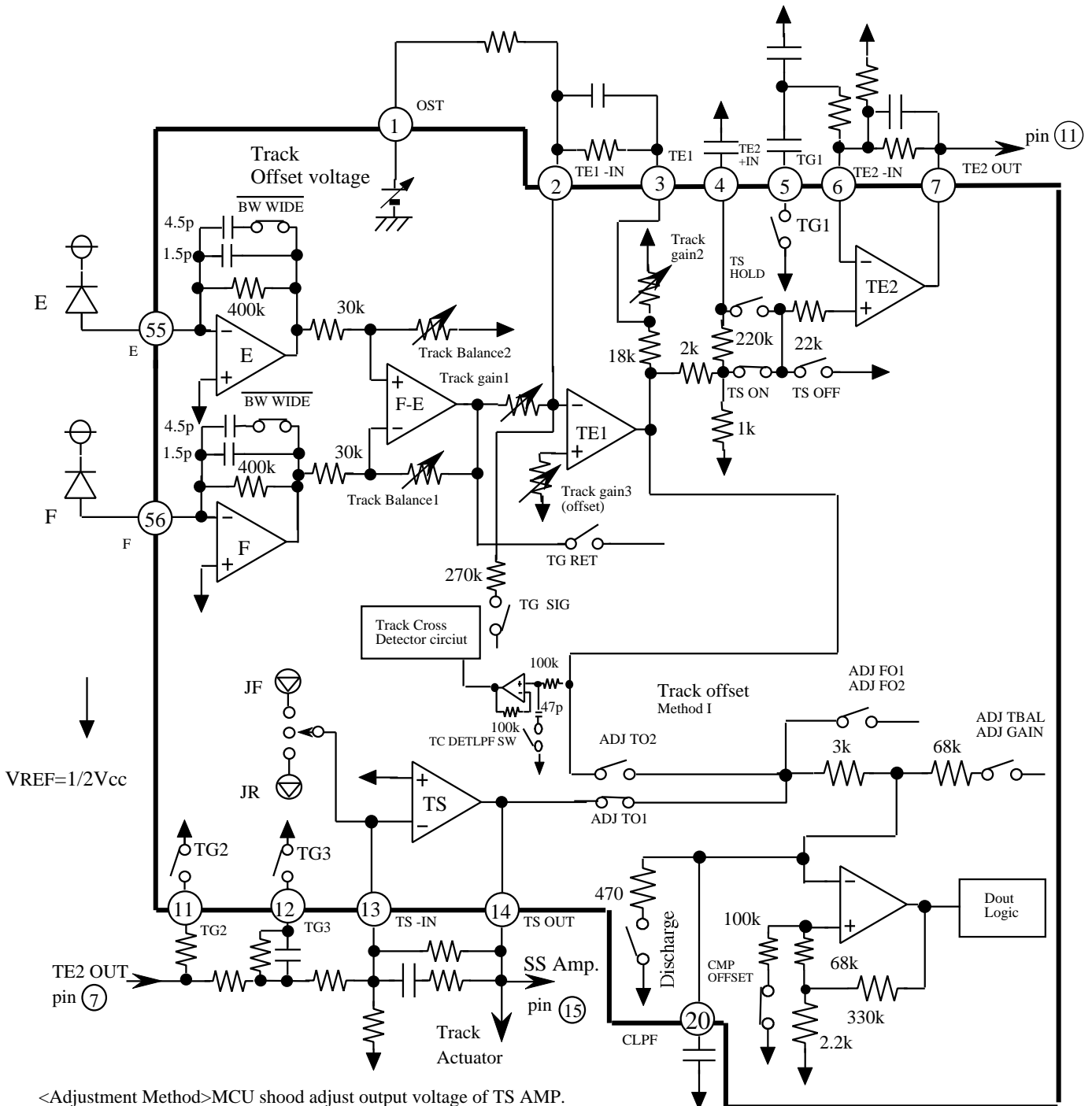
R3;D3	R3;D2	R3;D1	R3;D0	h	i	k	l	m	n
D	C	B	A						
0	0	0	0	1	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0
0	0	1	0	0	0	1	0	0	0
0	0	1	1	1	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0
0	1	0	1	0	0	1	0	0	0
0	1	1	0	1	0	0	0	0	0
0	1	1	1	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0
1	0	0	1	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1
1	0	1	1	0	0	0	1	0	0
1	1	0	0	0	0	0	0	1	0
1	1	0	1	0	0	0	0	0	1
1	1	1	0	0	0	0	1	0	0
1	1	1	1	0	0	0	0	1	0

PRELIMINARY
 Notice ; This is not a final specification.
 some parametric limits are subject to change.

•TRACK OFFSET

(1) Track Offset method I (8steps) Recommended Register Settings

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	X	X	0	0	0	0	X	0	0	0	0	X	X	X
R1	0	1	X	X	X	X	X	X	X	X	X	X	0	0	1	0
R2	1	0	C	B	A	X	X	X	X	X	X	X	X	X	X	X
R3	1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X

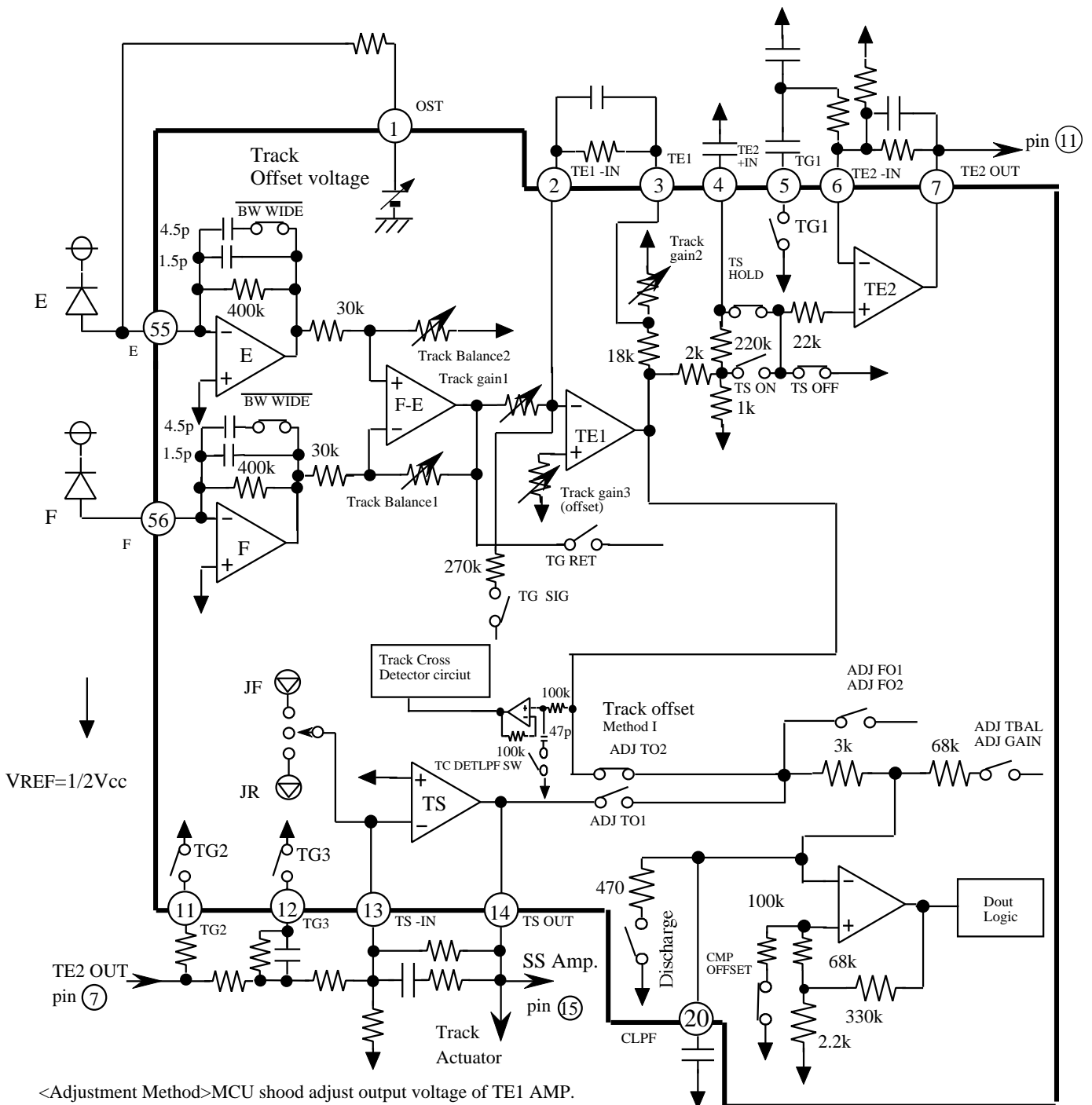


<Adjustment Method>MCU should adjust output voltage of TS AMP.

PRELIMINARY
 Notice ; This is not a final specification.
 some parametric limits are subject to change.

(2) Track Offset method II (8steps) Recommended Register Settings

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	X	X	0	0	0	0	X	1	0	0	0	X	X	X
R1	0	1	X	X	X	X	X	X	X	X	X	X	0	0	0	1
R2	1	0	C	B	A	X	X	X	X	X	X	X	X	X	X	X
R3	1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X

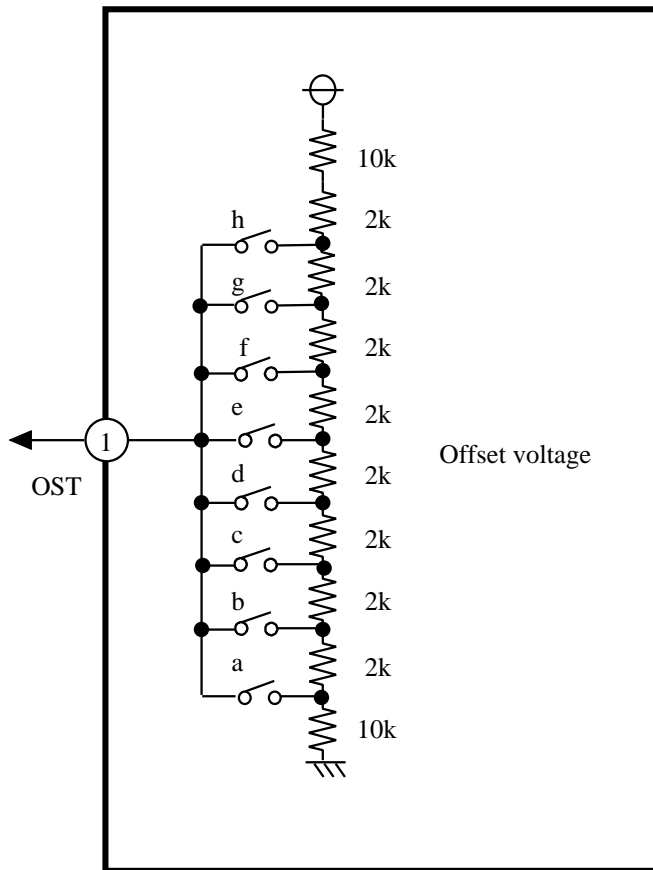


<Adjustment Method> MCU should adjust output voltage of TE1 AMP.

PRELIMINARY
 Notice ; This is not a final specification.
 some parametric limits are subject to change.

-2. Track Offset voltage source (R2;)

R2;D13	R2;D12	R2;D11	a	b	c	d	e	f	g	h	Voltage(V)
C	B	A									
0	0	0	1	0	0	0	0	0	0	0	1.39
0	0	1	0	1	0	0	0	0	0	0	1.67
0	1	0	0	0	1	0	0	0	0	0	1.94
0	1	1	0	0	0	1	0	0	0	0	2.22
1	0	0	0	0	0	0	1	0	0	0	2.50
1	0	1	0	0	0	0	0	1	0	0	2.78
1	1	0	0	0	0	0	0	0	1	0	3.06
1	1	1	0	0	0	0	0	0	0	1	3.33

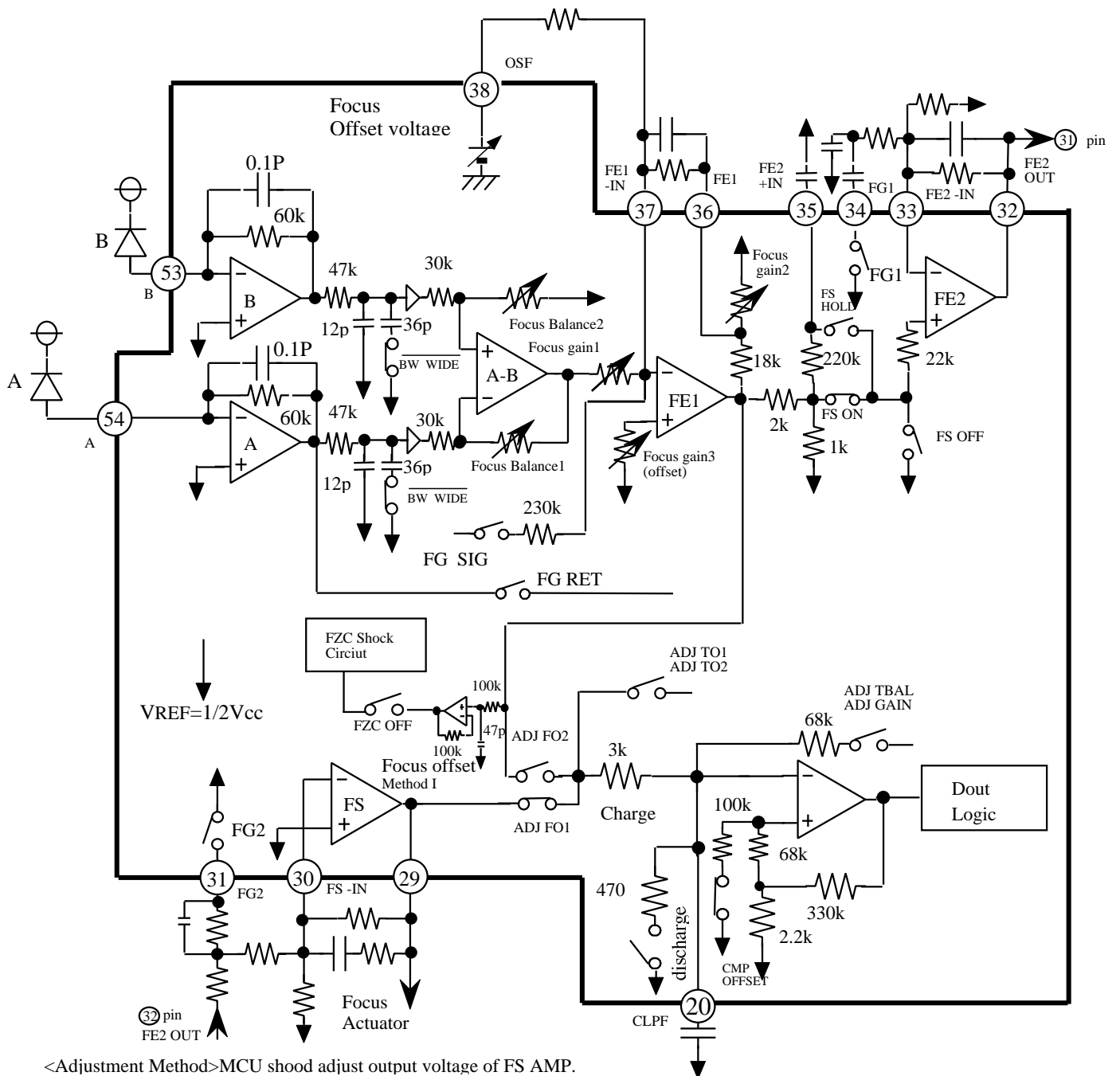


PRELIMINARY
 Notice ; This is not a final specification.
 some parametric limits are subject to change.

•FOCUS OFFSET

(1) Focus Offset method I (8steps) Recommended Register Settings

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	X	X	0	0	0	0	X	X	X	X	X	X	X	X
R1	0	1	X	X	X	X	X	X	0	1	1	X	1	0	0	0
R2	1	0	X	X	X	C	B	A	X	X	X	X	X	X	X	X
R3	1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X



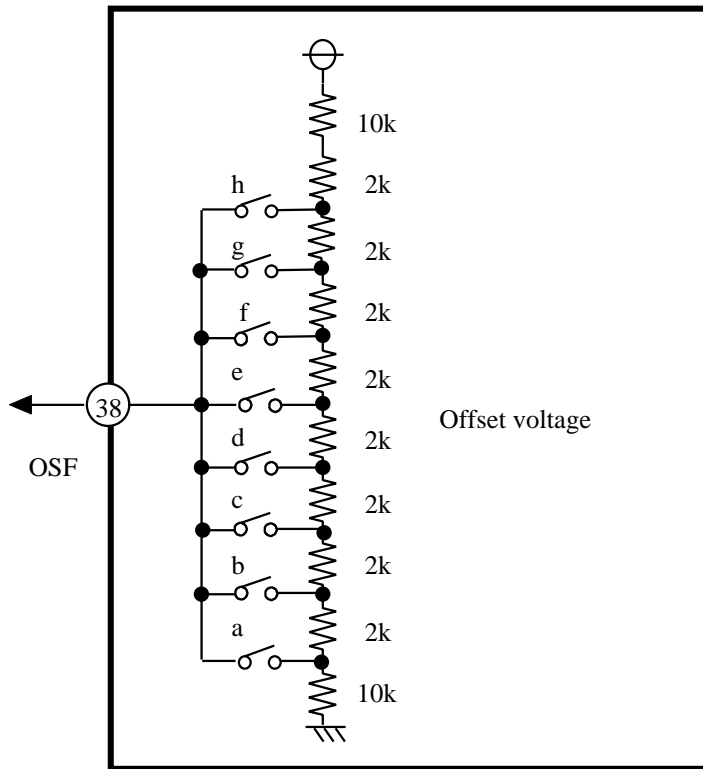
<Adjustment Method>MCU should adjust output voltage of FS AMP.

PRELIMINARY
 Notice ; This is not a final specification.
 some parametric limits are subject to change.

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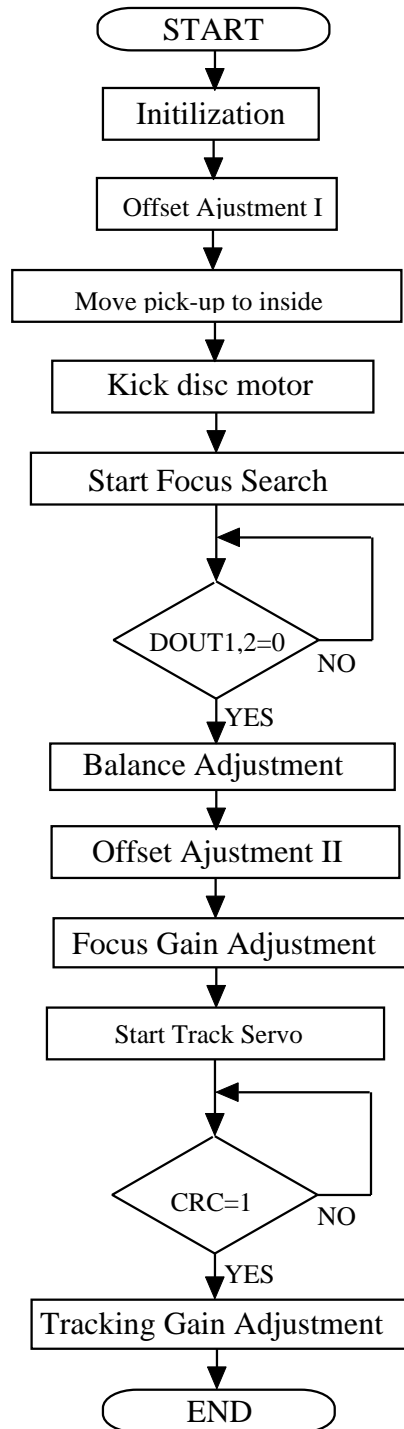
(2) -2. Focus Offset voltage source (R2;)

R2;D10 C	R2;D9 B	R2;D8 A	a	b	c	d	e	f	g	h	Voltage(V)
0	0	0	1	0	0	0	0	0	0	0	1.39
0	0	1	0	1	0	0	0	0	0	0	1.67
0	1	0	0	0	1	0	0	0	0	0	1.94
0	1	1	0	0	0	1	0	0	0	0	2.22
1	0	0	0	0	0	0	1	0	0	0	2.50
1	0	1	0	0	0	0	0	1	0	0	2.78
1	1	0	0	0	0	0	0	0	1	0	3.06
1	1	1	0	0	0	0	0	0	0	1	3.33



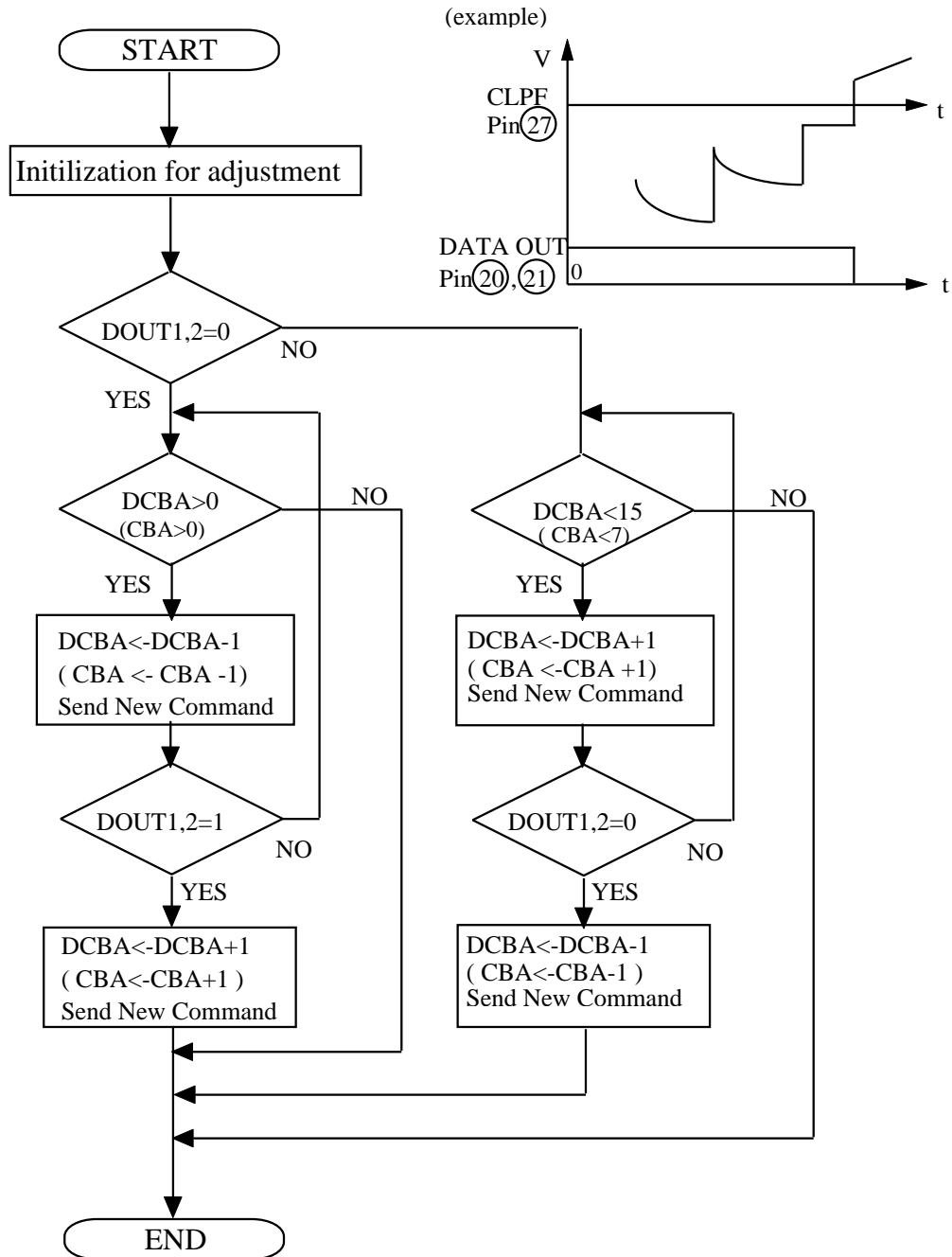
FLOW CHART OF AUTOMATIC ADJUSTMENT

(1)Basic Routine



(2)Automatic Adjustment

Serial Data Command:DCBA(the adjustment item)



(note)It's possible to control the tracking balance by (DCBA(CBA))

APPLICATION NOTE

Phase shift circuit for auto adjustment

The adjustment frequency for the auto adjustment is the frequency where the phase shift for the comparator is 90. When the phase characteristic is smooth around that adjustment frequency (figure 1). The standard circuit for the feed-in of the adjustment frequency can be used (figure 3).

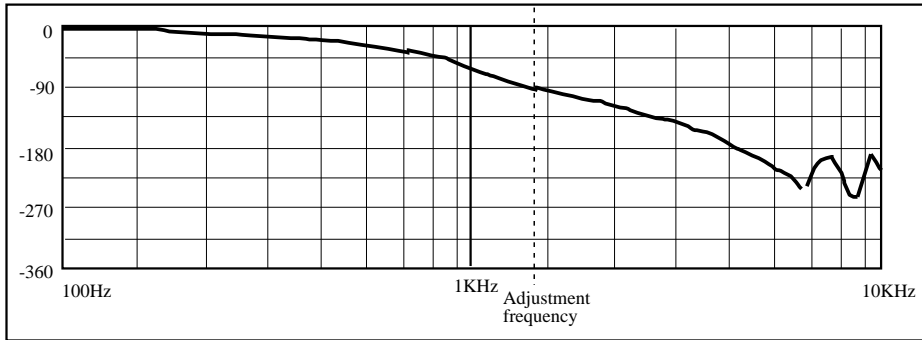


Figure 1: Phase Diagram of Pick Up + Servo

Some pick up units may have a phase turbulence around the ideal adjustment frequency. So the phase diagram may look like that in figure 2. Those phase turbulence can cause miss adjustment.

It is necessary to overcome this effect by the adjustment software.

E.g.:The adjustment frequency is shifted to a lower or a higher frequency , which results in a systematic misadjustment.This systematic misadjustment must then be taken into account by the adjustment software.

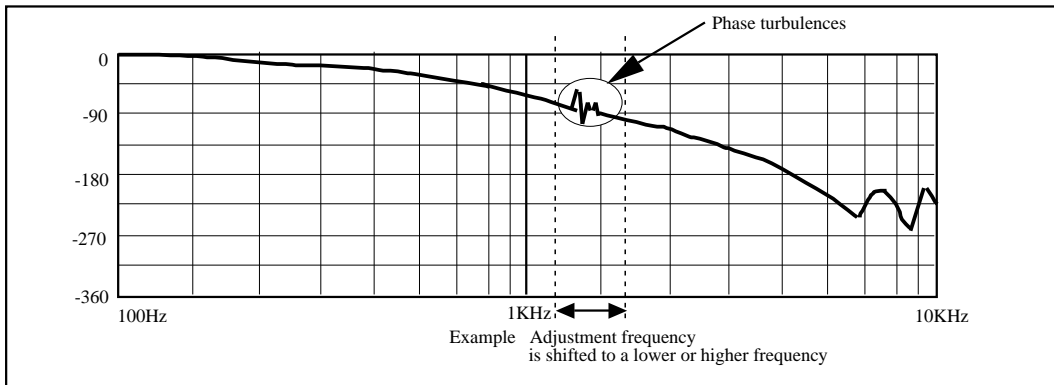


Figure 2: Phase Diagram of Pick Up + Servo with phase turbulence

Below figure shows the feed-in circuit in the track servo.

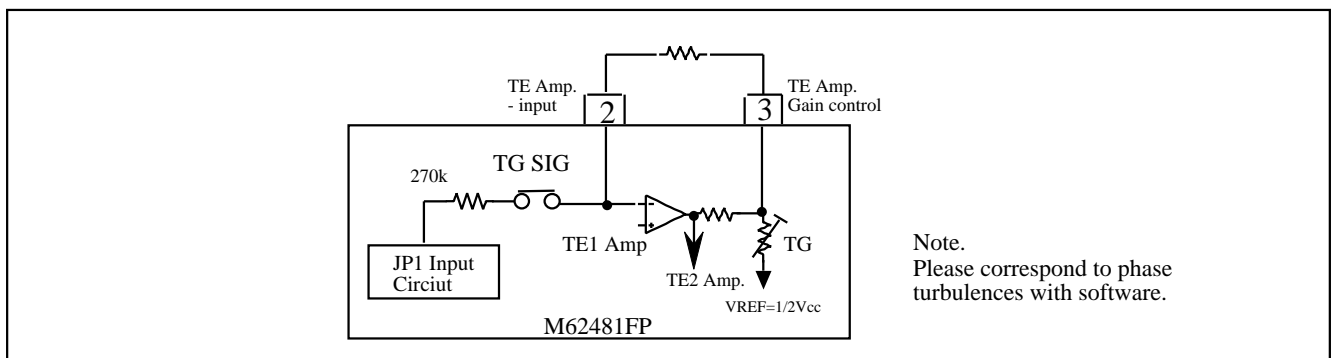


Figure 3: Circuit Examples