GT-48006A

Low Cost Two Port 10/100 Ethernet Bridge/Switch Controller

Galileo TECHNOLOGY

FEATURES

- Single-chip, low-cost, two port 10/100Mbps Ethernet bridge/switch
  - Provides packet switching functions between two 10/100Mbps, auto-negotiated on-chip Fast Ethernet ports
  - Ideal for dual speed repeater and 2-port bridge applications
- Incorporates two 802.3 compliant 10/100Mbps Media Access Controllers
  - Direct Interface to MII (Media Independent Interface)
  - Half/Full Duplex Support (up to 200 Mbps/port)
  - IEEE 802.3 100Base-TX, T4, and FX compatible
  - Support for backpressure in half-duplex mode
- Auto-negotiation supported through MII Interface
  - Can be disabled on a per-port basis
- High-Performance Switching Engine
  - Performs forwarding and filtering at full wire speed
  - 148,800 packets/sec on each Ethernet port

- Direct support for packet buffering
  - Glueless interface to 1or 2Mbyte of 50ns EDO DRAM
  - Up to 1K buffers, 1536-bytes each
  - Dynamic or fixed buffer allocation for each port
- Supports 'Store and Forward' switching approach
  - Low last-bit in to first-bit out delay
  - Provides packet buffering in overloaded networks
- High visibility LED interface
  - 3 pin serial LED interface for detailed status information per port
- Advanced address recognition
  - Intelligent address recognition mechanism enables forwarding rate at full wire speed
  - Self-learning mechanism
  - Supports up to 16K Unicast addresses and unlimited Multicast/Broadcast addresses
- Low-power 0.5u 3.3V process (5V tolerant)
- 100 pin PQFP package
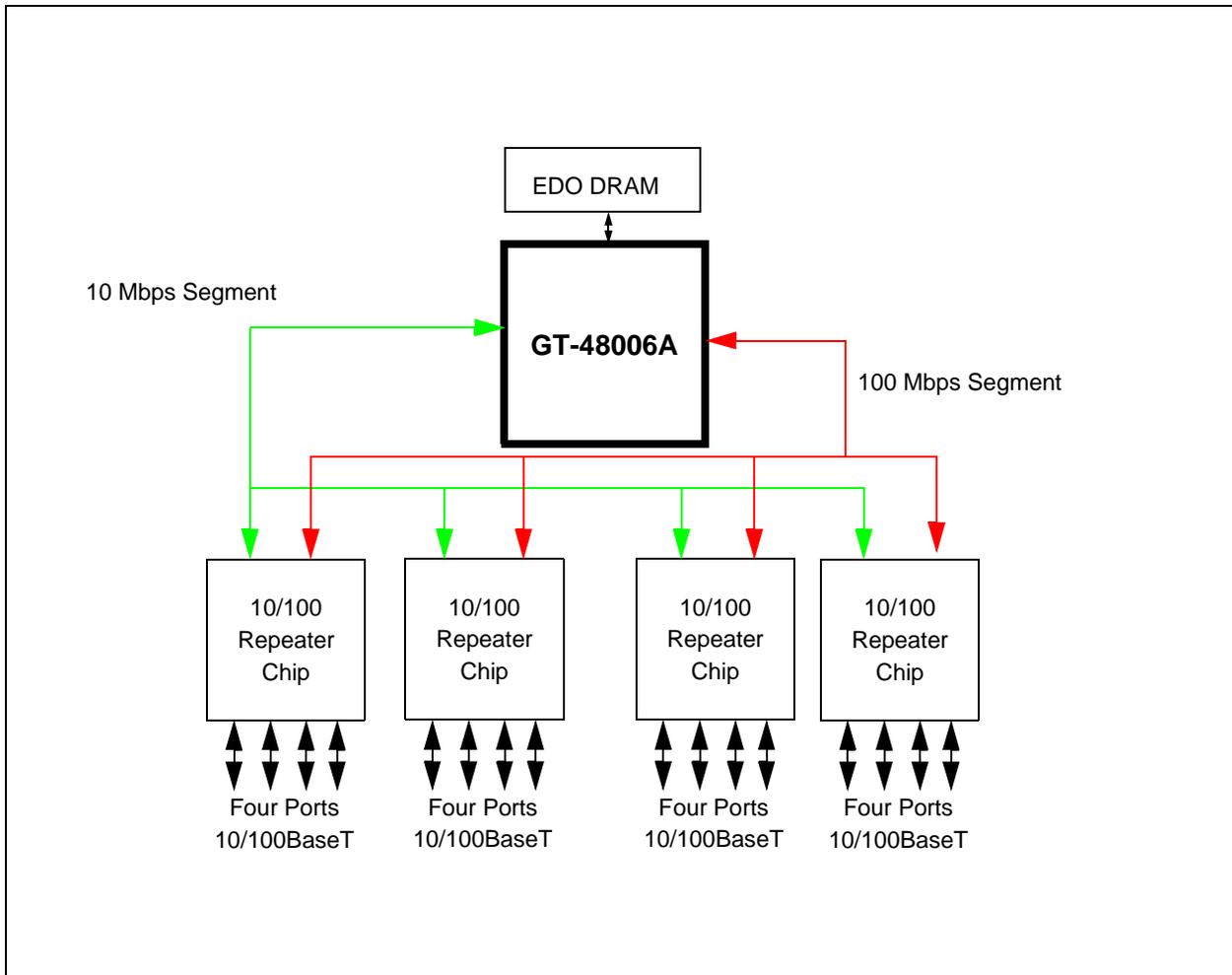
1. Functional Overview

The GT-48006A is a high-performance/low-cost, two-port 10/100Mbps Ethernet bridge/switch that provides packet switching/bridging functions between two on-chip 10/100Mbps auto-negotiated ports. The GT-48006A is intended for applications that need to bridge between two 10/100BaseX collision domains, such as:

- Autonegotiating "dual speed" 10/100 repeaters
- Unmanaged 10/100 bridges
- Fiber to 100BaseTX media converters

The GT-48006A provides no network management functions (other than LEDs). OEMs requiring management should consider the GT-48002A and GT-48004A 100BaseTX switches, or Galileo's Galaxy**™** Family of low-cost desktop switching components (the GT-48212 and GT-48208.)

1.1 Fast Ethernet Ports

The GT-48006A integrates two Fast Ethernet ports each capable of operation at 10/100Mbps (half-duplex) or 20/200Mbps (full-duplex). Two Media Independent Interfaces (MII) are provided for glueless connection to off-the-shelf PHY chips. The GT-48006A supports full auto-negotiation for capable PHYs. The speed (10 or 100 Mbps) and duplex (half or full) to which the PHY resolves to operate is automatically reported to the GT-48006A. The port can also be forced to operate in a specific duplex mode, if so desired. Each port includes the Media Access Control function (MAC); the serial LED and MDC/MDIO interface is shared between the ports.

The Fast Ethernet ports support backpressure in half-duplex mode. When backpressure is enabled, and there is no receive buffer available for incoming traffic, the GT-48006A will force a JAM pattern on the receiving port.

1.2 Address Recognition

The GT-48006A can recognize up to 16,000 different Unicast MAC addresses and unlimited Multicast/Broadcast MAC addresses. An intelligent address recognition mechanism enables filtering and forwarding packets at full Fast Ethernet wire speed.
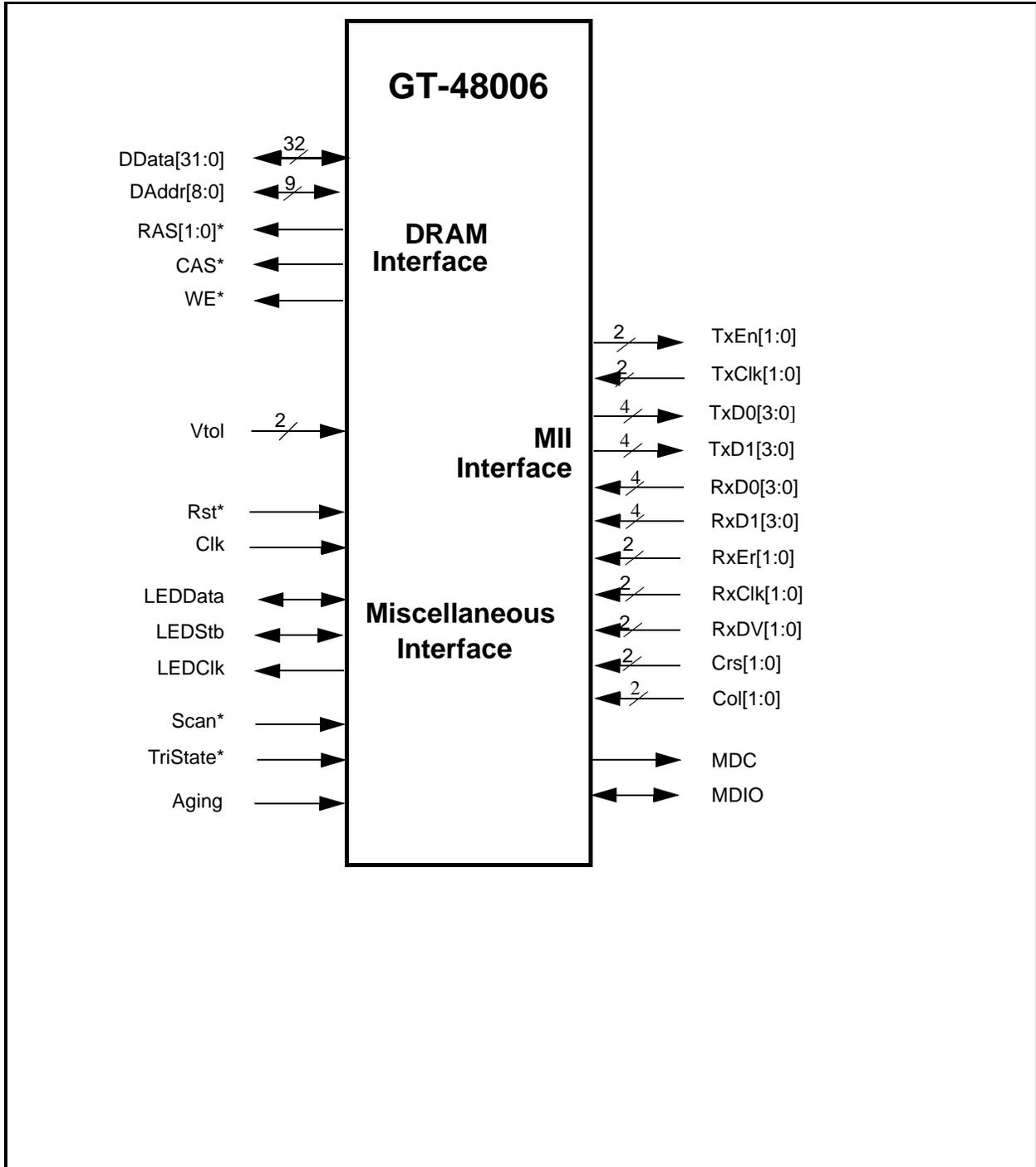
1.3 DRAM Interface

GT-48006A interfaces directly to 1Mbyte or 2Mbyte of EDO DRAM. The DRAM is used to store the incoming/outgoing packets as well as the address table and other device data structures. The interface to EDO DRAM is glueless; all signals needed to control EDO devices are provided.

1.4 Packet Buffers

Incoming packets are buffered in the DRAM array. These buffers provide elastic storage for transferring data between low-speed and high-speed segments. The packet buffers are managed automatically by the GT-48006A.

2. Pin Information

2.1 Logic Symbol

3. Pin Functions and Assignment

Symbol	Type	Description
Clock and Reset		
Rst*	I	**RESET:** Active LOW. Rst* must be asserted for at least 10 clock cycles when in the reset state. Following Rst* deassertion, the GT-48006A clears the internal buffers and initializes the address table in the DRAM. The address table initialization takes 165,000 CLK cycles to complete. Any incoming packets during address table initialization are ignored.
Clk	I	**Clock:** Provides the timing for the GT-48006A internal units. All functional units except for the serial interfaces use this clock. The clock frequency is 40MHz. THIS INPUT IS NOT 5V TOLERANT.
DRAM Interface		
DData[31:0]	I/O	**DRAM Data:** 32-bit EDO DRAM data bus. These signals connect directly to the data input/output pins of the DRAM devices.
DAddr[8:0]	I/O	**DRAM Multiplexed Address Bus:** In normal operation, DAddr[8:0] contain the DRAM multiplexed row/column address. During RESET, these multiplexed pins are sampled by the GT-48006A to indicate various parameters as follows: DAddr[0] - Autonegotiation enable for port 0 DAddr[1] - Autonegotiation enable for port 1 DAddr[2] - Skip Init DAddr[3] - Limit4 DAddr[4] - VL Tag Enable passing DAddr[5] - DRAM size DAddr[6] - Full Duplex for port 0 DAddr[7] - Full Duplex for port 0 DAddr[8] - Back Pressure enable
RAS[1:0]*	O	**Row Address Strobes:** DRAM row address strobes. For the two banks.
CAS*	O	**Column Address Strobe:** DRAM column address strobe. The GT-48006A always accesses 32-bit values and does not require a separate CAS* for each byte.
WE*	O	**Write Enable:** DRAM write enable.
Media Independent Interface		
TxEn[1:0]	O	**Transmit Enable:** Active HIGH. This output indicates that the packet is being transmitted. TxEn is synchronous to TxClk.
TxClk[1:0]	I	**Transmit Clock:** Provides the timing reference for the transfer of TxEn, TxD signals. TxClk frequency is one fourth of the data rate (25 MHz for 100Mbps, 2.5 MHz for 10Mbps). TxClk nominal frequency should match the nominal frequency of RxClk for the same port.
TxD0[3:0]	O	**Transmit Data 0:** Outputs the Port0 Transmit Data. Synchronous to TxClk[0].
TxD1[3:0]	O	**Transmit Data 1:** Outputs the Port1 Transmit Data. Synchronous to TxClk[1].
Col[1:0]	I	**Collision detect:** Active HIGH. Indicates a collision has been detected on the wire. This input is ignored in full-duplex mode. Col is not synchronous to any clock.
RxD0[3:0]	I	**Receive Data 0:** Port 0 Receive Data. Synchronous to RxClk[0].
RxD1[3:0]	I	**Receive Data 1:** Port 1 Receive Data. Synchronous to RxClk[1].

Symbol	Type	Description
RxEr[1:0]	I	**Receive Error**. Active HIGH. Indicates that an error was detected in the received frame. This input is ignored when RxDV for the same port is inactive.
RxClK[1:0]	I	**Receive Clock**. Provides the timing reference for the transfer of the RxDV, RxD, RxEr signals (per port). Operates at either 25 MHz (100Mbps) or 2.5 MHz (10Mbps). The nominal frequency of RxClk (per port) should match the nominal frequency of that port's TxClk.
RxDV[1:0]	I	**Receive Data Valid:** Active HIGH. Indicates that valid data is present on the RxD lines. Synchronous to RxClk.
CrS[1:0]	I	**Carrier Sense:** Active HIGH. Indicates that either the transmit or receive medium is non-idle. CrS is not synchronous to any clock.
MDC	O	**Management Data Clock:** Provides the timing reference for the transfer of the MDIO signal. This output may be connected to the PHY devices of both ports.
MDIO	I/O	**Management Data Input/Output:** This bidirectional line is used to transfer control information and status between the PHY and the GT-48006A. It conforms with IEEE Std 802.3u. This signal may be connected to the PHY devices of both ports. When not in use this pin must be connected to a pull-down resistor.
Miscellaneous Interface Pins		
LEDData	I/O	**LED Data/DisBufThr:** In normal configuration carries the serial data bit stream which contains the LED indicators per port. The data is shifted out using the LEDClk. LEDStb is used to mark the first data bit. This pin is active low. During reset, this pin is sampled by the GT-48006A for dynamic/fixed buffering allocation.
LEDStb	I/O	**LED Strobe/Force Link Pass:** In normal operation indicates the beginning (data bit #1) of a valid data frame on LEDData output - active High. During reset, this pin is sampled by the GT-48006A to Force the link to pass.
LEDClk	O	**LED Clock:** 1 MHz clock. This output is used to clock the LEDStb and LEDData outputs. During RESET, LEDClk frequency is 40 MHz.
Scan*	I	**Scan:** This pin together with TriState* indicate the GT-48006A mode of operation as follows: Scan* · TriState* · Mode 1 · 1 · Normal operation 0 · 1 · Factory test mode (reserved) 1 · 0 · The GT-48006A drives all outputs and I/O pins to high impedance. 0 · 0 · Factory test mode (reserved) Factory test modes are reserved and are not to be used in-system. Failure to observe this restriction could result in damage to the device.
TriState*	I	**Tri State:** This pin together with Scan* indicate the GT-48006A mode of operation as described above.

The Scan*/TriState* sub-table:

Scan*	TriState*	Mode
1	1	Normal operation
0	1	Factory test mode (reserved)
1	0	The GT-48006A drives all outputs and I/O pins to high impedance.
0	0	Factory test mode (reserved)

Symbol	Type	Description
Vtol	I	**Input Voltage Tolerance:** These pins are connected to the 5V supply to support 5V tolerance on GT-48006A I/Os. For pure 3.3V operation connect these pins to the 3.3V supply.
Aging	I	**Aging Control:** Active LOW. This pin enables/disables automatic address aging within the GT-48006A.

4. RESET Configuration

The GT-48006A uses several pins as configuration inputs to set certain parameters following a RESET. The definition of the configuration pins changes immediately after RESET to their usual function.

4.1 Configuration Pins

Configuration pins must be pulled up or down externally at RESET to select the desired operational parameter. The recommended value of the pull-up/down resistors is 4.7K ohms. Table 1 on page 7 shows the configuration pins for GT-48006A.

Table 1: RESET Pin Strapping Options

Pin	Configuration Function
DAddr[1:0] 0- 1-	Auto Negotiation Enable for port 1 and 0[1] Enable Disable
DAddr[2]	Skip Init
0- 1-	Skip Initialization on RESET Don't skip initialization
DAddr[3]	Limit4
0- 1-	Disable (standard backoff) Enable
DAddr[4]	VL Tag enable
0- 1-	Enable - Pass up to 1522 bytes packets Disable - Pass up to 1518 bytes packets
DAddr[5]	DRAM Size
0- 1-	2Mbyte 1Mbyte
DAddr[6]	Half/Full Duplex Mode for Port 0
0- 1-	Half Duplex Full Duplex
DAddr[7]	Half/Full Duplex Mode for Port 1
0- 1-	Half Duplex Full Duplex
DAddr[8]	Backpressure
0- 1-	Disable Enable
LEDStb	Force Link Pass
0- 1-	Force Link Status to "link is up" Read Link Status from the PHY via SMI
LEDData	Disable Buffer Threshold
0- 1-	Fixed buffer allocation Dynamic buffer allocation

1. This setting was listed incorrectly in previous revisions of this document. Please check your design and ensure that you have the proper pin strapping option for auto negotiation.

4.2   Configuration Input Timings

The configuration inputs have two timing requirements:
- setup/hold time to clock (as any synchronous input)
- setup of at least 10 clock cycles before RESET de-assertion (rising edge).

These parameters are set by using resistors to strap the configuration pins and delaying RESET de-assertion until least 10 clock cycles after the clock is stable.

5.   Operational Overview

The GT-48006A uses a "store-and-forward" switching approach. Store-and-forward was chosen for the following reasons:

- Store-and-forward switches allow switching between differing speed media (e.g. 10BaseX and 100BaseX.) Such switches require the large elastic buffers that are provided by the EDO DRAM arrays. This is especially true when bridging between a server on a 100Mbps network and clients on a 10Mbps segment.
- Store-and-forward switches improve overall network performance by acting as a "network cache", effectively buffering packets during times of heavy congestion.
- Store-and-forward switches prevent the forwarding of corrupted packets by analyzing the frame check sequence (FCS) before forwarding to the destination port.

5.1   Basic Operation

The basic operation of the GT-48006A is quite simple. The GT-48006A receives incoming packets from one of its ports, searches in the Address Table for the Destination MAC Address and then forwards the packet to the other port, if appropriate.

If the destination address and source address are not found in the other port's address table, the GT-48006A treats the packet as a multicast packet and forwards the packet to the other port.

The GT-48006A automatically learns the port number of attached network devices by examining the Source MAC Address of all incoming packets. If the Source Address is not found in the GT-48006A's Address Table, the device adds it to the table.

5.2   Address Learning

The GT-48006A can learn up to 8K unique MAC addresses. Addresses are stored in the Address Table located in DRAM. The Address Table is managed automatically by the GT-48006A (i.e. new addresses are automatically added to the Address Table). The GT-48006A's address learning process is outlined in Section 6.

5.3   Packet Buffering

The GT-48006A supports up to 1008 full packet size receive buffers. These buffers can be dynamically allocated to the two receive ports or can be optionally limited on a per port basis. When working in dynamic buffer allocation mode, the GT-48006A supports 1008 buffers in 2Mbyte DRAM configuration and 308 buffers in 1Mbyte DRAM configuration. In fixed buffer mode, the GT-48006A supports 140 buffers per port in 1Mbyte DRAM, and 320 buffers per port in the 2Mbyte configuration. Buffer allocation mode is selected via a RESET strapping option as shown in Table 1 on page 7.

5.4   Packet Forwarding

Once an address has been learned, and the packet is buffered, it must be forwarded. The packet forwarding mechanism for the GT-48006A is handled automatically based on the destination address.

5.5   Terminology

It is important to understand the basic terminology used to describe the GT-48006A before getting into a detailed description. Table 2 on page 9 explains the terms used throughout this document.

Table 2: Terminology

Term	Definition
Address Table	The Address Table is a data structure in the GT-48006A's DRAM that contains all learned MAC addresses, and routing information associated with those addresses.
Source Address	The Source Address (SA) is the MAC address from which a received packet was sent.

Table 2: Terminology

Term	Definition
Destination Address	The Destination Address (DA) is the MAC address to which a received packet was sent.
Port Number	Each Ethernet port on the GT-48006 has an associated port number. The GT-48006A associates Port Numbers with the MAC addresses located on those ports.

6.   MAC Address Learning Process

The GT-48006A has a self-learning mechanism for learning the MAC addresses of attached Ethernet devices in real time. The GT-48006A searches for the Source Address (SA) of an incoming packet in the Address Table and acts as follows:

If the SA was not found in the Address Table (a new address), the GT-48006A waits until the end of the packet (non errored packet) and updates the Address Table.

6.1   Address Recognition

The GT-48006A forwards the incoming packets between bridge ports according to Destination Address (DA) as follows:

1.   If the DA is a Unicast address and the address was found in the Address Table, the GT-48006A acts as follows:
     •   If the Port Number is equal to the Port on which the packet was received, the packet is discarded.
     •   If the Port Number is different, the packet is forwarded across the bridge.

2.   If the DA is a Unicast address and the address was not found (Unknown), the GT-48006A acts as if it the unknown packet is a Multicast packet and forwards across the bridge.

3.   If the DA is a Multicast address, the packet is forwarded across the bridge.

6.2   Address Recognition Failure

It is possible that an address recognition cycle will fail when more than 8K addresses have already been entered into the address table. In the case of an address recognition failure the packet will be treated as unknown and forwarded to all ports.

Address recognition failures are not fatal and do not need to be handled (i.e. designers need not worry about them.)

6.3   Address Aging

Address aging is supported for topology changes such as an address moving from one port to the other. When this happens, the GT-48006A detects the change and updates its address table accordingly. Addresses of stations permanently removed from the network are not aged or removed from the address table. If you wish to age out (remove) these addresses, RESET the GT-48006A. There will be a short interruption of traffic flow, however, this is taken care of by the higher-layer protocols.

Pin 25 is designated to enable or disable the function. In revision prior to the GT48006A, Pin 25 is used as a Vtol input, and must be tied HIGH . In the current part, GT-48006A, tying pin 25 HIGH will disable address aging. Therefore, designs which use versions prior to the GT-48006A must have a stuffing option to tie this pin to ground in order to enable address aging with the GT48006A. See pin descriptions for more information. Future revisions of the GT-48006 will be completely backwards compatible with the current revisions

The aging interval will be fixed at 250 seconds based on a 40MHz clock input, or 300 seconds based on a 33MHz clock input to the GT-48006A. Addresses which have not been seen within the timer period will automatically be removed from the address table.

7.   GT-48006A Buffers and Queues

The GT-48006A incorporates two transmit queues for the 2 Ethernet ports and one common receive buffer area (see Figure 1.) The receive buffers as well as the transmit queues are located in the DRAM along with the Address Table. The GT-48006A data structure components are the following:

- **Receive Buffer** - A common Receive Buffer area for all ports. The buffer is divided into 308 or 1008 blocks (depending on the DRAM size) of 1.5KBytes (1536 bytes) each. Each block contains an entire packet.
- **Rx Empty List** - A list of 308 or 1008 bits. Each bit contains the status of its appropriate receive block in the DRAM (empty or occupied).
- **Tx Descriptors** - A set of 2 transmit descriptor rings. Each ring contains 1024 descriptors. The descriptor size is one 32-bit word and contains the Block Address divided by 0x600 (1.5K), the byte count and the packet type (Multicast or Unicast).
- **Read/Write Pointers** - 2 pairs of pointers to the transmit descriptors.

Figure 1: GT-48006A Buffers and Queues
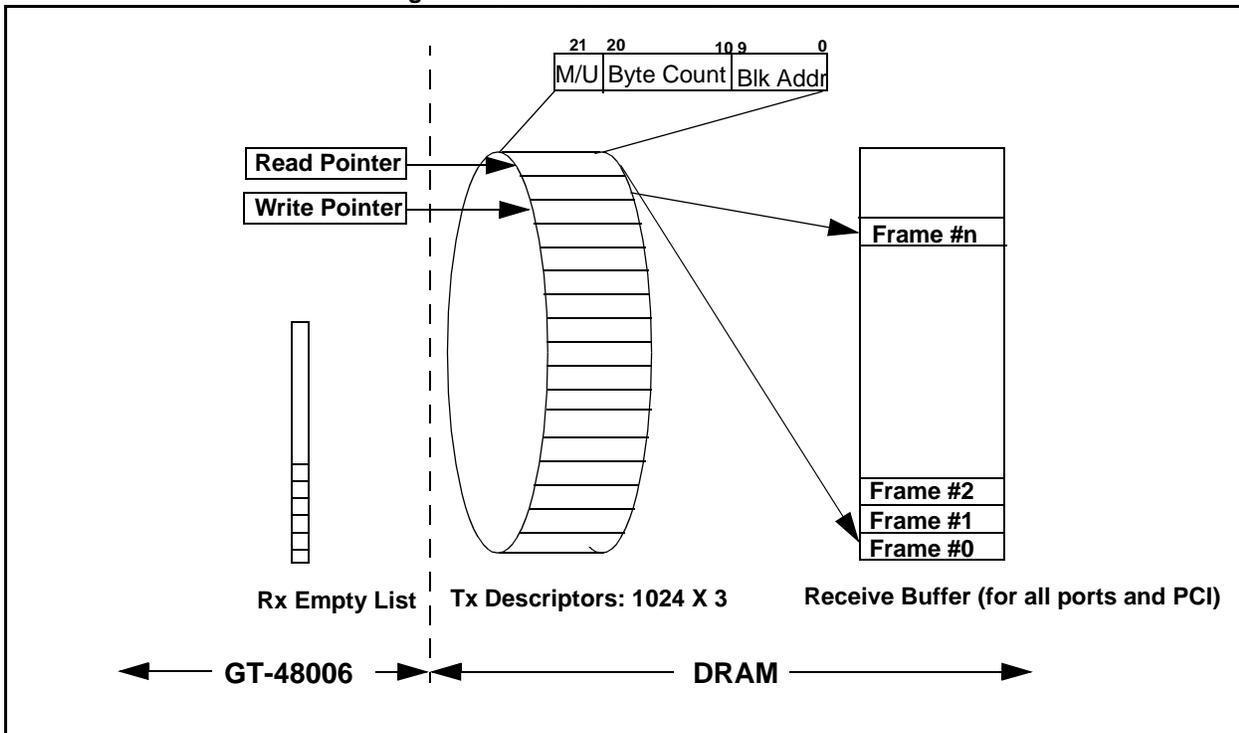
7.1   Rx Buffer Options

There are two modes of operation for the Rx buffers: dynamic buffer allocation and fixed buffer size. Buffer allocation mode is selected via a RESET strapping option as shown in Table 1 on page 7.

In dynamic buffer allocation mode, each port uses receive buffers from a common pool of available buffers. There are 1008 buffers available with 2 Mbyte of DRAM, 308 buffers with 1 Mbyte.

In fixed buffer mode, each port is assigned a fixed number of receive buffers. There are 320 buffers available per port with 2 Mbyte of DRAM, 140 buffers with 1 Mbyte.

The overflow of the Rx buffer threshold is indicated by the "Receive Buffer Full" LED in the Serial LED Interfaces. This indication is active only in fixed buffer mode.

8.   Packet Forwarding

The following sections describe the procedures for forwarding packets in the following situations:
- A unicast packet
- A multicast packet

8.1   Forwarding a Unicast Packet Across the Bridge

The sequence for forwarding a unicast packet across the bridge is as follows:

1. The incoming packet is fed to the Rx FIFO (there is an 20x32-bit Rx FIFO per port) and is transferred to an empty block in the Receive Buffer area of DRAM.

2. In parallel, an address recognition cycle is performed for both the DA and the SA. The GT-48006A uses the DA's corresponding Port Number to queue the packet to the other port, or to drop the packet if the destination port equals the source port.

3. At the end of an error-free packet transfer, packet information is written to the output port's transmit descriptor. This information includes the Byte Count and the Receive Buffer Block Address which is pointed to by the Write Pointer.

4. The Write Pointer of the outgoing port's transmit descriptor is incremented. The target device transmits whenever the Write Pointer is not equal to the Read Pointer.

5. At the end of the packet transmit process, the target device increments the Read Pointer and clears the appropriate bit in the Empty List.

8.2   Forwarding a Multicast Packet

The GT-48006A forwards Multicast packets across the bridge using the same mechanism as described for Unicast packets. Multicast and Broadcast packets are not re-sent on the input port.

8.3   Tx Watchdog Timer

The GT-48006A includes a transmit watchdog timer for each transmit queue. For 100Mbps operation, the value of the timer is 63msec. For 10Mbps operation, the default value of the timer is 630msec. The timer measures the time between the transmission of two consecutive outgoing packets. When the timer expires, the GT-48006A clears the appropriate used blocks.

9. Fast Ethernet Interfaces

The GT-48006A interfaces directly to two MII (Media Independent Interface) ports which are compliant with the IEEE standard (please see 802.3u Fast Ethernet standard for detailed interface information and timing parameters). Each MII port has the following characteristics:

- Capable of supporting both 10 Mbps and 100 Mbps data rates in half or full duplex modes
- Data and delimiters are synchronous to clock references
- Provides independent 4-bit wide transmit and receive paths
- Uses TTL signal levels
- Provides a simple management interface (common to all ports)
- Capable of driving a limited length of shielded cable

The GT-48006A incorporates all the required digital circuitry to interface to 100BaseTX, 100BaseT4, and 100BaseFX.

9.1 10/100 MII Compatible Interface

The GT-48006A MAC allows it to be connected to a 10Mbps or 100Mbps network. The GT-48006A interfaces to an IEEE 802.3u 10/100 Mbps MII compatible PHY device. The data path consists of a separate nibble-wide stream for both transmit and receive data. The GT-48006A can switch automatically between 10 or 100 Mbps operation depending on the speed of the network. Data transfers are clocked by the 25 MHz transmit and receive clocks in 100 Mbps operation, or by 2.5 MHz transmit and receive clocks in 10 Mbps operation. The clock inputs are driven by the PHY, which controls the clock rate based on auto-negotiation.

9.2 Media Access Control (MAC)

The GT-48006A MAC performs all of the functions of the 802.3 protocol such as frame formatting, frame stripping, collision handling, deferral to link traffic, etc. The GT-48006A ensures that any outgoing packet complies with the 802.3 specification in terms of preamble structure. The GT-48006A transmits 56 preamble bits before Start of Frame Delimiter (SFD). The GT-48006A operates in half-duplex or full-duplex modes. In half-duplex mode, the GT-48006A checks that there is no competitor for the network bus before transmission. In addition to listening for a clear line before transmitting, the GT-48006A handles collisions in a pre-determined way. If two nodes attempt to transmit at the same time, the signals collide and the data on the line is garbled. The GT-48006A listens while it is transmitting, and it can detect a collision. If a collision is detected, the GT-48006A transmits a 'JAM' pattern and then delays its re-transmission for a random time period determined by the backoff algorithm. In full-duplex mode, the GT-48006A transmits unconditionally.

9.3 Auto-negotiation

9.3.1 Disabled

Autonegotiation can be disabled for a port through the state of the DAddr[1:0] pins at reset. Following RESET the port duplex mode is set by the state sampled on DAddr[6] for Port 0 and DAddr[7] for Port 1. The speed that each port operates in (10Mbps or 100Mbps) is determined by the frequency of TxClk[x] and RxClk[x] generated by the PHY. When the port is operating at 10Mbps, the PHY generates a 2.5MHz clock for both TxClk and RxClk. When the port is operating at 100Mbps, the PHY generates a 25MHz clock for both TxClk and RxClk.

9.3.2 Enabled

When auto-negotiation is enabled for a port the GT-48006A decodes the duplex mode for each port from the values of the Auto-Negotiation Advertisement register and the Auto-Negotiation Link Partner Ability registers at the end of the Auto-Negotiation process.

Note: If autonegotiation is enabled for either port, then the link status for BOTH ports will be determined automatically by the GT-48006A by reading the PHY status registers. FORCE LINK PASS overrides the PHY in this mode.

The auto-negotiation feature on the GT-48006A is used only to tell the GT-48006A the duplex status of each port. The speed (10/100) of each port is determined only by RxClk and TxClk. The GT-48006A will continuously perform the following operations for each port (PHY addresses 1 and 2 alternately), implemented as READ commands issued via the

MDC/MDIO interface:

1. Read the PHY Auto-Negotiation Complete status. As long as PHY bit 1.5 (Register 1, bit 5) is '0' switch to Half-Duplex mode and continue to read PHY register bit 1.5. Continue to step 2 when PHY bit 1.5 is '1', signaling Auto-negotiation is complete.

Steps 2 through 6 are performed once for every transition of PHY bit 1.5 from '0' to '1'. Once PHY bit 1.5 remains '1' and PHY registers 4 and 5 have already been read, the GT-48006A will continue to read PHY register 1, and monitor PHY bit 1.5. Steps 2 to 6 are performed once, if after Rst* de-assertion, the PHY bit 1.5 is read as '1', in order to update the GT-48006A duplex mode.

NOTE: PHY bit 1.2 (Link Status) is read and latched during this same register read operation, regardless of the Auto-Negotiation status.

2. Read the Auto-Negotiation Advertisement register, PHY Register 4. Continue to step 3.

3. Read the Auto-Negotiation Link Partner Ability register, PHY Register 5. Continue to step 4.

4. Resolve the highest common ability of the two link partners in the following manner (according to the 802.3u Priority Resolution clause 28B.3):

  if (bit 4.8 AND bit 5.8) == '1' then ability is 100BASE-TX Full Duplex

   else if (bit 4.9 AND bit 5.9) == '1' then ability is 100BASE-T4 Half Duplex

    else if (bit 4.7 AND bit 5.7) == '1' then ability is 100BASE-TX Half Duplex

     else if (bit 4.6 AND bit 5.6) == '1' then ability is 10BASE-T Full Duplex

       else ability is 10BASE-T Half Duplex;

Continue to step 5.

5. Resolve the duplex mode of the two link partners in the following manner:

  if ((ability == "100BASE-TX Full Duplex") or (ability == "10BASE-T Full Duplex")) then

   duplex mode = FULL DUPLEX

    else duplex mode = HALF DUPLEX;

NOTE: the value of the duplex mode indication should change only after reading both PHY registers 4 and 5. Continue to step 6.

6. Update the GT-48006A MAC. Continue with step 1.

9.4   Backoff Algorithm Options

The GT-48006A implements the truncated exponential backoff algorithm defined by the 802.3 standard. Aggressiveness of the backoff algorithm used by all of the ports is controlled by the Limit4 pin. Limit4 controls the number of consecutive packet collisions that will occur before the consecutive collision counter is reset. When Limit4 is LOW, the GT-48006A resets the collision counter after 16 consecutive retransmit trials, restarts the backoff algorithm, and continues to try and retransmit the frame. A packet which is endlessly colliding on re-transmits will continue to be re-transmitted forever, only changing backoff intervals. The retransmission is done from the data already stored in the DRAM. In the case of a successful transmission, the GT-48006A is ready to transmit any other frames queued in its transmit FIFO within the minimum IPG of the link.

When Limit4 is HIGH, the GT-48006A will reset its collision counter and restarts the backoff algorithm after 4 consecutive transmit trials. This results in the GT-48006A being more aggressive in acquiring the media following a collision. This will result in better overall switch throughput (less packet loss) in standardized tests. Limit4 can be toggled during switch operation.

9.5   Data Blinder

The internal data blinder field sets the period of time during which the port does not look at the wire to decide to transmit (inhibit time.) The value is fixed at 32 bit times.

9.6   Inter-Packet Gap (IPG)

IPG is the idle time between any two successive packets from the same port. The value (from the standard) is 9.6uS for 10Mbps Ethernet and 960nsec for 100-Mbps Fast Ethernet.

9.7   10/100 Mbps MII Transmission (Half-Duplex)

When the GT-48006A has a frame ready for transmission, it samples the link activity. If the RxDV signal is inactive (no activity on the link), and the Inter-packet gap (IPG) counter has expired, frame transmission begins. The data is transmitted via pins TxD[3:0] of the transmitting port, clocked on the rising edge of TxClk. The signal TxEn is asserted at this same time. In the case of collision, the PHY asserts the CoL signal on the GT-48006A which will then stop transmitting the frame and transmit a jam sequence onto the link. After the end of a collided transmission, the GT-48006A will back off and attempt to retransmit once the backoff counter expires.

A waveform of the signals which are synchronous to TxClk (TxD0[3:0], TxD1[3:0], TxEn[1:0]) is shown in Figure 2. The actual delay times of the GT-48006A are tighter than the IEEE 802.3u standard, clause 22.3.1, as shown in Table 3.

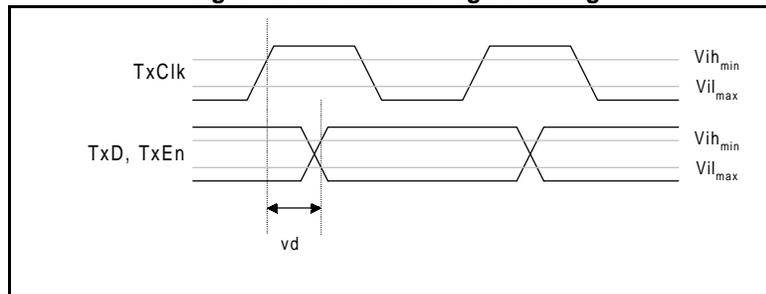**Figure 2: MII Transmit Signal Timing**

Table 3: MII Signal Timings Synchronous to TxClk

		GT-48006A		IEEE 802.3u Spec.		
Name	Parameter	MIN	MAX	MIN	MAX	Units
vd	Valid Delay after Rising TxClk	2	14	0	25	ns

9.8   10/100 Mbps MII Reception (Half-Duplex)

Frame reception starts with the assertion of RxDV (while the GT-48006A is not transmitting) by the PHY. Once RxDV is asserted, the GT-48006A will begin sampling incoming data on pins RxDV[3:0] on the rising edge of RxClk. Reception ends when the RxDV is deasserted by the PHY. The last nibble sampled by the GT-48006A is the nibble present on RxD[3:0] on the last RxClk rising edge in which RxDV is still asserted. During reception, the RxDV is asserted. If, while RxDV is asserted, the GT-48006A detects the assertion of RxEr, it will designate this packet as corrupted. While no reception is taking place, RxDV should remain deasserted.

A waveform of the signals which are synchronous to RxClk (RxD0[3:0], RxD1[3:0], RxDV[1:0], RxEr[1:0]) is shown in Figure 3. The setup and hold times of the GT-48006A are tighter than the IEEE 802.3u standard, clause 22.3.2, as shown in Table 4.
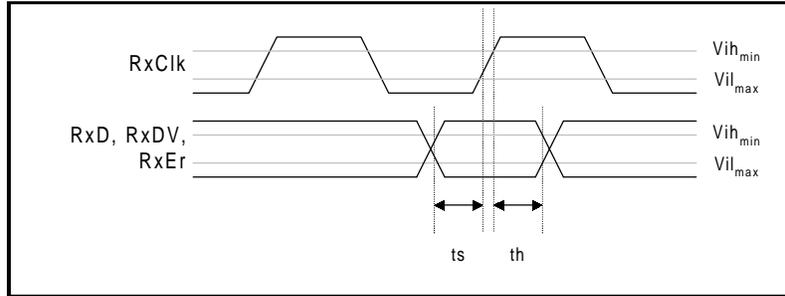
Figure 3: MII Receive Signal Timing

Table 4: MII Signal Timings Synchronous to RxClk

| Name | Parameter | GT-48006A | | IEEE 802.3u Spec. | | |
		MIN	MAX	MIN	MAX	Units
ts	Setup Time to Rising RxClk	6		10		ns
th	Hold Time after Rising RxClk	1		10		ns

9.9   10/100 Mbps Full-Duplex Operation

When operating in Full-duplex mode the GT-48006A can transmit and receive frames simultaneously. In full-duplex mode, the CrS signal is associated with received frames only and has no effect on transmitted frames. The Col signal is ignored by the GT-48006A while in Full-duplex mode. Transmission starts when TxEn goes active. Transmission starts regardless of the state of RxDV. Reception starts when the RxDV signal is asserted indicating traffic on the receive port of the PHY.

9.10   Illegal Frames

The GT-48006A will discard all illegal frames. Examples include: runts (less than 64 bytes), oversize (greater than 1518 or 1522 bytes), and bad FCS (bad CRC.)

9.11   Backpressure

Backpressure is supported for half-duplex operation. When the GT-48006A cannot allocate a receive buffer for an incoming packet, the device will transmit a jamming pattern on the port, thus forcing a collision. Backpressure is not active in full-duplex mode.

Backpressure is enabled via a RESET strapping option as shown in Table 1 on page 7. Backpressure is not active when dynamic buffer mode is enabled (see Section 7.1).

9.12   VLAN Tagging Support

The GT-48006A will pass 802.1q frames (i.e. frames up to 1522 bytes) if the VL Tag Enable is selected at RESET via the DAdr[4] pin.

10. MII Management Interface (SMI)

The GT-48006A MAC contains an MII Management Interface (SMI) for an MII compliant PHY devices. This allows control and status parameters to be passed between the GT-48006A and the PHY by one serial pin (MDIO) and a clocking pin (MDC), reducing the number of control pins required for PHY mode control. Typically, the GT-48006A will continuously query the PHY devices for their link status. The predefined PHY addresses for the link query are 1 and 2 (out of possible 32 addresses).

10.1 SMI Cycles

The SMI protocol consists of a bit stream that is driven or sampled by the GT-48006A on each rising edge of the MDC clock. The bit stream format of the SMI frame is described in Table 5.

Table 5: SMI Bit Stream Format

	PRE	ST	OP	PhyAd	RegAd	TA	Data	IDLE
READ	1...1	01	10	AAAAA	RRRRR	Z0	D..D(16)	Z
WRITE	1...1	01	01	AAAAA	RRRRR	10	D..D(16)	Z

- PRE (Preamble). At the beginning of each transaction, the GT-48006A sends a sequence of 32 contiguous logic one bits on MDIO with 32 corresponding cycles on MDC to provide the PHY with a pattern that it can use to establish synchronization.
- ST (Start of Frame). A Start of Frame pattern of 01.
- OP (Operation Code). 10 - Read; 01 - Write
- PhyAd (PHY Address). A 5 bit address of the PHY device (32 possible addresses). The first PHY address bit transmitted by the GT-48006A is the MSB of the address.
- RegAd (Register Address). A 5 bit address of the PHY register (32 possible registers in each PHY). The first register address bit transmitted by the GT-48006A is the MSB of the address. The GT-48006A always queries the PHY device for status of the link by reading register 1, bit 2.
- TA (Turn Around). The turnaround time is a 2 bit time spacing between the Register Address field and the Data field of the SMI frame to avoid contention during a read transaction. During a Read transaction the PHY should not drive MDIO in the first bit time and drive '0' in the second bit time. During a write transaction, the GT-48006A drives a '10' pattern to fill the TA time.
- Data (Data). The data field is 16 bits long. The PHY drives the data field during Read transactions. The GT-48006A drives the data field during write transactions. The first data bit transmitted and received shall be bit 15 of the PHY register being addressed.
- IDLE (Idle). The IDLE condition on MDIO is a high impedance state. The MDIO driver is disabled and the PHY should pull-up the MDIO line to a logic one.

10.1.1 SMI Timing Requirements

Figure 4 shows a waveform of the MDC line which is driven by the GT-48006A. Table 6 shows typical MDC timings.
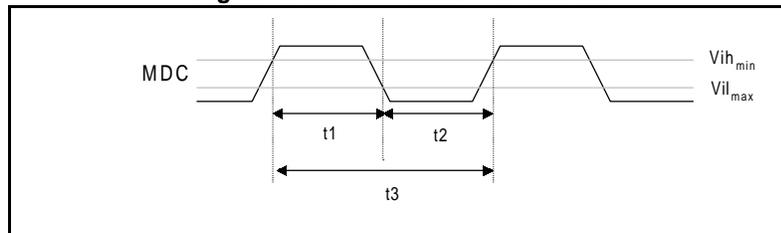
Figure 4: GT-48006A **MDC Waveform**

Table 6: Typical MDC Timings

Name	Parameter	GT-48006A TYPICAL	Units
t1	MDC High Time	480	ns
t2	MDC Low Time	480	ns
t3[1]	MDC Period	960	ns

1. MDC is generated internally by dividing the Clk clock input by 32. Clk clock frequency of 33MHz is assumed.

A waveform of the MDIO line when it is driven by the GT-48006A is shown in Figure 5. The actual delay times of the GT-48006A are tighter than the IEEE 802.3u standard, clause 22.3.4, as shown in Table 7.
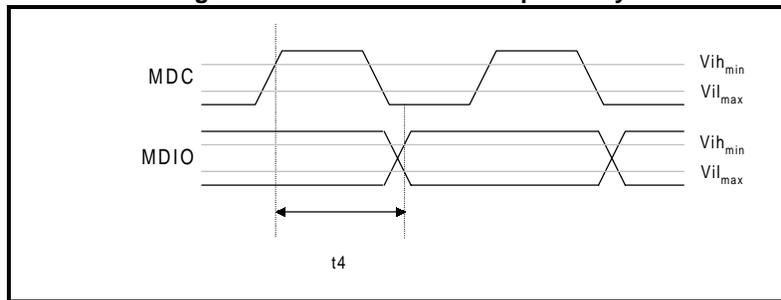
Figure 5: GT-48006A **MDIO Output Delay**

Table 7: MDIO Signal Timings (GT-48006A **Driving MDIO)**

		GT-48006A		IEEE 802.3u Spec.		
Name	Parameter	MIN	MAX	MIN	MAX	Units
t4	Rising MDC to Valid MDIO	10	50	0	300	ns

A waveform of the MDIO line when it is driven by the PHY is shown in Figure 6. The setup and hold times requirements of the GT-48006A are the same as the IEEE 802.3u standard, clause 22.3.4, as shown in Table 8.
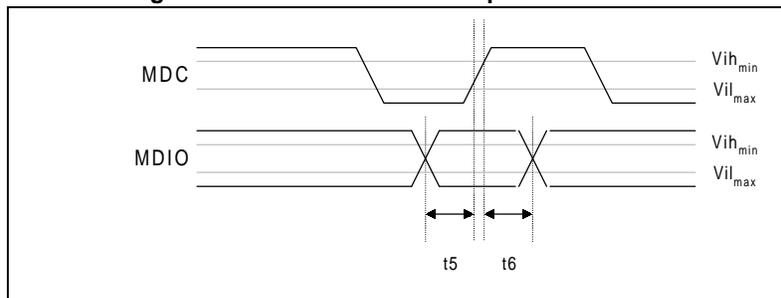
Figure 6: GT-48006A **MDIO Setup and Hold Time**

Table 8: MDIO Signal Timings (PHY Driving MDIO)

Name	Parameter	GT-48006A		IEEE 802.3u Spec.		Units
		MIN	MAX	MIN	MAX	
t5	Setup Time to Rising MDC	10		10		ns
t6	Hold Time after Rising MDC	10		10		ns

10.2   Link Detection and Link Detection Bypass (ForceLinkPass*)

Typically, the GT-48006A will continuously query the PHY devices for its link status. The predefined PHY addresses for the link query are 1 and 2 (out of possible 32 addresses). The GT-48006A will alternately read register 1 from PHY1 and PHY2 and update the internal link bits according to the value of bit 2 of register 1. In the case of "link is down" (i.e. bit 2 is '0'), that port will enter link test fail state. In this state, all of the port's logic is reset. The port will exit from link test fail state only when the "link is up" i.e. bit 2 of register 1 is read from the port's PHY as '1'.

The GT-48006A offers the option to disable the link detection mechanism by forcing the link state of both ports to the link test pass state regardless of the PHY's link bit value. This is done with the LEDStb pin, which is sampled at RESET (see Table 1 on page 7).

11. DRAM Interface and Usage

The GT-48006A includes direct support for EDO DRAMs. The performance of EDO satisfies the required bandwidth for wire-speed data transfer, address recognition and Tx descriptor fetch/update. The DRAM interface is entirely glueless. All accesses are performed as 32-bits. The DRAM interface is designed for 50ns EDO DRAMs and all timings are guaranteed to work with these devices. Refresh is performed automatically by the GT-48006A. Please refer to the EV-48006 evaluation platform schematics for an example of EDO DRAM design with the GT-48006A.

The GT-48006A requires about 300Kbytes of the DRAM for the address table and other private data structures. The remainder is used for packet buffers. Following power-up or system RESET, the GT-48006A device creates the MAC Address Table in DRAM, and initializes all locations in the table to indicate that invalid entries exist in all locations.

Galileo recommends using DRAM with 256K x 16 configuration. When using this configuration, 2 DRAM chips are required for 1 MByte, and 4 DRAM chips are required for 2 MBytes. If 1 MByte is selected, RAS0* should be connected to 2 DRAM chips while RAS1* should be left unconnected.

If 2 MBytes is selected, RAS0* will control the first 1MB bank, while RAS1* will activate the second 1MB bank. DData[31:0], DAddr[8:0], CAS*, and WE* should be connected to both banks.

Using 1 or 2 MBytes of DRAM is entirely up to the architect. 2MBytes increases the size of the Rx Buffer space. This performance advantage must be weighed against the cost of additional memory.

12. LED Support

The GT-48006A's serial LED interface is similar to the 3-pin LED interface of the GT-48001A device which requires a PAL to interpret the LED bit stream. Galileo provides reference designs and example PAL equations in the LED interface application note available on our website.

12.1 LED Indications Interface Description

Table 9 on page 21 shows the data accessible on the LED Indications Serial Interface for both GT-48006A ports.

Table 9: LED Signals Available

Data Description	Symbolic Signal Name	Type
Primary Port Status LED	primary_port_status	n/a
Transmit data in progress	transmit	dynamic
Receive data in progress	receive	dynamic
Collision active	collision	dynamic
Full/Half duplex	full_duplex	static
Receive Buffer Full	rx_buffer_full	dynamic

### 12.2 Detailed LED Signal Description

12.2.1 Primary Port Status LED

The Primary Port Status LED provides the following information:

> If Link Integrity test failed
> > Port Status LED blinks once;
> else Everything is OK (Port Status LED is ON)

12.2.1.1 Status LED blink timing

Link Integrity test failed, Status LED blinks once. Primary status bit is active for 500 ms every 5s.

Link Integrity Test Fails: Primary Status LED Blinks 500ms every 5 seconds
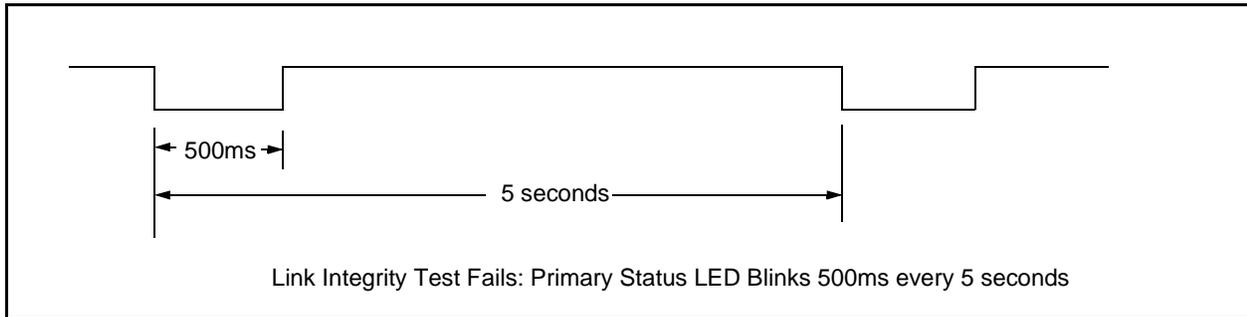
12.2.2 Transmit data in progress

This signal indicates the port is transmitting data.

12.2.3 Receive data in progress

This signal indicates port receive activity.

12.2.4 Collision active

This signal indicates the port collision event detected by the port.

12.2.5 Full/Half duplex

This signal indicates the port duplex: active - full duplex, inactive - half duplex.

12.2.6 Receive Buffer Full

In order for this LED to be active, Rx Buffer Threshold must be enabled (i.e. the GT-48006A must be in fixed buffer allocation mode.) This signal indicates the port receive buffer status: active - the buffer exceeds it's programmed threshold, inactive otherwise.

12.2.7 Link Fail State

This signal indicates the port link status: active - link is down, inactive - link is up.

12.2.8 Pure Port Status LED

This signal will be inactive for the following event:

- Link Integrity Test Failed

Otherwise, this signal is active.

12.3 LED Signals Timing Type

12.3.1 Static LED Signals

These signals are stable for relatively long time periods. The LED indication directly reflects their current value. The static signals are:

- Port Status
- Forwarding of Unknown packets enabled
- Full/Half Duplex

12.3.2 Dynamic Internal Signals:

These signals are typically active for short time periods. In order to be visible through the LED Indication Interfaces, the GT-48006A includes a "monostable" function per each of these dynamic signals so they can be viewed on the LED indication output for a period of about 62 ms. The dynamic signals are:

- Port Status
- Transmit data in progress (TxEn)
- Receive data in progress (RxDV)
- Collision active (Col)
- Receive Buffer Full

12.4 Serial LED Interface Description

The LED serial interface consists of three outputs:
- **LEDClk**: LEDClk is the primary timebase of the LED Indications Interface. It is a 50% duty cycle free running clock at a fixed frequency of 1 MHz. LEDClk is HIGH-Z when Rst* is asserted.
- **LEDStb**: LEDStb (active HIGH) indicates the beginning of the data frame. LEDStb is activated for a duration of one LEDClk cycle once every 128 LEDClk cycles, starting from Rst* deactivation. This signal marks the beginning of the 128 bit long LED data frame. LEDStb transitions occur 90 ns after LEDClk rising edge.
- **LEDData**: The internal signals are multiplexed on the LEDData output for every data frame. LEDStb activation signals the presence of data bit #1 (out of 128 bits) on the LEDData output. LEDData transitions occur 90 ns after LEDClk rising edge. All internal signals accessible via LEDData are active HIGH internally and are inverted on the LEDData output (i.e. when an internal signal is active, the data bit on the LEDData output will be LOW). For example: If port 0 transmits data, the internal_event_transmit[0] signal is active HIGH and the corresponding bit 9 in the LEDData serial stream is LOW.

The timings for the LED serial interface are shown in Figure 7.

Figure 7: Serial LED Interface Timings
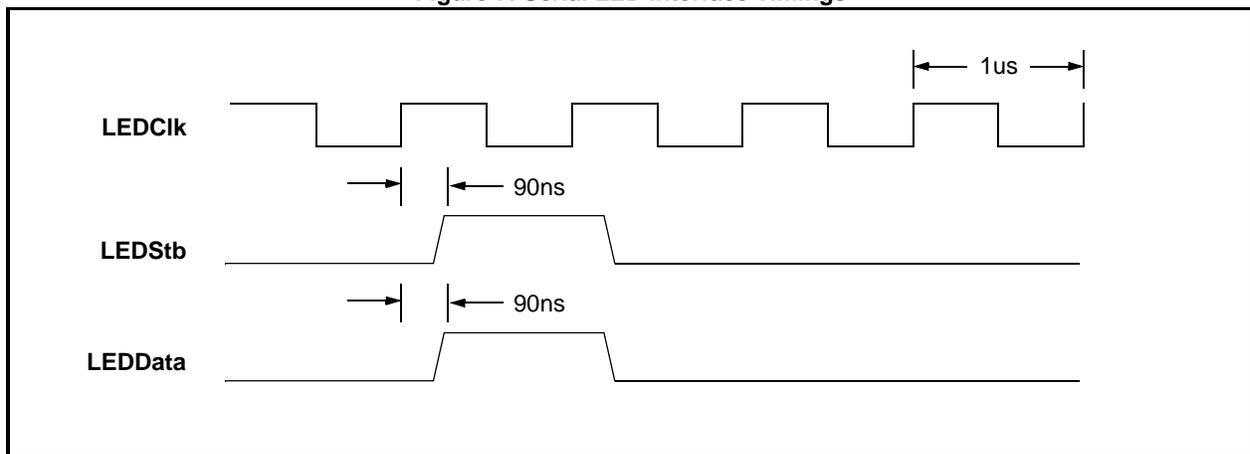
12.4.1   Table of Internal Activities/Status Driven via the Serial LED Interface

The following table defines a bit by bit description of the internal signals driven through the LED Indications Serial Interface. The bit number refers to the activation of LEDStb. LEDStb is active for bit# 1. RESERVED bit contents are not defined (i.e. can be either HIGH or LOW).

Table 10: LED Signals

Bit Number	Signal	Bit Number	Signal
1	primary_port_status[0]	22	-reserved-
2	primary_port_status[1]	23	full_duplex[1]
3-8	-reserved-	24-72	-reserved-
9	transmit[0]	73	link_test_fail[0]
10	receive[0]	74	link_test_fail[1]
11	collision[0]	75-97	-reserved-
12	rx_buffer_full[0]	97	pure_port_status[0]
13	-reserved-	98	pure_port_status[1]
14	-reserved-	99-128	-reserved-
15	full_duplex[0]		
16	-reserved-		
17	transmit[1]		
18	receive[1]		
19	collision[1]		
20	rx_buffer_full[1]		
21	-reserved-		

13.   Pinout for 100 Pin PQFP

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	DData[31]	36	DData[2]	71	GND
2	DData[30]	37	GND	72	Col[0]
3	DData[29]	38	DData[1]	73	TxEn[1]
4	GND	39	DData[0]	74	TxClk[1]
5	DData[28]	40	CAS*	75	**Vtol**
6	DData[27]	41	WE*	76	TxD1[3]
7	DData[26]	42	Vdd	77	Vdd
8	DData[25]	43	RAS[1]*	78	TxD1[2]
9	DData[24]	44	RAS[0]*	79	TxD1[1]
10	Vdd	45	DAddr[8]	80	TxD1[0]
11	DData[23]	46	DAddr[7]	81	RxD1[3]
12	DData[22]	47	DAddr[6]	82	RxD1[2]
13	DData[21]	48	DAddr[5]	83	RxD1[1]
14	DData[20]	49	DAddr[4]	84	Vdd
15	DData[19]	50	DAddr[3]	85	RxD1[0]
16	DData[18]	51	DAddr[2]	86	RxEr[1]
17	DData[17]	52	DAddr[1]	87	RxClk[1]
18	DData[16]	53	DAddr[0]	88	GND
19	DData[15]	54	GND	89	RxDV[1]
20	GND	55	TxEn[0]	90	CrS[1]
21	DData[14]	56	TxClk[0]	91	Col[1]
22	DData[13]	57	TxD0[3]	92	MDC
23	DData[12]	58	TxD0[2]	93	MDIO
24	DData[11]	59	TxD0[1]	94	Scan*
25	Vtol (Future: Aging)	60	TxD0[0]	95	GND
26	DData[10]	61	Clk	96	TriState*
27	DData[9]	62	RxD0[3]	97	LEDClk
28	DData[8]	63	GND	98	LEDData
29	GND	64	RxD0[2]	99	LEDStb
30	DData[7]	65	RxD0[1]	100	Rst*
31	DData[6]	66	RxD0[0]		
32	DData[5]	67	RxEr[0]		
33	Vdd	68	RxClk[0]		
34	DData[4]	69	RxDV[0]		

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
35	DData[3]	70	CrS[0]		

NOTE: Vtol pins were shown as Vdd in the last version of this document and in recent pinout lists. Pin 25 is currently used as a "Vtol" pin, and must be tied HIGH for proper operation. In a future revision, automatic address aging will be supported, and this pin will control this operation. See section 6.3 for more information.

14.   DC Characteristics - *PRELIMINARY/SUBJECT TO CHANGE*

14.1   Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
Vdd	Supply Voltage	-0.3	3.6	V
Vtol	Input Voltage Tolerance Protection Pins[1]	3.0	5.25	V
Vi	Input Voltage	-0.3	Vtol+0.3	V
Vo	Output Voltage	-0.3	Vdd+0.3	V
Io	Output Current		24	mA
Iik	Input Protect Diode Current			mA
Iok	Output Protect Diode Current			mA
Tc	Operating Case Temperature	0	70	C
Tstg	Storage Temperature	-40	125	C

1. This voltage does not apply to CLK. CLK is NOT 5V tolerant.

14.2   Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vdd	Supply Voltage	3.0		3.6	V
Vtol	I/O Voltage Tolerance Protection Voltage (3.3V I/O)	3.0		3.6	V
Vtol	I/O Voltage Tolerance Protection Voltage (5.0V I/O)[1]	4.75		5.25	V
Vi	Input Voltage	0		Vdd	V
Vo	Output Voltage	0		Vdd	V
Tc	Case Operating Temperature	0		70	C
Cin	Input Capacitance				pF
Cout	Output Capacitance				pF

1. This voltage does not apply to CLK. CLK is NOT 5V tolerant.

14.3   DC Electrical Characteristics Over Operating Range

(Tc=0-80 C; Vdd=+3.3V, +/-5%)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Vih	Input HIGH level	Guaranteed Logic HIGH level	2.0			V
Vil	Input LOW level	Guaranteed Logic LOW level			0.8	V
Voh	Output HIGH Voltage	IoH = 2 mA IoH = 4 mA IoH = 8 mA IoH = 12 mA IoH = 16 mA IoH = 24 mA	2.4		Vdd	V

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Vol	Output LOW Voltage	IoL = 2 mA IoL = 4 mA IoL = 8 mA IoL = 12 mA IoL = 16 mA IoL = 24 mA	0		0.4	V
Iih	Input HIGH Current				+-1	uA
Iil	Input LOW Current				+-1	uA
Iozh	High Impedance Output Current				+-1	uA
Iozl	High Impedance Output Current				+-1	uA
Icc	Operating Current	Vdd = 3.45V f=40MHz			175	mA

NOTE: Pullup/Pulldown resistors are 45KOhm minimum, 65KOhm typical, 80KOhm maximum.

14.4   Thermal Data

Table 11: 100 PQFP Thermal Data

Parameter	Definition	Value
θ_{ja}	Thermal resistance: junction to ambient, 0 ft./s airflow	42.0 C/W

15.   AC Timing - *PRELIMINARY/SUBJECT TO CHANGE*

(Tc= 0-70°C; VDD= +3.3V, +/- 5%)

Symbol	Signals	Description	Min	Max	Unit
	Clk	System Clock	30	40	MHz
	Clk	Rise/Fall Time	1	4	V/ns
	Rst*				
t3	DAddr[8:0], DData[31:0], CAS*, RAS*, WE*	Delay from Clock Rising or Falling Edge	2	13	ns
t4	DData[31:0]	Setup	10		ns
t5	DData[31:0]	Hold	1		ns
t6	DData[31:0]	Float Delay	2	16	ns
t7	DData[31:0]	Drive Delay	2	10	ns

Notes:
1. All Delays, Setup, and Hold times are referred to Clk rising edge, unless stated otherwise.
2. All outputs are specified for 50pF load.
3. "All Inputs" and "All Outputs" also refer to I/O signal behavior.

Figure 8: Output Delay from Rising Edge
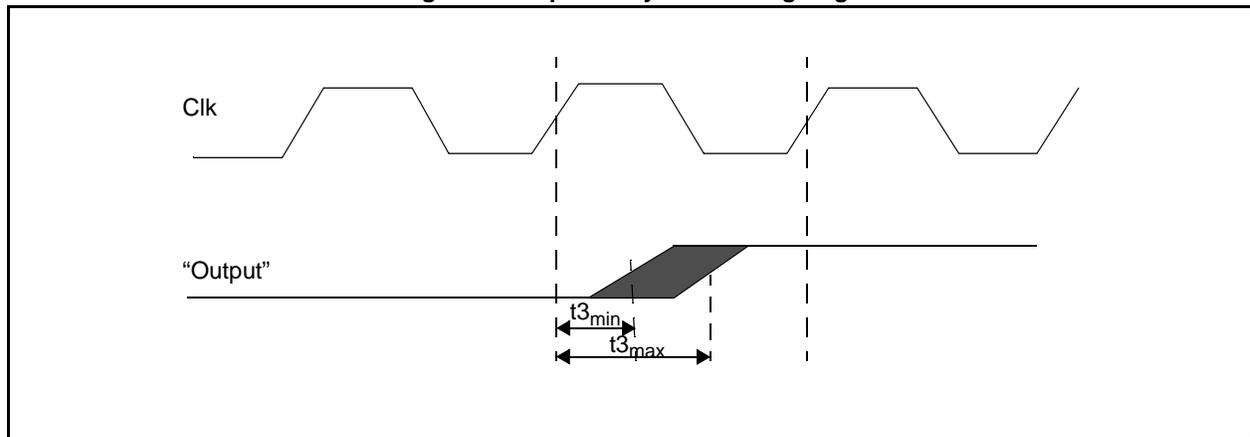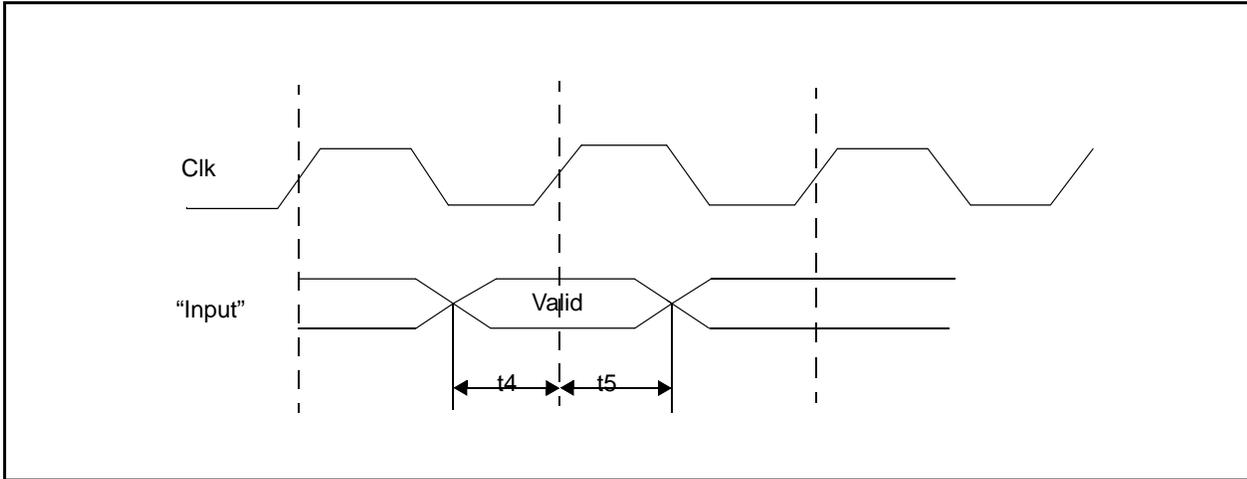
Figure 9: Input Setup and Hold

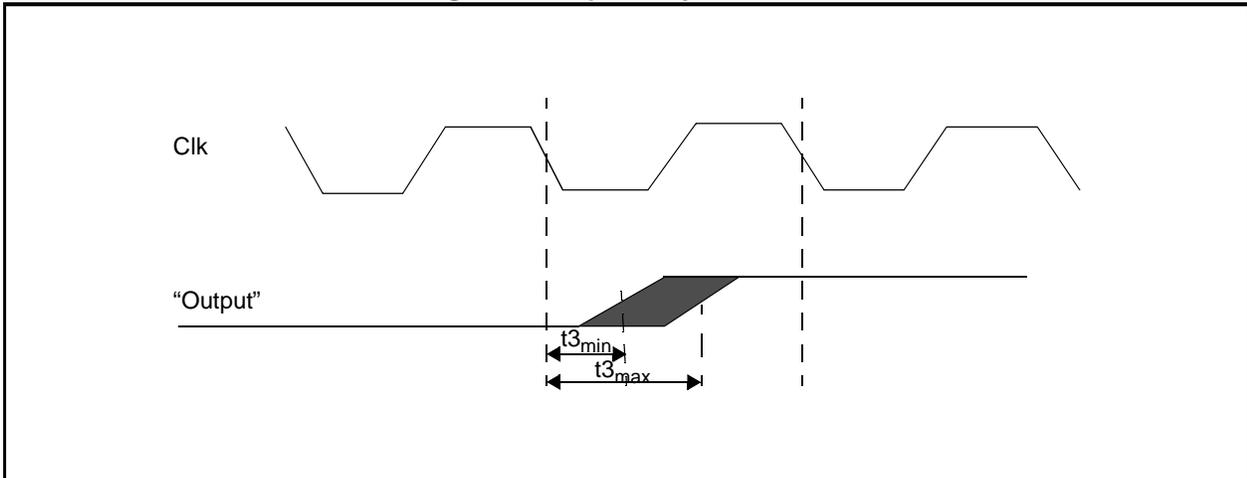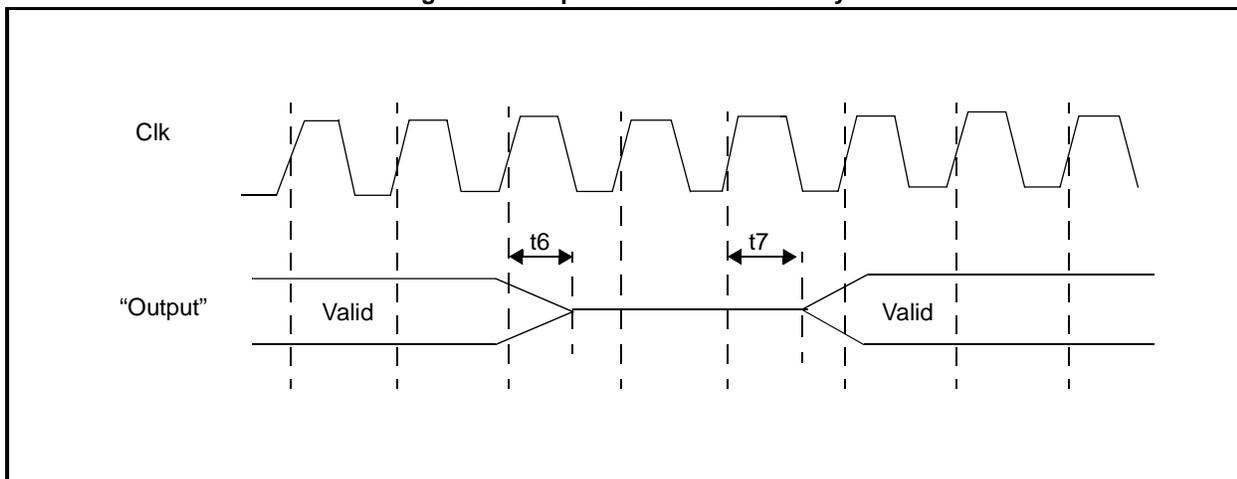**Figure 10: Output Delay from Clock**

Figure 11: Output Float and Drive Delay

16.   Functional Waveforms

Figure 12: EDO DRAM Read

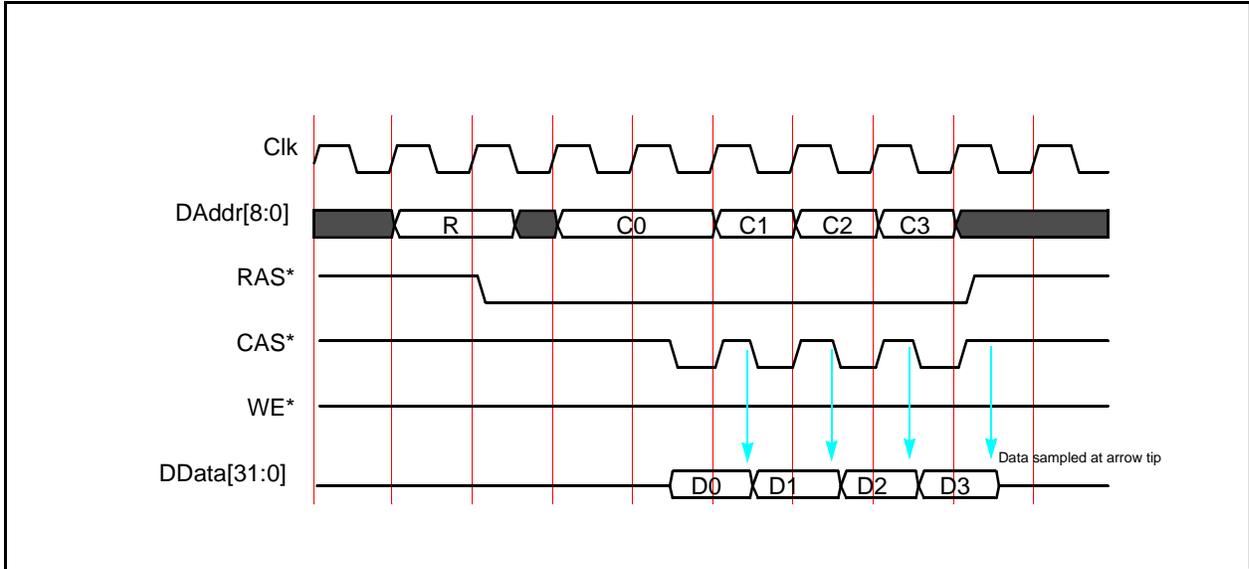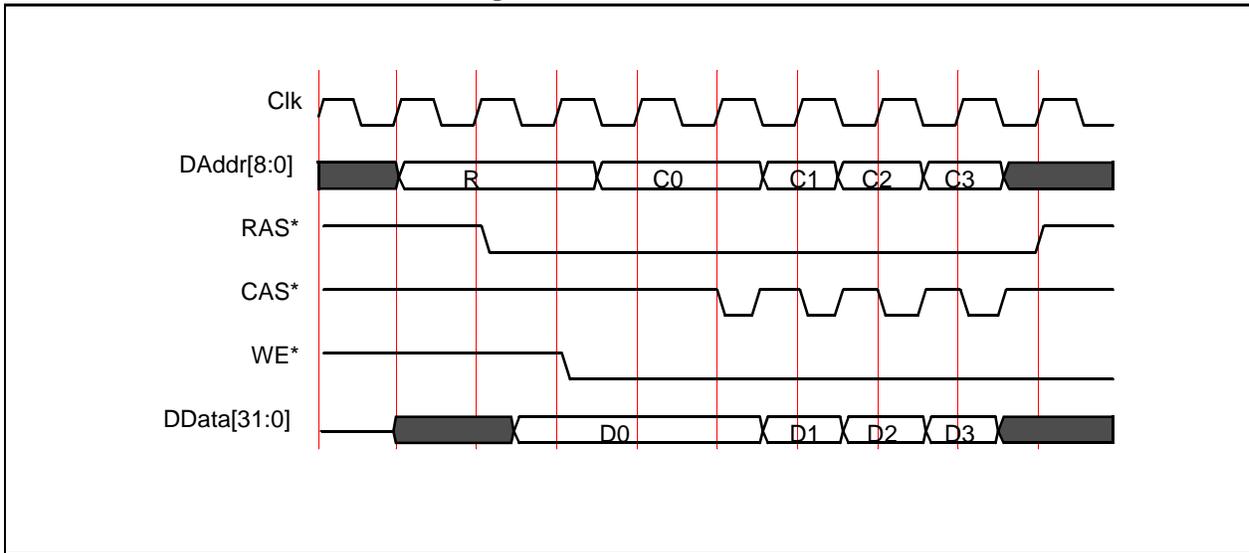**Figure 13: EDO DRAM Write**

17.   Packaging

Figure 14: 100 Lead PQFP Package Outline

18.   Document History

Table 12: Document History

Document Type	Rev. Number	Date	Comments
PRELIMINARY REV	1.1	6/17/98	Added definition for pin 25, Aging. Increase temperature specification. removed Thermal resistance: junction to case.
PRELIMINARY	1.2	8/3/98	Set minimum CLK frequency restriction (min.=30MHz, max.=40MHz).