AN1214
APPLICATION NOTE

DESIGN TIPS FOR L6561 POWER FACTOR CORRECTOR IN WIDE RANGE

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This application note will describe some basic steps to optimize the design of the L6561 PFC for wide range voltage input (105V- 300V) while also having a broad output power range (65W - 105W). Initial design steps are covered in application note AN966. This is to serve as a supplement to that application note and also give an example of a wide range demo board optimized for the US market (110V - 277V). A deeper look at the control of the L6561 can also be found in application note AN1089 "Control loop modeling of L6561-based TM PFC".

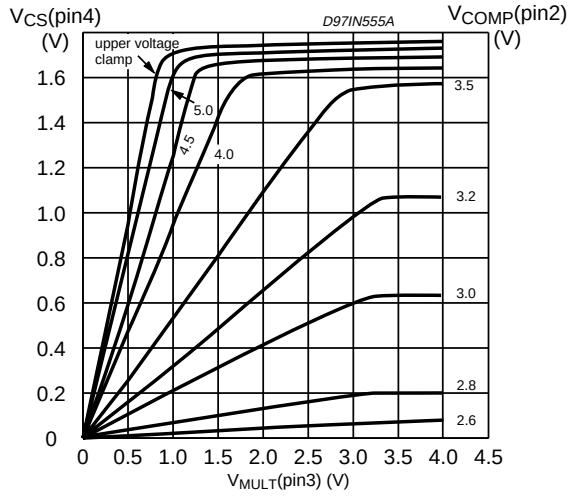
Introduction

Designing a PFC circuit with a singular input voltage and a singular output power is a task that is rather straight forward and gives a very good set of component values when the design equations are used. The task becomes a little more difficult when a wide range PFC is needed and the specifications are tight. This is common in applications such as lighting where there is a demand for good power factor (>.99) and THD less than 10% in the full range of nominal operating conditions. The problem occurs since the design must be done for the worst case conditions which are a low input voltage and maximum output power. As we will see, this will diminish the performance of the PFC circuit when the input voltage is high and the output power is low. What must be done in this case is to look closely at the limits of the L6561 and external components and to optimize or compromise where needed.

Design Tips

Multiplier Operation. Once the initial design is done and measurements have been made, the next step is to look at the operating parameters of the L6561 to see that it is working within its full capabilities without going over its linear operating range. A copy of the table we will be referring to is shown in Fig. 1.

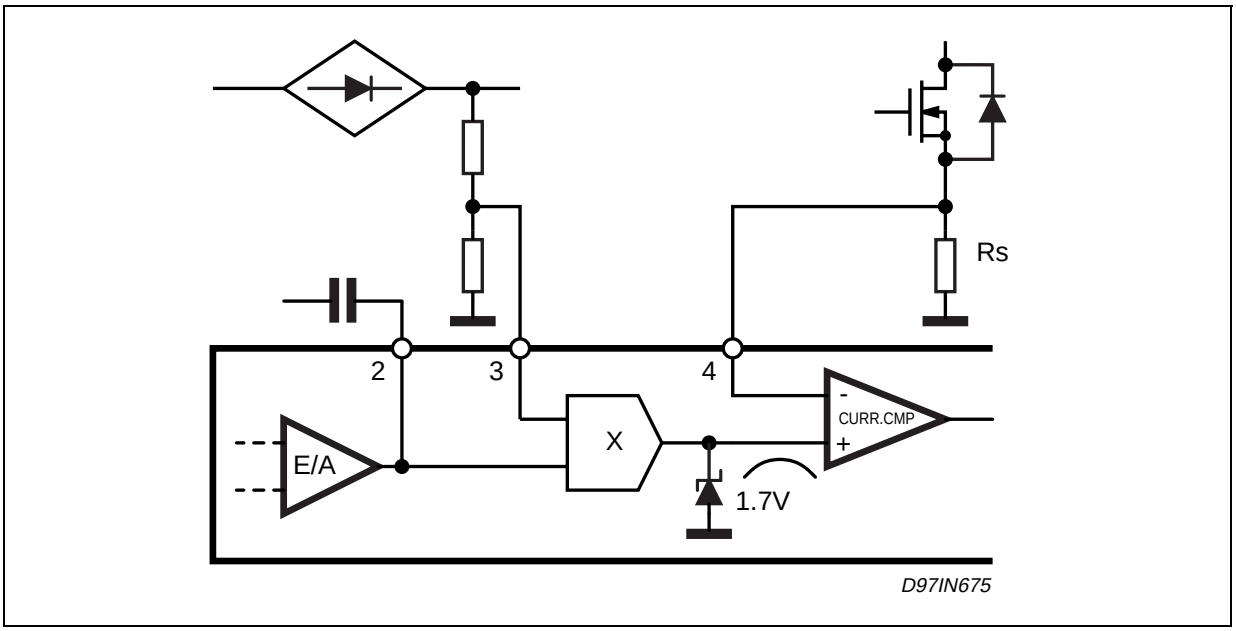
Figure 1. Multiplier Characteristics



For optimal operation the device should stay in the linear operation of the multiplier. As can be seen, there are three pins that should be measured in the worst case conditions. The first is with the lowest input voltage (low line) and the highest output power. The second is at the highest input voltage (high line) and the lowest output power. The first pin to be measured is the Vcomp (pin2). This is the output of the error amplifier (Figure 2) and will determine which curve will be referenced when measuring the other two parameters - Vcs and Vmult. Once this is established, the peak voltage of the multiplier input (pin 3) should be measured and noted. Next measure the peak voltage of the current sense resistor (Vcs - pin 4). Looking at the graph in Figure 1, determine which curve to use from the Vcomp voltage.

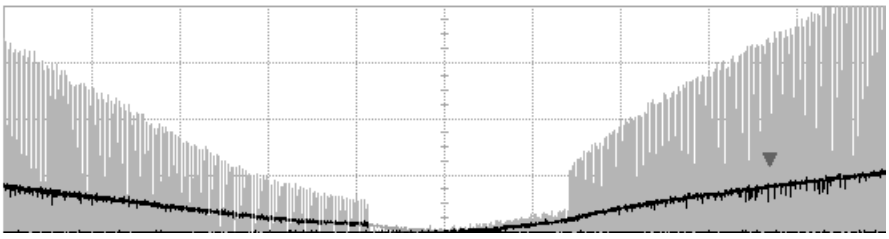
Next, note where the Vcs and Vmult are on the curve to make sure that they are in the linear operating region. If operation in the linear region is not met, adjust the variable that allows linear operation to be met. If however the device is operating in the linear region but is not allowing the full range of the multiplier to be used, then increasing one of the variables (the multiplier voltage for example) can help to maximize the full operating range of the multiplier.

Figure 2. Multiplier Block Diagram.



Zero crossing dead time. Once the multiplier operating parameters have been met, the input voltage as well as the input current should be looked at together. One problem to look for is a distortion of the current waveform especially at high line and low load. An example can be seen in figure 3.

Figure 3. Current Shape at Zero Crossing with High Capacitance FET and slow Turn-on Diode.



The main reason for this effect is that near zero-crossings the energy stored in the inductor is very low, not enough to charge up the drain node total capacitance (basically, the FET's drain-to-source capacitance C_{oss} and the inductor's parasitic intrawinding capacitance) to turn the boost diode on. The turn-on speed of the boost diode adds to the problem as well. As a result, energy is exchanged between reactive components and there is no input-to-output transfer. This can be seen in figure 3.

To minimize Coss, the $Rds_{(ON)}$ of the FET should be maximized within the limits of acceptable conduction losses, and its voltage rating should be the minimum that still provides adequate breakdown capability. In fact, both

a low $Rds_{(ON)}$ and a high voltage imply a higher C_{oss}.

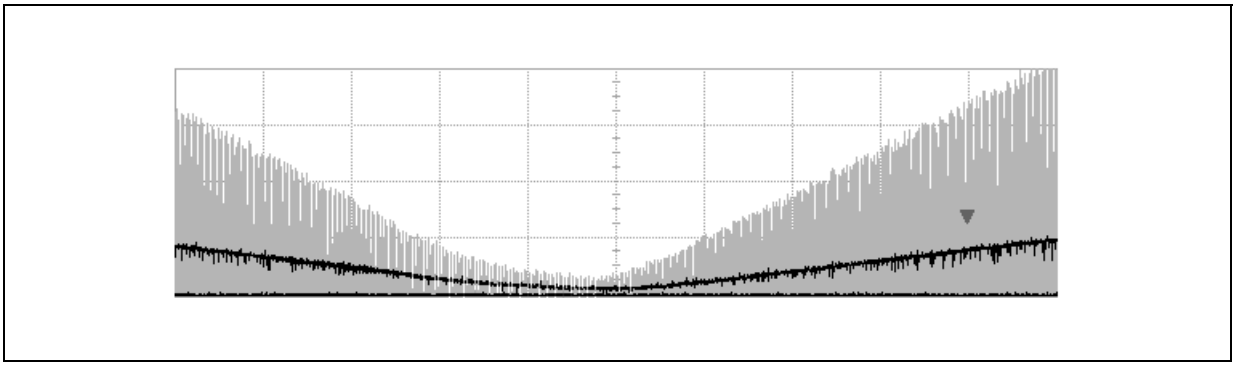
Inductor parasitic capacitance can be reduced by minimizing the number of winding layers. Adding a layer of tape between winding layers can reduce the capacitance considerably. The use of a slotted bobbin is also very effective.

Also optimizing the diode can offer a positive contribution. A minimum junction capacitance will be somewhat beneficial, even though this is a minor contribution to the total drain capacitance.

A major improvement can be offered by a diode with a well controlled die resistivity (such as Turboswitch series) which has a lower peak forward voltage, so that it actually turns on just a few volts above the PFC output voltage.

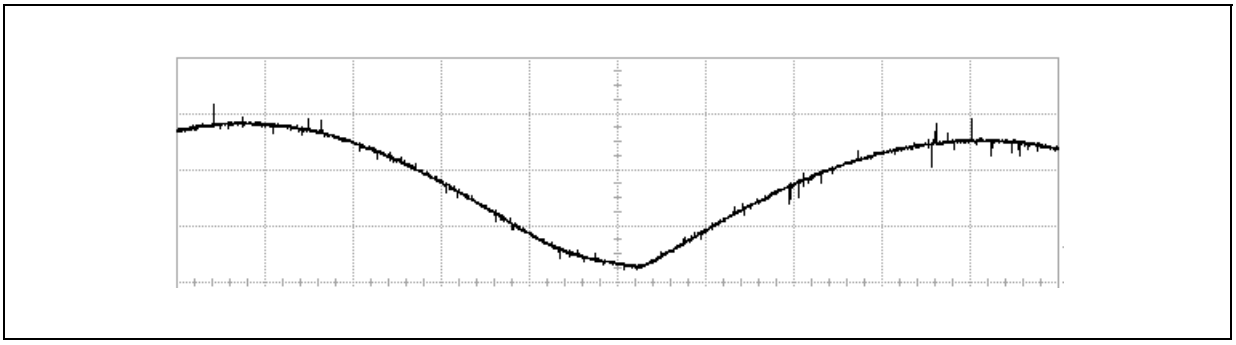
An example of the improvement given by optimizing the FET and the diode is shown in figure 4.

Figure 4. Current Shape at Zero Crossing with Lower Capacitance FET and Turboswitch Diode



Input capacitance (EMI filtering). Another source of error can be due to the input filter. Since the voltage output from the rectifier bridge is used as the reference for the current to follow, any distortions in this waveform will translate into distortions of the current waveform, hence lower power factor or greater THD. One cause of this can be due to too large of a high frequency filter capacitor being used after the bridge. A high value capacitor can filter the rectified voltage and cause the voltage to deviate from a rectified sinusoid and even not reach zero at light load. This can be seen in figure 5.

Figure 5. Non-discontinuous Voltage Error



The obvious way of improving this is to lower the high frequency capacitor value. Care must be taken not to lower the capacitance such that the effectiveness of the EMI filter (in front of the diode bridge) is not degraded so as to not pass regulatory requirements. So, by lowering that capacitance, the HF filter capacitor in front of the diode bridge may need to be increased.

Switching frequency. One other method of using the full dynamic range of the L6561 is to reduce the minimum switching frequency of the FET. By using the lowest possible switching frequency of the L6561, a wider range

of switching frequencies are available to be used. This helps minimize the effects of the internal propagation delay as well as the offset of the current sense comparator. In this way the current will track the voltage waveform better, in particular near the zero-crossings. This, however, must be weighed against the size increase of the inductor because a lower switching frequency implies a larger inductance value.

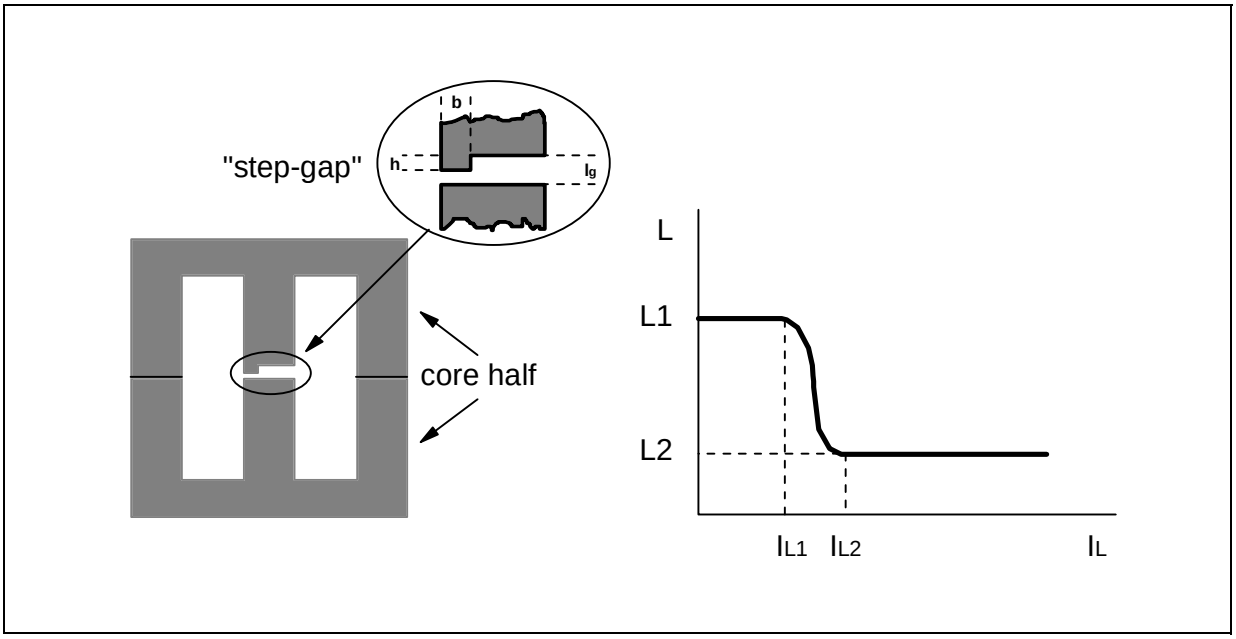
When determining the lowest frequency, it must be noted that switching below 15kHz is not recommended since this may interfere with the internal starter.

A special construction technique of the inductor can offer the optimum compromise: one that allows the use of a low inductance value so as to minimize inductor size and, at the same time, have a lower switching frequency near zero-crossings. The price to pay for that is an additional step in the inductor manufacturing flow.

It is the so-called “step-gap core” technique: the centre leg of one half of the ferrite core is ground so that the air gap thickness has a step change, as shown in fig. 6.

At low inductor current the small thinner part of the air gap dictates a high inductance value (L1). As current increases above a certain value (I_{L1}), the thinner part of the air gap will progressively saturate and the inductance will drop to a value (L2<L1) determined by the thicker part of the air gap (l_g). A non-linearity is deliberately introduced so that, for a given switching frequency at the top of the rectified sinusoid - where current is high - (that is, for a given L=L2), the switching frequency near the zero-crossings - where current is low - will not go as high as with a linear inductor.

Figure 6. Step-gap ferrite grinding and its effect on inductance value



The appropriate height h and breadth b of the ferrite step (both of them determine L1 and I_{L1}) for a given application will be found empirically.

Wide Range Example Circuit

An example circuit was designed with a varying voltage input of 110V to 277V and an output power of 65W to 105W. The techniques in this paper (except the step-gap core) were used to help bring the power factor and THD into acceptable levels. The example schematic and associated EMI filter are shown below along with the measured results.

Figure 7. Example Schematic

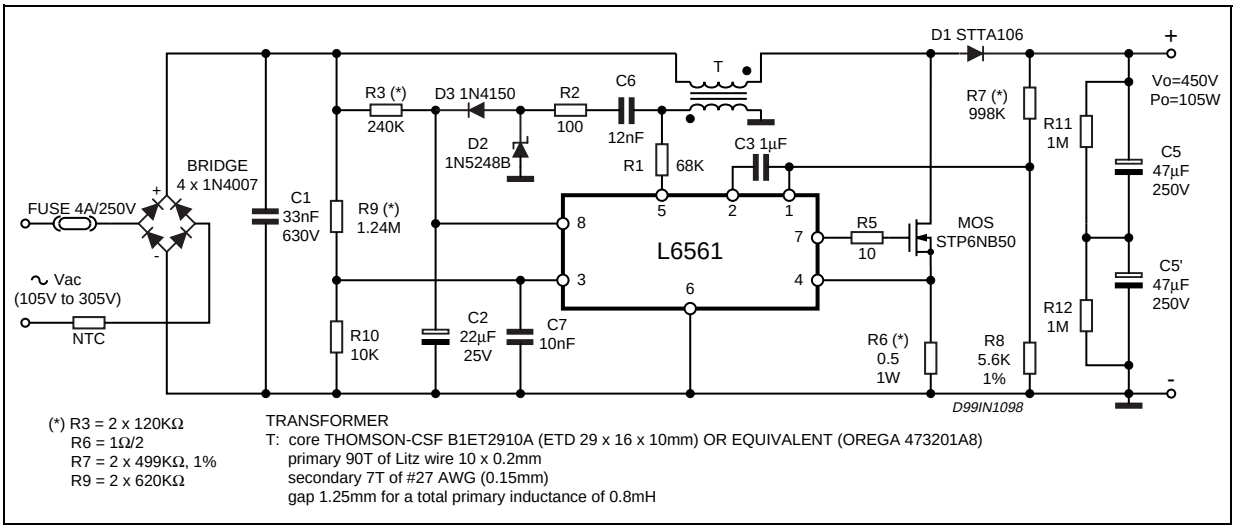


Figure 8. Emi Filter

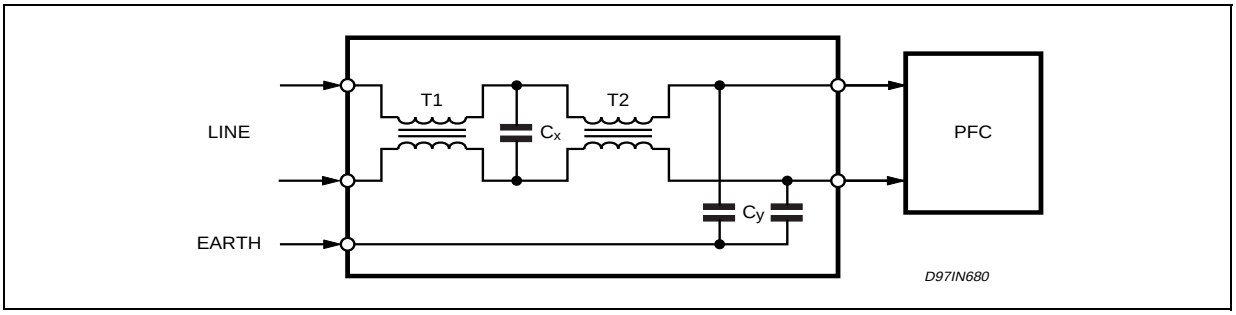


Table 1. Example Schematic Results

Vin [V_{AC}]	Vout [V]	Iout [mA]	PF	THD [%]	Pin [W]	Pout [W]	Efficiency [%]
105	449	136	0.998	4.7	66.4	61.0	91.9
120	449	136	0.998	5.3	65.8	61.0	92.7
277	449	136	0.995	9.7	65.0	61.0	93.9
300	449	136	0.993	11.0	65.0	61.0	93.9
105	449	237	0.999	4.0	115.8	106.5	92.0
120	449	237	0.999	4.0	114.7	106.5	92.9
277	449	237	0.997	7.7	111.0	106.5	96.0
300	449	237	0.994	11.2	111.0	106.5	96.0

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