MOTOROLA

Military 54LS164

8-Bit Parallel-Out Shift Register

ELECTRICALLY TESTED PER:
MIL-M-38510/30605

The 'LS164 is a high-speed 8-Bit Serial-in Parallel-Out Shift Register. Serial data is entered through a 2-input AND gate synchronous with the LOW to HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register setting all outputs LOW independent of the clock. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with Motorola TTL products.

- Typical Shift Frequency of 35 MHz
- Asynchronous Master Reset
- Gated Serial Data Input
- Fully Synchronous Data Transfers
- Input Clamp Diodes Limit High-Speed Termination Effect

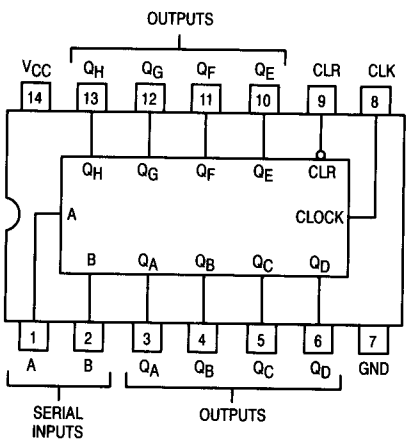
AVAILABLE AS:

1) JAN: JM38510/30605BXA
2) SMD: N/A
3) 883: 54LS164/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

CONNECTION DIAGRAM



PIN ASSIGNMENTS

FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
A IN	1	1	2	V_{CC}
B IN	2	2	3	V_{CC}
Q_A	3	3	4	OPEN
Q_B	4	4	6	OPEN
Q_C	5	5	8	OPEN
Q_D	6	6	9	OPEN
GND	7	7	10	GND
CLK	8	8	12	V_{CC}
CLR	9	9	13	GND
Q_E	10	10	14	OPEN
Q_F	11	11	16	OPEN
Q_G	12	12	18	OPEN
Q_H	13	13	19	OPEN
V_{CC}	14	14	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

Pin Names		Loading (Note a) HIGH	LOW
A, B	Data Inputs	0.5 U.L.	0.25 U.L.
CLK	Clock (active HIGH going Edge Input)	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active Low) Input	0.5 U.L.	0.25 U.L.
Q_A-Q_H	Outputs	10 U.L.	5(2.5) U.L.

MODE SELECT TRUTH TABLE

Operating Mode	Inputs $\overline{MR}$	A	B	Outputs Q_A	Q_B – Q_H	
Reset (Clear)	L	X	X	L	L	L
Shift	H	l	l	L	q_A	q_G
	H	l	h	L	q_A	q_G
	H	h	l	L	q_A	q_G
	H	h	h	H	q_A	q_G

H (h) = HIGH Voltage Levels
L (l) = LOW Voltage Levels
X = Don't Care
q_n = Lower case letters indicate the state of the reference input or output one set-up time prior to the Low to High clock transition.

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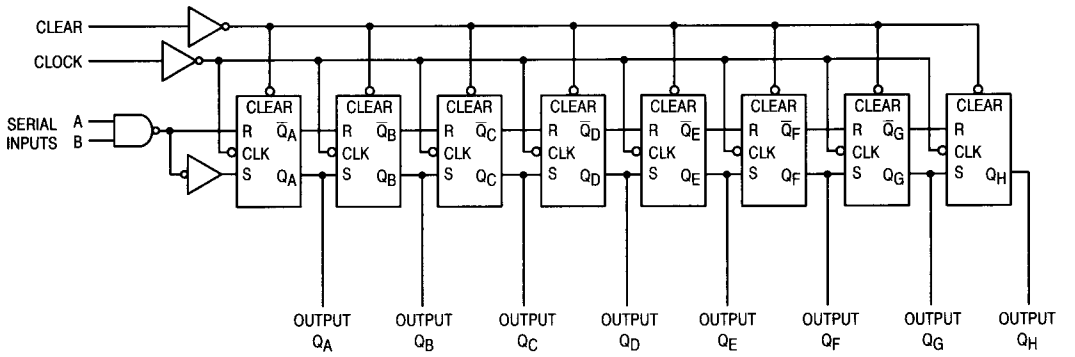
LOGIC DIAGRAM

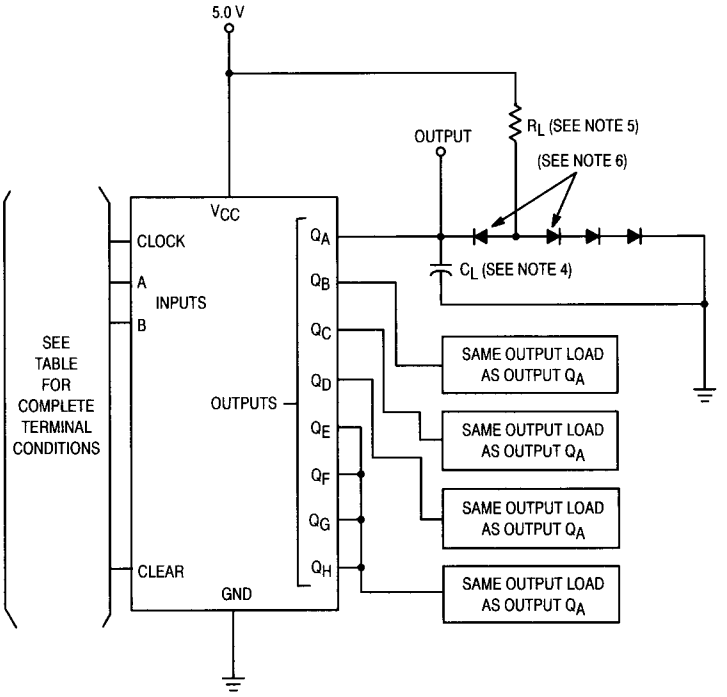


FUNCTIONAL DESCRIPTION

The 'LS164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH, or both inputs connected together.

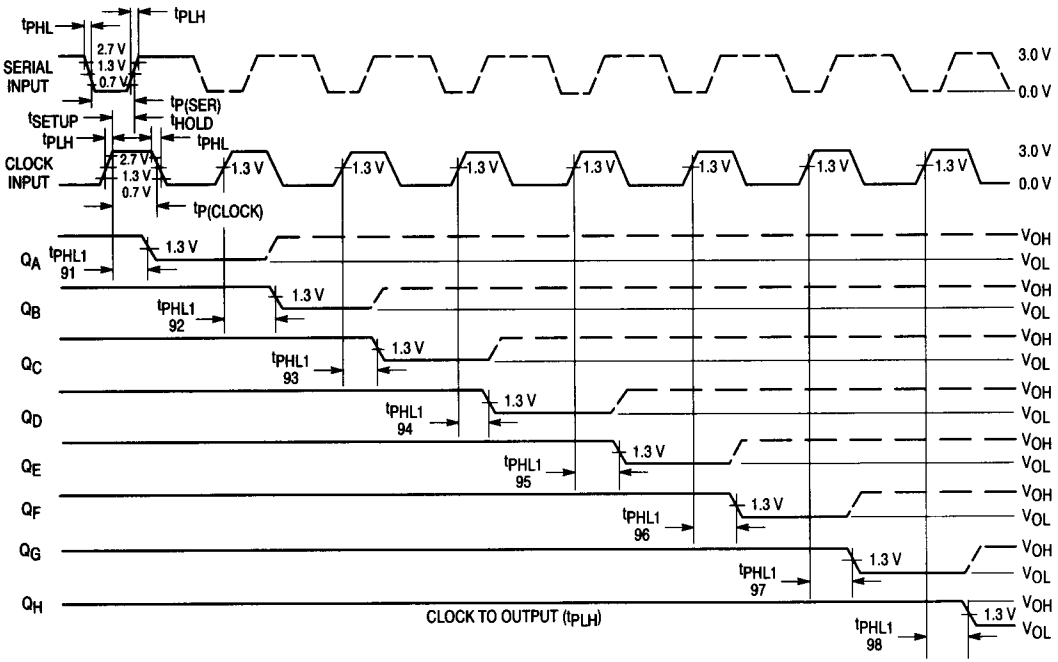
Each LOW-HIGH transition on the Clock (CLK) input shifts data one place to the right and enters into Q_A the Logical AND of the data inputs (A • B) that existed before the rising clock edge. A LOW level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

TEST CIRCUIT

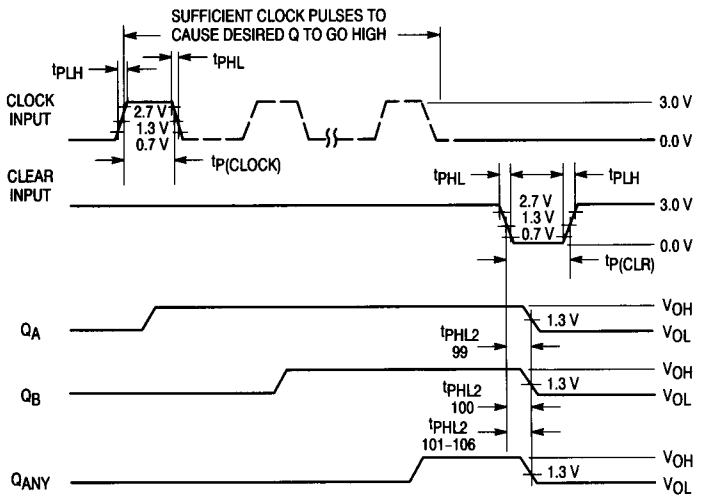


REFERENCE NOTES ON PAGE 5-202

CLOCK TO OUTPUT WAVEFORM



CLEAR TO OUTPUT WAVEFORM



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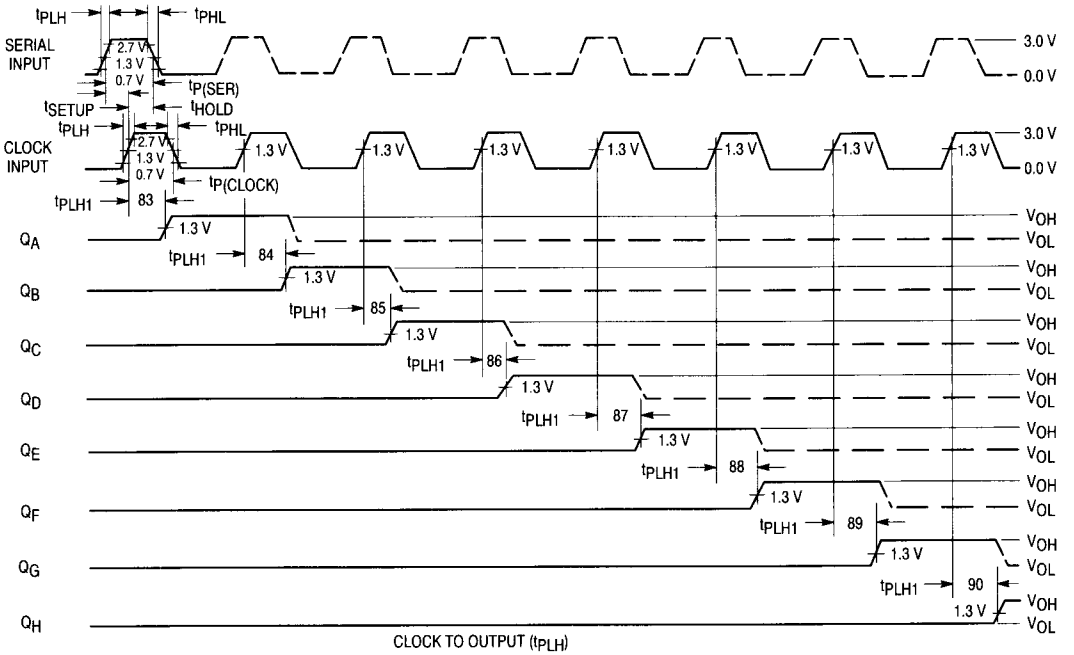
WAVEFORMS



NOTES:

1. Clock pulse characteristics:
   PRR ≤ 1.0 MHz, $t_{PLH} \leq 15$ ns, $t_{p(clock)} = 25$ ns.
2. Clear pulse characteristics:
   $t_{PLH} \leq 15$ ns, $t_{PHL} \leq 6.0$ ns, $t_{p(clear)} = 25$ ns.
3. Serial pulse characteristics:
   $t_{PLH} \leq 15$ ns, $t_{PHL} \leq 6.0$ ns, $t_{p(serial)} = 30$ ns, $t_{setup} = 20$ ns, $t_{hold} = 10$ ns.
4. $C_L = 50$ pF ± 10% including scope probe, wiring and stray capacitance without package in test fixture.
5. $R_L = 2.0$ kΩ ± 5.0%.
6. All diodes are 1N3064, 1N916, or equivalent.
7. Prior to initiating tests, the output shall be placed in the proper state.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −0.4 mA, CLR = 2.0 V, CLK = (See Notes 1-7), V_{IH} = 2.0 V (both inputs).
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, other inputs are open, CLK = open, CLR = 0.7 V.
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V (other inputs = GND).
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V (other inputs = GND).
I_{OS}	Output Short Circuit Current	−15	−100	−15	−100	−15	−100	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V (both inputs), CLR = 4.5 V, V_{OUT} = GND, CLK = (See Notes 1-7), CR = 4.5 V.
I_{IL}	Logical "0" Output Voltage	− 0.12	− 0.36	− 0.12	− 0.36	− 0.12	− 0.36	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs = 4.5 V.
I_{CC}	Power Supply Current Off		27		27		27	mA	V_{CC} = 5.5 V, V_{IN} = GND (both inputs), CLK = 5.5 V, CLR = (See Note 9).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output Clock to Q_n	5.0 —	37 32	5.0 —	56 51	5.0 —	56 51	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH1} t_{PLH1}	Propagation Delay /Data-Output Clock to Q_n	5.0 —	32 27	5.0 —	48 43	5.0 —	48 43	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL2} t_{PHL2}	Propagation Delay /Data-Output Clear to Q_n	5.0 —	41 36	5.0 —	62 57	5.0 —	62 57	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
f_{MAX} f_{MAX}	Maximum Clock Frequency	22 25		20		20		MHz	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.

NOTES:

1. One pulse minimum.
2. Two pulse minimum.
3. Three pulse minimum.
4. Four pulse minimum
5. Five pulse minimum.
6. Six pulse minimum.
7. Seven pulse minimum.
8. Eight pulse minimum.
9. 

10. The limits specified for C_L = 15 pF are guaranteed but not tested.

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