

256k SRAM - Radiation Hardened

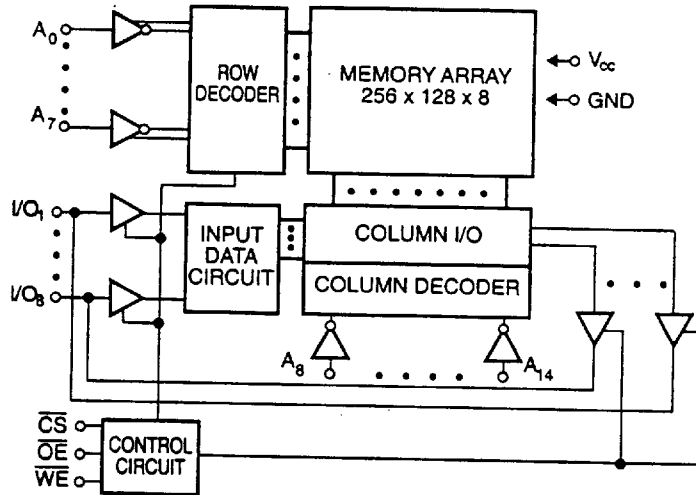
32C2568ERP

CMOS 32 k x 8 bit Static RAM

For Space Applications

SEI's 32C2568ERP (RP for RAD-PAK[®]) high density 32kword SRAM microcircuit features a minimum 100kilorad(Si) total dose tolerance. Using SEI's radiation hardened RAD-PAK[®]

packaging technology, the 32C2568ERP is fully equivalent to the commercial IDT 71256, which is a 32k x 8 SRAM. This device is a very low power CMOS static RAM. This advanced CMOS technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs. All bidirectional inputs and outputs of the 32C2568ERP are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation. An epitaxial layer is used for extra protection against heavy ions. Capable of surviving space environments, the 32C2568ERP is ideal for satellite, spacecraft, and space probe missions. The RAD-PAK[®] packaging technology incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing lifetime in orbit. The 32C2568ERP is available in Class B and S packaging and screening.

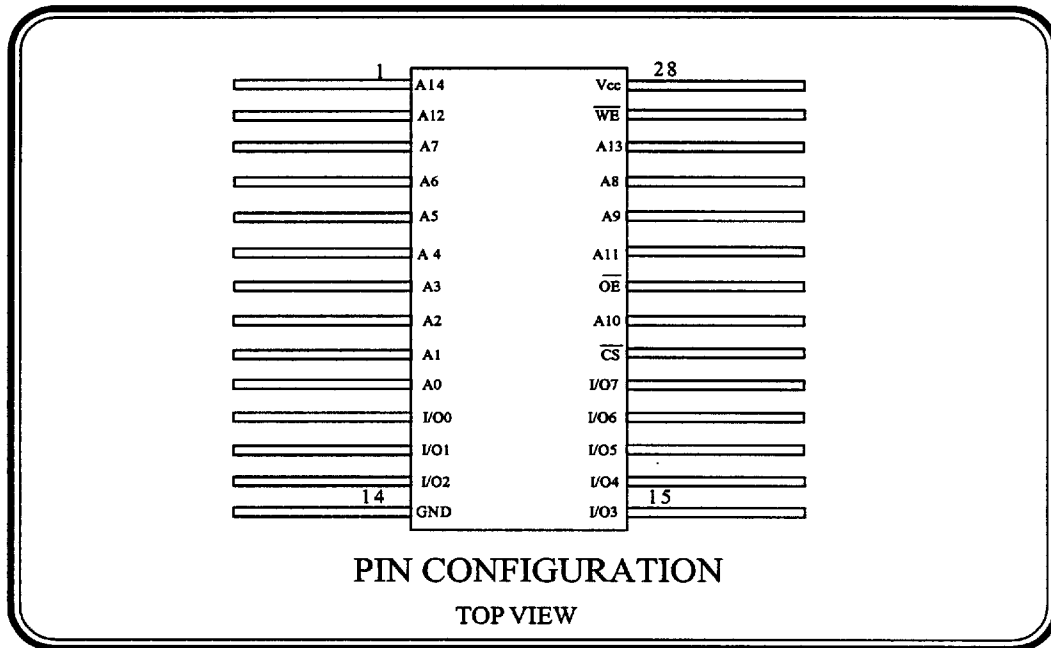


SPACE
ELECTRONICS
INCORPORATED

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Radiation Hardened 32C2568ERP

CMOS 28 Pin
32k x 8 bit Static RAM



Features:

- 32 kword x 8 bit Organization
- Pin Compatible with IDT 71256
- RAD-PAK® Radiation Hardened
Against Natural Space Radiation
- Total Dose Hardness >100 krad (Si)
- Package:
 - 28 Pin RAD-PAK® flat pack
(420 mils x 740 mils)
 - Weight - 6.0 grams
 - 28 Pin RAD-PAK® DIP
(1.490 mils x 610 mils)
 - Weight - 6.0 grams
- Fast Propagation Time:
 - 45, 55 ns Maximum Access Times.
- Completely Static Memory
 - No clock or timing strobe required
- High Speed Epi CMOS Technology
 - Single 5 Volt power supply
 - Equal access and cycle times
 - TTL compatible inputs and outputs
 - Very Low Power Consumption
 - One Chip Select plus one Output Enable pin
- Screening per TM 5004
- QCI per TM5005

Specifications and design are subject to change without notice.



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For Further Information Contact:

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32C2568ERP ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage to GND Potential	V_{CC}	-0.3	7.0	V
Input/Output Voltage Applied	V_{IO}	Gnd-0.3	$V_{CC}+0.3$	V
Storage Temperature	T_s	-65	+150	°C
Operating Temperature	T_A	-55	+125	°C

32C2568ERP RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V_{CC}	4.5	5.5	V
Ground	Gnd	0.0	0.0	V
Input Low Voltage <u>1/</u>	V_{IL}	-0.3	0.8	V
Input High Voltage <u>1/</u>	V_{IH}	2.2	$V_{CC}+0.3$	V

Note:

1/ $V_{IHmax}=V_{CC}+0.3V$, $V_{ILmin}=-0.3V$ or -1.0 pulse 50ns.

32C2568ERP CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input Capacitance <u>2/</u>	C_{in}		8	pF
Output Capacitance <u>2/</u>	C_{out}		8	pF

Note:

2/ $T_A=25^\circ C$, $f=1MHz$, $V_{CC}=5.0V$.



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32C2568ERP DC CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input Leakage Current ^{3/}	I_{IX}	-1.0	1.0	μA
Output Leakage Current ^{3/}	I_{OZ}	-1.0	1.0	μA
Output Low Voltage ^{4/}	V_{OL}		0.4	V
Output High Voltage ^{4/}	V_{OH}	2.4		V

Notes:

^{4/} $Gnd < V_{IN} < V_{CC}$, $Gnd < V_{OUT} < V_{CC}$ Output disabled.

^{4/} V_{CCmin} , $I_{OL}=4mA$, $I_{OH}=-1.0mA$.

32C2568ERP CONSUMPTION CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Standby Supply Current ^{5/} 32C2568ERPxx-45 32C2568ERPxx-55	I_{CCSB}		5 5	mA
Standby Supply Current ^{6/} 32C2568ERPxx-45 32C2568ERPxx-55	I_{CCSB1}		100 100	μA
Operating Supply Current ^{7/} 32C2568ERPxx-45 32C2568ERPxx-55	I_{CCOP}		70 70	mA

Notes:

^{5/} $CS \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$.

^{6/} $CS \geq V_{CC}-0.3V$, $I_{OUT}=0mA$. $V_{IN} \geq V_{CC}-0.3V$ or $V_{IN} \leq 0.3V$.

^{7/} V_{CCmax} , $I_{OUT}=0mA$, $V_{IN}=Gnd/V_{CC}$. Duty cycle 100%, $F=5MHz$, derating=10mA/MHz.

32C2568ERP DATA RETENTION MODE

32C2568ERP is designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip select (CS\) must be held high during data retention; within V_{CC} to $(V_{CC}-0.2V)$.
2. Output Enable (OE\) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. CS\ must be kept between $V_{CC}-0.3V$ and 70% of V_{CC} during the power up and power down transitions.
4. The RAM can begin operation > 45 ns after V_{CC} reaches the minimum operating voltage (4.5 V).



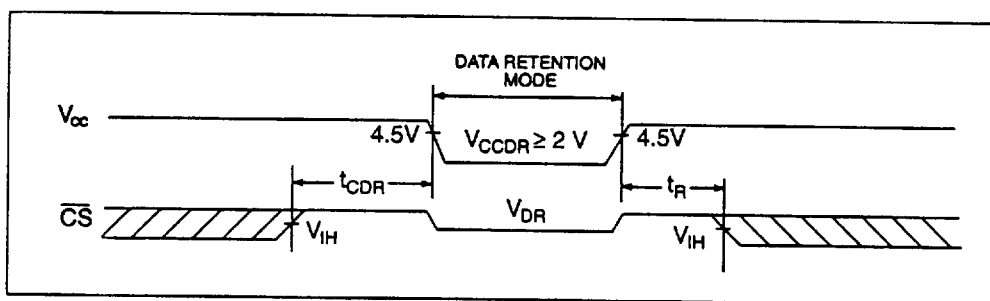
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TIMING



32C2568ERP DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNIT
V_{CC} for Data Retention	V_{CCDR}	2.0		V
Chip Deselect to Data Retention Time	T_{CDR}	0.0		ns
Operation Recovery Time	T_R	T_{AVAV} 8/		ns
Data Retention Current @2.0V	I_{CCDR1} 9/		80	uA
Data Retention Current @3.0v	I_{CCDR2} 9/		90	uA

Notes:

8/ T_{AVAV} =Read cycle time.

9/ $CS \setminus = V_{CC}$, $V_{IN} = Gnd/V_{CC}$, which is tested at $V_{CC} = 2V$.

32C2568ERP AC CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input Pulse Levels		GND	3.0	V
Input Rise			5	ns
Input Timing Reference Levels			1.5	V



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32C2568ERP WRITE CHARACTERISTICS 11/

PARAMETER	SYMBOL	MIN	MAX	UNIT
Write Cycle Time 32C2568ERPxx-45 32C2568ERPxx-55	T_{AVAV}	45 55		ns ns
Address Set-up Time 32C2568ERPxx-45 32C2568ERPxx-55	T_{AVWL}	0 0		ns ns
Address Valid to End of Write 32C2568ERPxx-45 32C2568ERPxx-55	T_{AVWH}	35 40		ns ns
Data Set-up Time 32C2568ERPxx-45 32C2568ERPxx-55	T_{DVWH}	25 25		ns ns
CS\ Low to Write End 32C2568ERPxx-45 32C2568ERPxx-55	T_{ELWH}	35 40		ns ns
Write Low to High Z 32C2568ERPxx-45 32C2568ERPxx-55	T_{WLQZ} 10/	15 20		ns ns
Write Pulse Width 32C2568ERPxx-45 32C2568ERPxx-55	T_{WLWH}	35 40		ns ns
Address Hold to End of Write 32C2568ERPxx-45 32C2568ERPxx-55	T_{WHAX}	0 0		ns ns
Data Hold Time 32C2568ERPxx-45 32C2568ERPxx-55	T_{WHDX}	0 0		ns ns
Write High to Low Z 32C2568ERPxx-45 32C2568ERPxx-55	T_{WHQX} 10/	0 0		ns ns



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32C2568ERP READ CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Read Cycle Time 32C2568ERPxx-45 32C2568ERPxx-55	T_{AVAV}	45 55		ns ns
Address Access Time 32C2568ERPxx-45 32C2568ERPxx-55	T_{AVQV}	45 55		ns ns
Address Valid to Low Z 32C2568ERPxx-45 32C2568ERPxx-55	T_{AVQX}	5 5		ns ns
Chip-select Access Time 32C2568ERPxx-45 32C2568ERPxx-55	T_{ELQV}	45 55		ns ns
CS\ Low to Low Z 32C2568ERPxx-45 32C2568ERPxx-55	T_{ELQX} 10/	5 5		ns ns
CS\ High to High Z 32C2568ERPxx-45 32C2568ERPxx-55	T_{EHQZ} 10/	20 20		ns ns
Output Enable Access Time 32C2568ERPxx-45 32C2568ERPxx-55	T_{GLQV}	20 25		ns ns
OE\ Low to Low Z 32C2568ERPxx-45 32C2568ERPxx-55	T_{GLQX} 10/	5 5		ns ns
OE\ High to High Z 32C2568ERPxx-45 32C2568ERPxx-55	T_{CHQZ} 10/	15 20		ns ns

Notes:

10/ Specified with $C_L=5pF$. Guaranteed but not tested.

11/ The internal write time of the memory is defined by the overlap of CS\LOW and W\LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

Data out is high impedance if OE\ = VIH.



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32C2568ERP PACKAGE ORDERING GUIDE

Package Style	Case Outline	1/	Description
D	D-28		28 Pin Dual In Line Package
F	F-28		28 Pin Flat Package

Note:

1/ For outline information, see Appendix A (Package Information - Outline Dimension)

32C2568ERP TRUTH TABLE

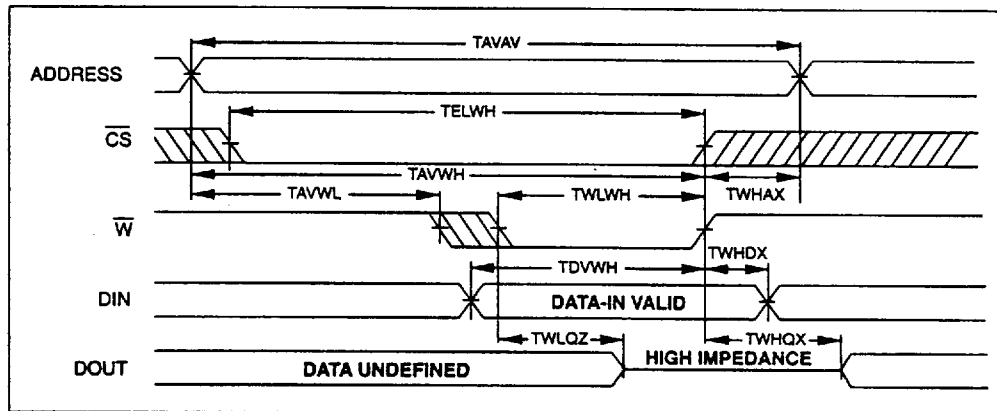
CS\	W\	OE\	INPUTS/OUTPUT	MODE
H	X	X	Z	Deselect/POWER-DOWN
L	H	L	DATA OUT	Read
L	L	X	DATA IN	Write
L	H	H	Z	Output Disable



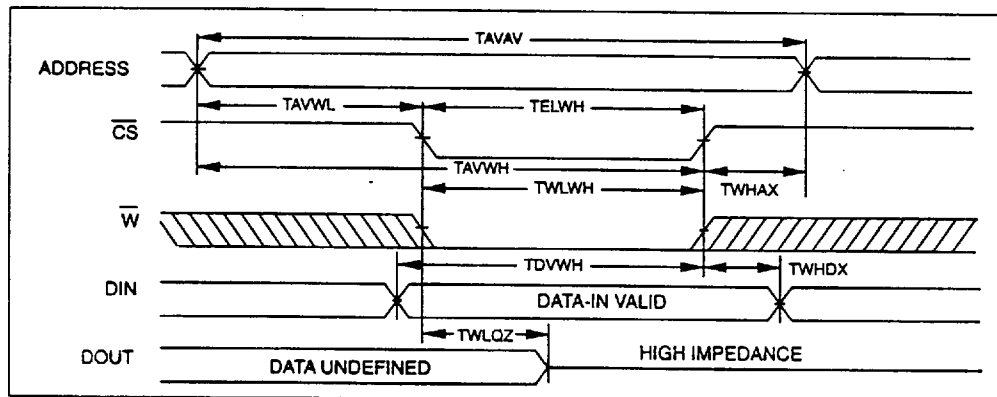
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32C2568ERP WRITE CYCLE 1: \overline{W} CONTROLLED 11/



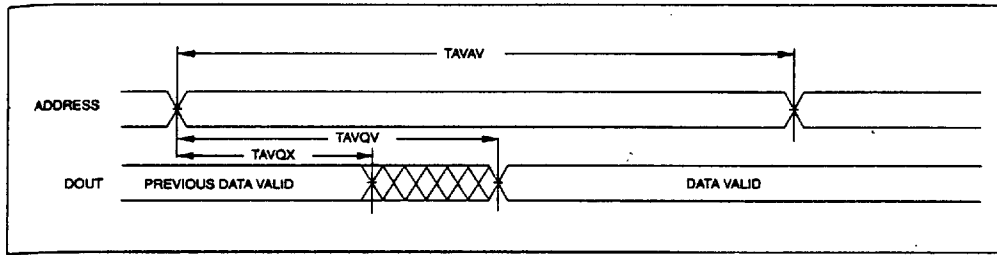
32C2568ERP WRITE CYCLE 2: CS-bar CONTROLLED 11/



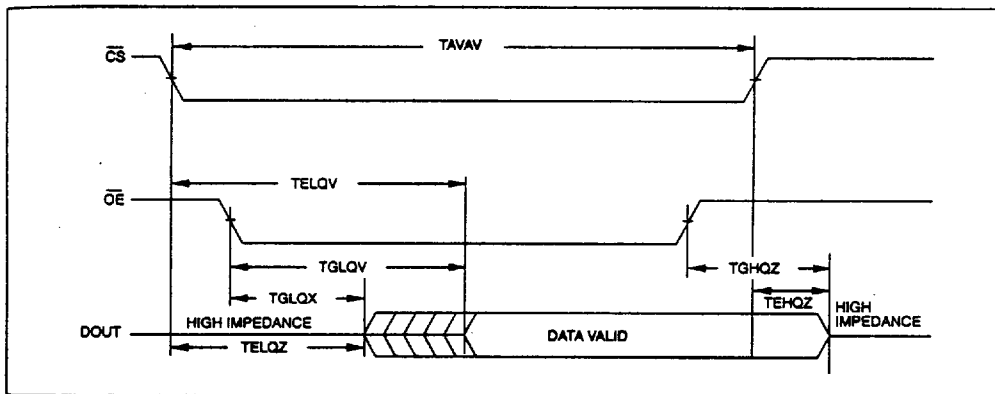
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32C2568ERP READ CYCLE nb1 13/ 14/



32C2568ERP READ CYCLE nb2 13/ 15/



Notes:

- 13/ W is high for read cycle.
- 14/ Device is continuously selected CS\ & OE\ = VIL.
- 15/ Address valid prior to or coincident with CS\ transition low.



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