

**DESCRIPTION**

The SSI 75T202 and 75T203 are complete Dual-Tone Multifrequency (DTMF) receivers detecting a selectable group of 12 or 16 standard digits. No front-end pre-filtering is needed. The only externally required components are an inexpensive 3.58-MHz television "colorburst" crystal (for frequency reference) and a bias resistor. Extremely high system density is made possible by using the clock output of a crystal-connected SSI 75T202 or 75T203 receiver to drive the time bases of additional receivers. Both are monolithic integrated circuits fabricated with low-power, complementary symmetry MOS (CMOS) processing. They require only a single low tolerance voltage supply and are packaged in a standard 18-pin plastic DIP.

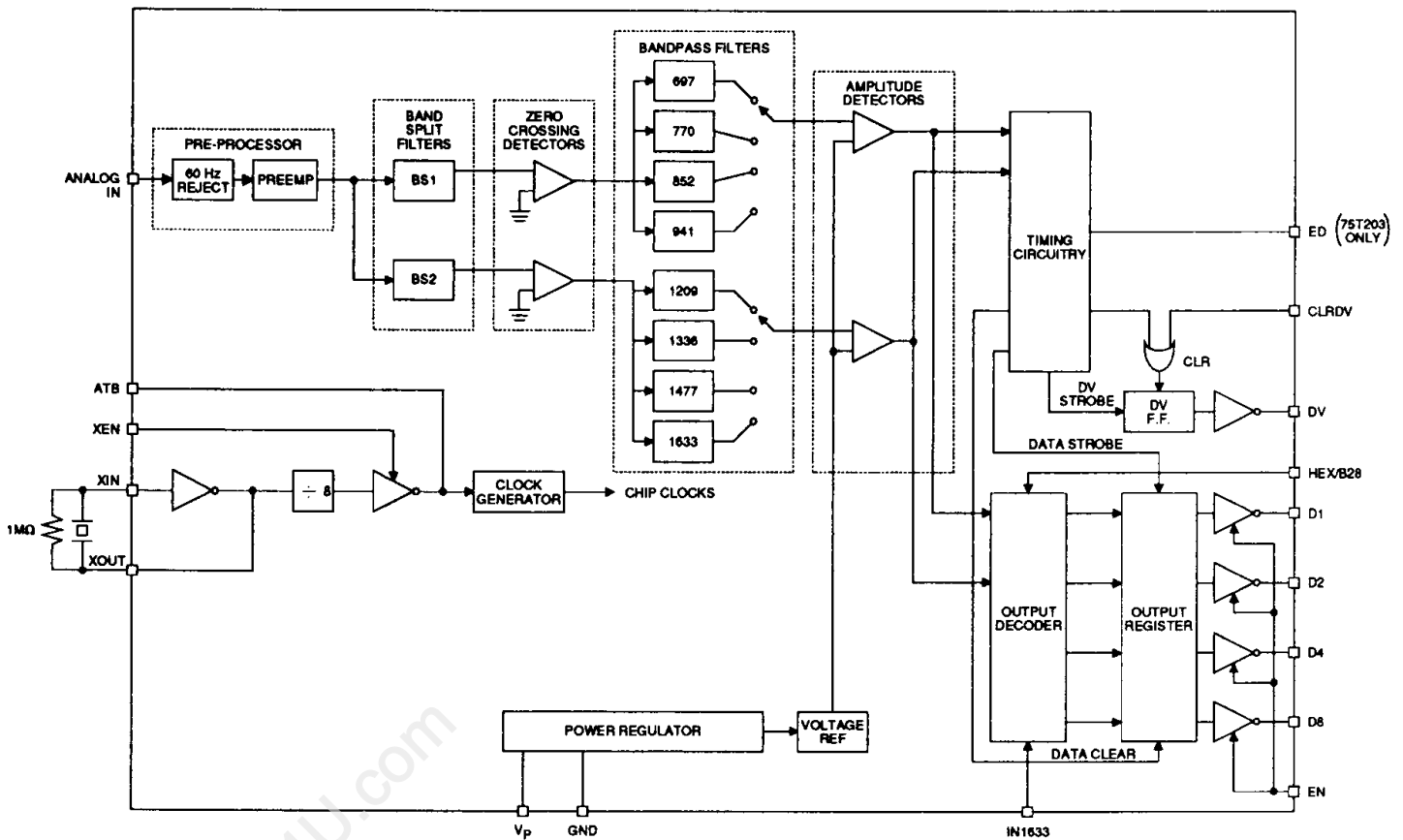
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**FEATURES**

- Central office quality
- NO front-end band-splitting filters required
- Single, low-tolerance, 5-volt supply
- Detects either 12 or 16 standard DTMF digits
- Uses inexpensive 3.579545-MHz crystal for reference
- Excellent speech immunity
- Output in either 4-bit hexadecimal code or binary coded 2-of-8
- 18-pin DIP package for high system density
- Synchronous or handshake interface
- Three-state outputs
- Early detect output (SSI 75T203 only)

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**BLOCK DIAGRAM**



CAUTION: Use handling procedures necessary for a static sensitive component.

# SSI 75T202/203

## 5V Low-Power DTMF Receiver

### DESCRIPTION (Continued)

The SSI 75T202 and 75T203 employ state-of-the-art circuit technology to combine digital and analog functions on the same CMOS chip using a standard digital semiconductor process. The analog input is pre-processed by 60-Hz reject and band splitting filters and then hard-limited to provide AGC. Eight bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. Outputs interface directly to standard CMOS circuitry, and are three-state enabled to facilitate bus-oriented architectures.

### ANALOG IN

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated in Figure 1.

The SSI 75T202 is designed to accept sinusoidal input wave forms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics less than -20 dB below the fundamental.

### CRYSTAL OSCILLATOR

The SSI 75T202 and 75T203 contain an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "colorburst" crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1 M $\Omega$  10% resistor is also connected between these pins. In this mode, ATB is a clock frequency output. Other SSI 75T202's (or 75T203's) may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively. Ten devices may run off a single crystal-connected SSI 75T202 or 75T203 as shown in Figure 2.

### HEX/B28

This pin selects the format of the digital output code. When HEX/B28 is tied high, the output is hexadecimal. When tied low, the output is binary coded 2-of-8. The table below describes the two output codes.

Hexadecimal					Binary Coded 2-of-8				
Digit	D8	D4	D2	D1	Digit	D8	D4	D2	D1
1	0	0	0	1	1	0	0	0	0
2	0	0	1	0	2	0	0	0	1
3	0	0	1	1	3	0	0	1	0
4	0	1	0	0	4	0	1	0	0
5	0	1	0	1	5	0	1	0	1
6	0	1	1	0	6	0	1	1	0
7	0	1	1	1	7	1	0	0	0
8	1	0	0	0	8	1	0	0	1
9	1	0	0	1	9	1	0	1	0
0	1	0	1	0	0	1	1	0	1
*	1	0	1	1	*	1	1	0	0
#	1	1	0	0	#	1	1	1	0
A	1	1	0	1	A	0	0	1	1
B	1	1	1	0	B	0	1	1	1
C	1	1	1	1	C	1	0	1	1
D	0	0	0	0	D	1	1	1	1

TABLE 1: Output Codes

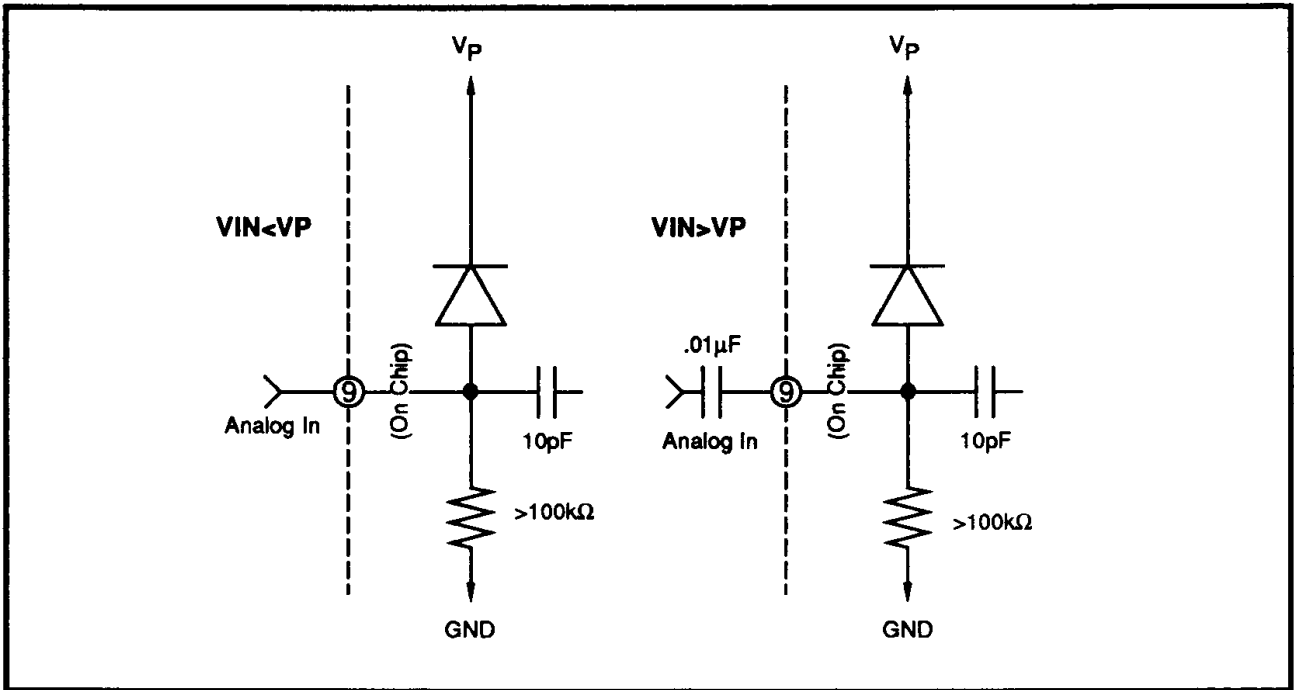


FIGURE 1: Input Coupling

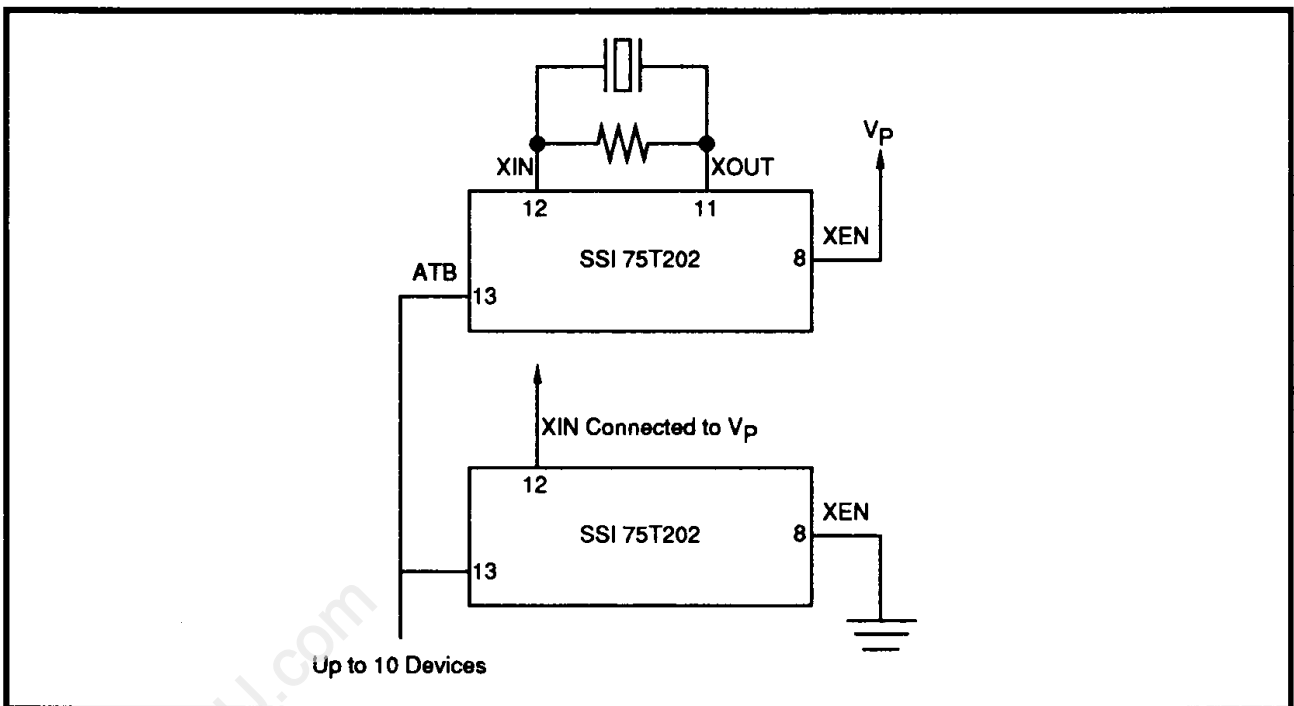


FIGURE 2: Crystal Connections

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#### IN1633

When tied high, this pin inhibits detection of tone pairs containing the 1633Hz component. For detection of all 16 standard digits, IN1633 must be tied low.

#### OUTPUTS D1, D2, D4, D8 and EN

Outputs D1, D2, D4, D8 are CMOS push-pull when enabled (EN high) and open circuited (high impedance) when disabled by pulling EN low. These digital outputs provide the code corresponding to the detected digit in the format programmed by the HEX/B28 pin. The digital outputs become valid after a tone pair has been detected and they are then cleared when a valid pause is timed.

#### DV and CLRDV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, and D8. DV remains high until a valid pause occurs or the CLRDV is raised high, whichever is earlier.

#### ED (SSI 75T203 only)

The ED output goes high as soon as the SSI 75T203 begins to detect a DTMF tone pair and falls when the 75T203 begins to detect a pause. The D1, D2, D4, and

D8 outputs are guaranteed to be valid when DV is high, but are not necessarily valid when ED is high.

#### N/C PINS

These pins have no internal connection and may be left floating.

#### DTMF DIALING MATRIX

See Figure 3. Please make note that column 3 is for special applications and is not normally used in telephone dialing.

	Col 0	Col 1	Col 2	Col 3
Row 0	1	2	3	A
Row 1	4	5	6	B
Row 2	7	8	9	C
Row 3	*	0	#	D

FIGURE 3: DTMF Dialing Matrix

#### DETECTION FREQUENCY

Low Group $f_0$	High Group $f_0$
Row 0 = 697 Hz	Column 0 = 1209 Hz
Row 1 = 770 Hz	Column 1 = 1336 Hz
Row 2 = 852 Hz	Column 2 = 1477 Hz
Row 3 = 941 Hz	Column 3 = 1633 Hz

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### DTMF Receiver

#### ABSOLUTE MAXIMUM RATINGS

(Operation above absolute maximum ratings may damage the device. All SSI 75T202/203 unused inputs must be connected to  $V_P$  or GND, as appropriate.)

PARAMETER	CONDITIONS	RATING
DC Supply Voltage - $V_P$		+7V
Operating Temperature		-40°C to +85°C Ambient
Storage Temperature		-65°C to +150°C
Power Dissipation (25°C)		65mW
Input Voltage	All inputs except ANALOG IN	( $V_P + .5V$ ) to $-.5V$
ANALOG IN Voltage		( $V_P + .5V$ ) to ( $V_P - 10V$ )
DC Current into any Input		$\pm 1.0mA$
Lead Temperature	Soldering, 10 sec.	300°C

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#### ELECTRICAL CHARACTERISTICS

(-40°C  $\leq T_A \leq$  +85°C,  $V_P = 5V \pm 10\%$ )

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Detect Bandwidth		$\pm(1.5+2Hz)$	$\pm 2.3$	$\pm 3.5$	% of $f_0$
Amplitude for Detection	each tone	-32		-2	dBm ref. to 600 $\Omega$
Twist Tolerance	Twist = $\frac{\text{High Tone}}{\text{Low Tone}}$	-10		+10	dB
60-Hz Tolerance				0.8	V <sub>rms</sub>
Dial Tone Tolerance	"precise" dial tone			0dB	dB*
Talk Off	MITEL tape #CM 7290		2		hits
Digital Outputs (except XOUT)	"0" level, 400 $\mu A$ load	0		0.5	V
	"1" level, 200 $\mu A$ load	$V_P - 0.5$		$V_P$	V
Digital Inputs	"0" level	0		0.3 $V_P$	V
	"1" level	0.7 $V_P$		$V_P$	V
Power Supply Noise	wide band			10	mV p-p
Supply Current	$T_A = 25^\circ C$		10	16	mA
Noise Tolerance	MITEL tape #CM 7290			-12	dB*
Input Impedance	$V_P \geq V_{IN} \geq V_P - 10$	100k $\Omega$    15pF			

\* dB referenced to lowest amplitude tone

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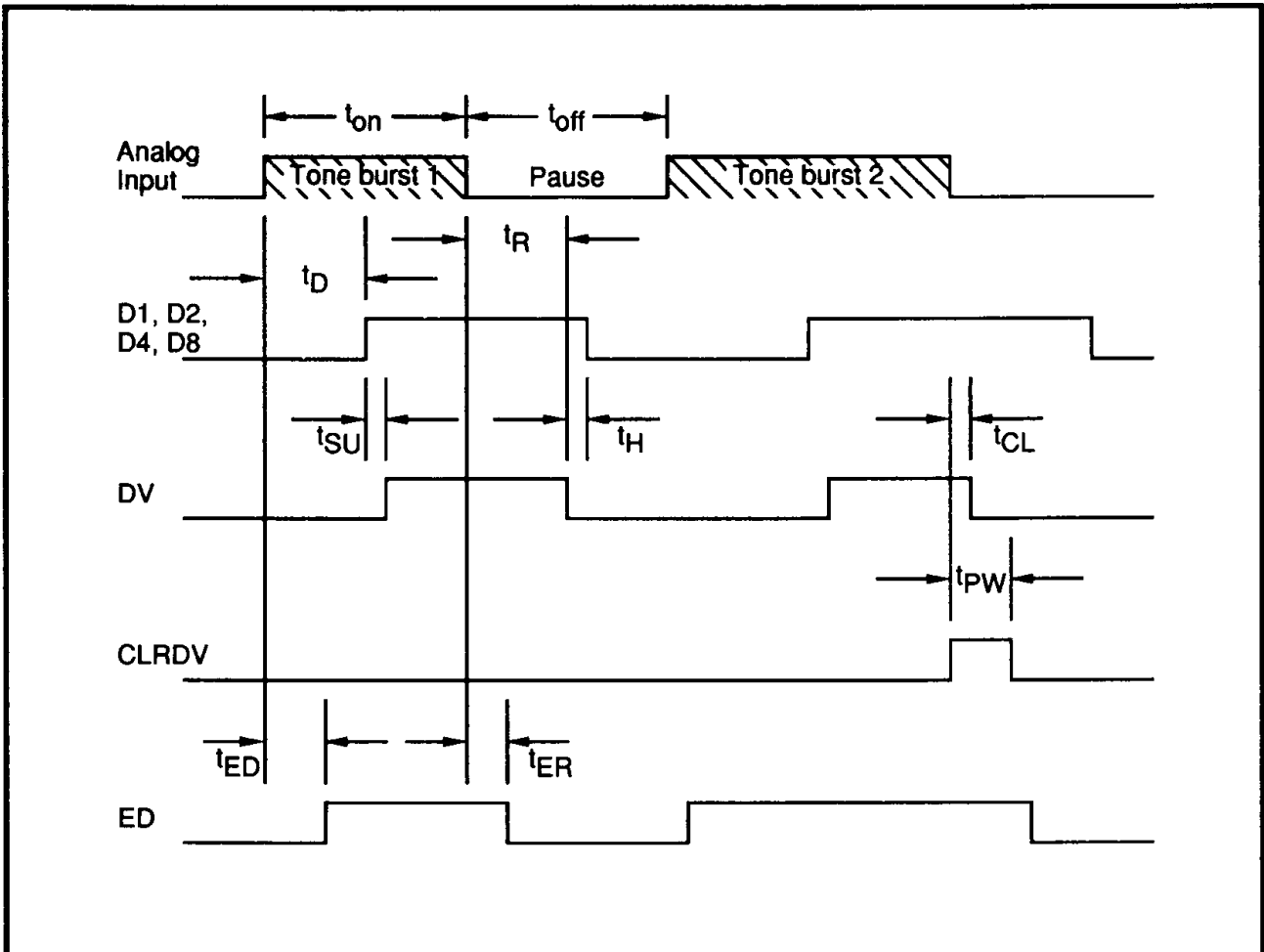
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### DTMF Receiver

#### SSI 75T202/203 TIMING

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
t <sub>ON</sub> Tone Time	for detection	40	-	-	ms
	for rejection	-	-	20	ms
t <sub>OFF</sub> Pause Time	for detection	40	-	-	ms
	for rejection	-	-	20	ms
t <sub>D</sub> Detect Time		25	-	46	ms
t <sub>R</sub> Release Time		35	-	50	ms
t <sub>SU</sub> Data Setup Time		7	-	-	μs
t <sub>H</sub> Data Hold Time		4.2	-	5.0	ms
t <sub>CL</sub> DV Clear Time		-	160	250	ns
t <sub>PW</sub> CLRDV Pulse Width		200	-	-	ns
t <sub>ED</sub> ED Detect Time		7	-	22	ms
t <sub>ER</sub> ED Release Time		2	-	18	ms
Output Enable Time	C <sub>L</sub> = 50pF, R <sub>L</sub> = 1kΩ	-	-	200	ns
Output Disable Time	C <sub>L</sub> = 35pF, R <sub>L</sub> = 500Ω	-	-	200	ns
Output Rise Time	C <sub>L</sub> = 50pF	-	-	200	ns
Output Fall Time	C <sub>L</sub> = 50pF	-	160	200	ns

SSI 75T202/203 TIMING (Continued)



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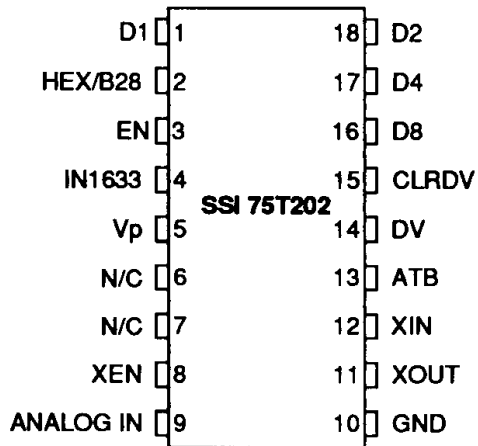
FIGURE 4: Timing Diagram

# SSI 75T202/203

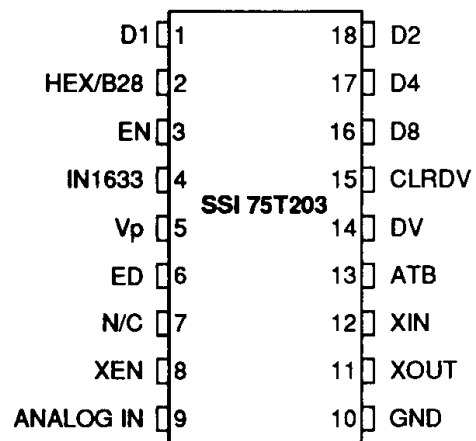
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## DTMF Receiver

### PACKAGE PIN DESIGNATIONS (TOP VIEW)



**18 - Pin DIP**  
**SSI 75T202**



**18 - Pin DIP**  
**SSI 75T203**

### ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T202 18-pin Plastic DIP	75T202-IP	75T202-IP
SSI 75T203 18-pin Plastic DIP	75T203-IP	75T203-IP

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Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX: (714) 573-6914