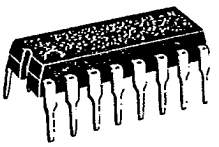
MN4022B / MN4022BS

4-Stage Divide-by-8 Johnson Counters

■ Description

The MN4022B/S are octal Johnson counters constructed with 4-stage D-type flip-flops.
The built-in decoder converts output to the coal number.
One output of 8 outputs ($O_0 \sim O_7$) becomes "H" by the count pulse added to CP_0 and $\overline{CP}_1$.
Count advances the count on the positive going edge of CP_0 at $\overline{CP}_1$ = "L" or on the negative going edge of $\overline{CP}_1$ at CP_0 = "H".
MR input of the "H" level resets counter to O_0 = "H" and $O_1 \sim O_7$ = "L" regardless of CP_0 and $\overline{CP}_1$.
The MN4022B/S are equivalent to MOTOROLA MC14022B and RCA CD4022B.

P-3



16-Pin • Plastic DIL Package

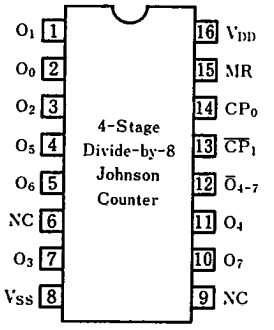
P-4

16-Pin • Panaflat Package (SO-16D)

■ Truth Table

MR	CP_0	$\overline{CP}_1$	Mode
H	×	×	$O_0=\overline{O}_{4\text{-}7}=H$, $O_1 \sim O_7=L$
L	H	↓	Counter Advance
L	↑	L	
L	L	×	No Change
L	×	H	
L	H	↑	
L	↓	L	

Pin Configuration



■ Maximum Ratings (Ta=25℃)

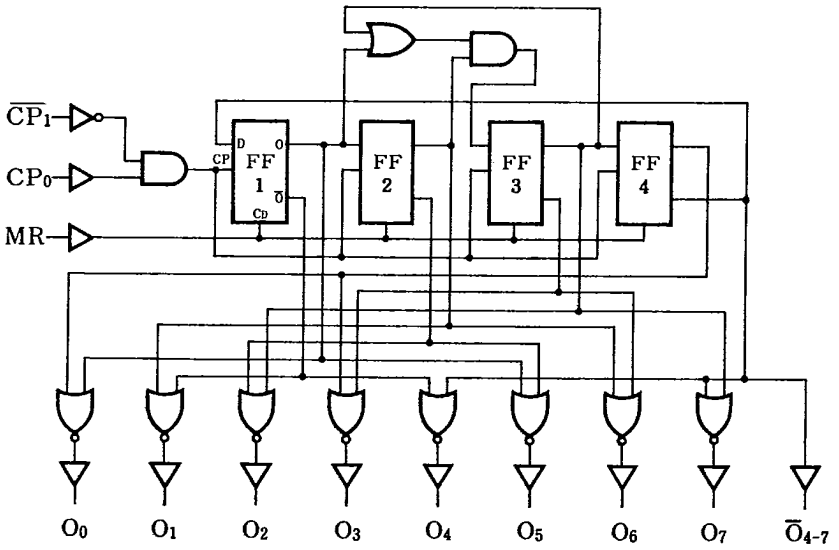
Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5~+18	V
Input Voltage		V_I	−0.5~V_{DD}+0.5*	V
Output Voltage		V_O	−0.5~V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40~+60℃	P_D	max. 400	mW
	Ta=+60~+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40~+85	℃
Storage Temperature		Tstg	−65~+150	℃

* V_{DD} + 0.5V should be under 18V

DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} $\lvert I_O\rvert$<1μA		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} $\lvert I_O\rvert$<1μA		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\lvert I_O\rvert$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\lvert I_O\rvert$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

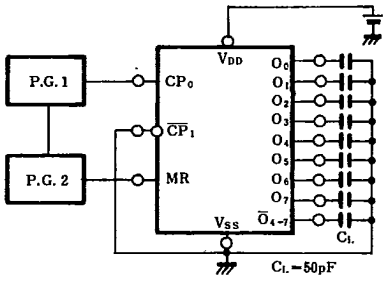
Logic Diagram



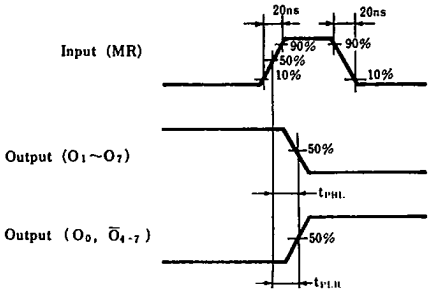
■ Switching Characteristics ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

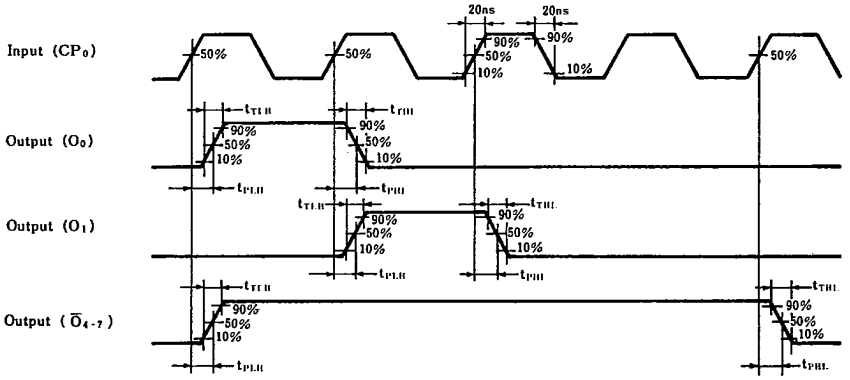
Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time $CP_0, \overline{CP}_1 \rightarrow On$ (H→L)	5	t_{PHL}	—	195	585	ns
	10		—	75	225	
	15		—	50	150	
Propagation Delay Time $CP_0, \overline{CP}_1 \rightarrow On$ (L→H)	5	t_{PLH}	—	245	735	ns
	10		—	95	285	
	15		—	60	180	
Propagation Delay Time $CP_0, \overline{CP}_1 \rightarrow \overline{O}_{4-7}$ (H→L)	5	t_{PHL}	—	245	735	ns
	10		—	90	270	
	15		—	60	180	
Propagation Delay Time $CP_0, \overline{CP}_1 \rightarrow \overline{O}_{4-7}$ (L→H)	5	t_{PLH}	—	190	570	ns
	10		—	75	225	
	15		—	50	150	
Propagation Delay Time $MR \rightarrow O_1$ to O_7 (H→L)	5	t_{PHL}	—	130	390	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time $MR \rightarrow O_0$ (L→H)	5	t_{PLH}	—	130	390	ns
	10		—	55	165	
	15		—	40	120	
Propagation Delay Time $MR \rightarrow \overline{O}_{4-7}$ (L→H)	5	t_{PLH}	—	110	330	ns
	10		—	45	135	
	15		—	35	105	
Hold Time $CP_0 \rightarrow \overline{CP}_1$	5	t_{hold}	—	70	210	ns
	10		—	25	75	
	15		—	15	45	
Hold Time $\overline{CP}_1 \rightarrow CP_0$	5	t_{hold}	—	85	255	ns
	10		—	30	90	
	15		—	20	60	
Minimum Clock Pulse Width	5	t_{WCP}	—	35	105	ns
	10		—	15	45	
	15		—	10	30	
Minimum Reset Pulse Width	5	t_{WMRH}	—	35	105	ns
	10		—	15	45	
	15		—	10	30	
Reset Recovery Time	5	t_{RMR}	—	10	30	ns
	10		—	5	15	
	15		—	5	15	
Maximum Clock Frequency	5	fmax	3	6	—	ns
	10		8	16	—	
	15		12	24	—	
Input Capacitance		C_I	—	—	7.5	pF

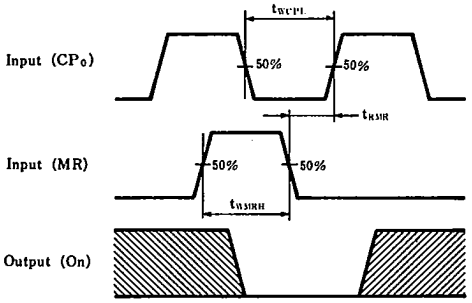
1. Switching Time Test Circuit



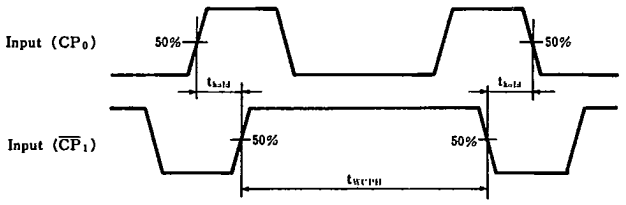
2. Waveforms







Waveforms showing recovery time for MR; minimum CP_0 and MR pulse widths
Conditions: $\overline{CP}_1$ = LOW while CP_0 is triggered on a LOW to HIGH transition.
t_{WCP} and t_{RMR} also apply when CP_0 = HIGH and $\overline{CP}_1$ is triggered on a HIGH to LOW transition



Waveforms showing hold times for CP_0 to $\overline{CP}_1$ and $\overline{CP}_1$ to CP_0
Hold times are shown as positive values, but may be specified as negative values.

Timing Diagram