

3.3V 1M × 64-Bit EDO-DRAM Module 3.3V 1M x 72-Bit EDO-DRAM Module

HYM64V1005GU-50/-60/-70
HYM72V1005GU-50/-60/-70

168pin unbuffered DIMM Module with serial presence detect

Preliminary Information

- 168 Pin JEDEC Standard, Unbuffered 8 Byte Dual In-Line Memory Module
- 1 bank 1M x 64, 1M x 72 organisation
- Optimized for byte-write non-parity or ECC applications
- Extended Data Out (EDO)
- Performance:

		-50	-60	-70
tRAC	RAS Access Time	50 ns	60 ns	70 ns
tCAC	CAS Access Time	13 ns	15 ns	20 ns
tAA	Access Time from Address	25 ns	30 ns	35 ns
tRC	Cycle Time	84 ns	104 ns	124 ns
tHPC	EDO Mode Cycle Time	20 ns	25 ns	30 ns

- Single +3.3 V ± 0.3 V Power Supply
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ -only-refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs and clocks are fully LV-TTL compatible
- Serial presence detects (optional)
- Utilizes four 1M × 16 -DRAMs in TSOPII-50/44 and two 1M x 4 - DRAMs in SOJ 26/20 packages
- 1024 refresh cycles / 16 ms with 10 / 10 addressing (Row / Column)
- Gold contact pad
- Card Size: 133,35mm x 25,40 mm x 5,30 mm
- This DRAM product module family is intended to be fully pin and architecture compatible with the 168pin unbuffered SDRAM DIMM module family

The HYM64(72)V1005GU-50/-60/-70 are industry standard 168-pin 8-byte Dual In-Line Memory Module (DIMMs) which are organized as 1M x 64 and 1M x 72 high speed memory arrays designed with EDO DRAMs for non-parity and ECC applications. The DIMMs use four 1M x 16 EDO DRAMs for the 1M x 64 organisation and additional two 1M x 4 DRAMs for the 1M x 72 organisation. Decoupling capacitors are mounted on the PC board.

The DIMMs use optional serial presence detects implemented via a serial E²PROM using the two pin I²C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes of serial PD data are available to the customer.

All 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 133,35 mm long space-saving footprint.

Ordering Information

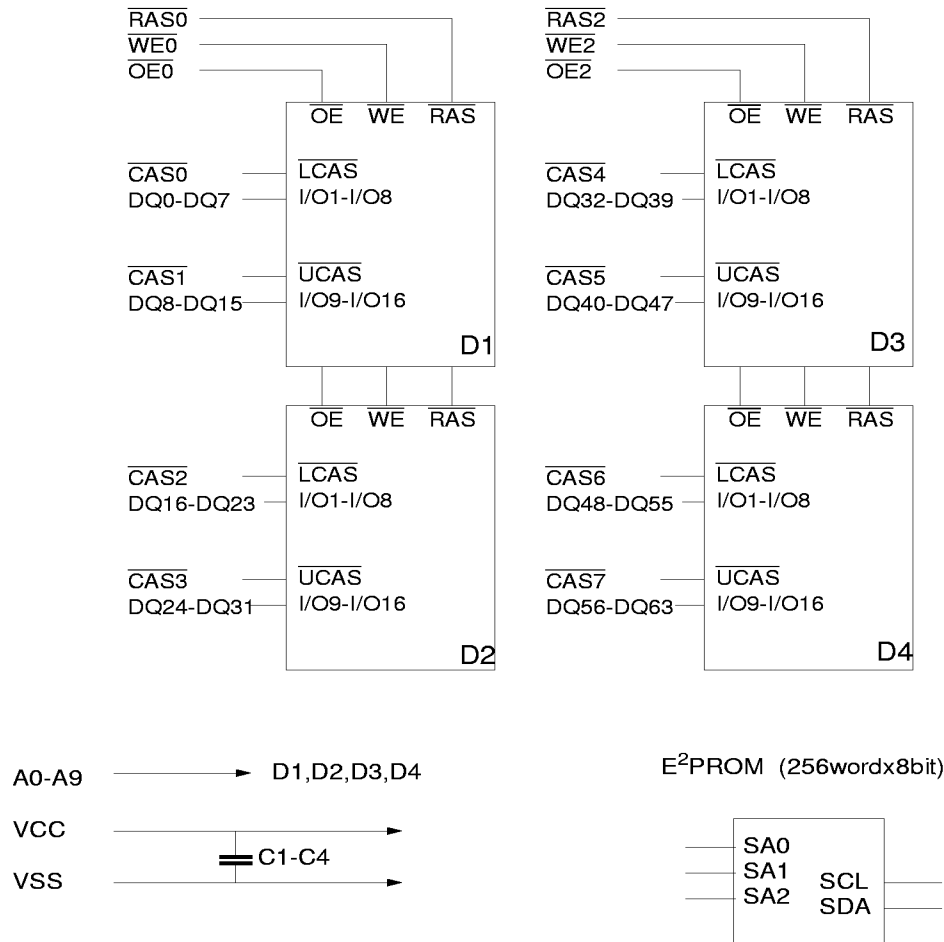
Type	Ordering Code	Package	Descriptions
HYM 64V1005GU-50	Q67100-Q2176	L-DIM-168-10	1M x 64 DRAM module (access time 50 ns)
HYM 64V1005GU-60	Q67100-Q2177	L-DIM-168-10	1M x 64 DRAM module (access time 60 ns)
HYM 64V1005GU-70		L-DIM-168-10	1M x 64 DRAM module (access time 70 ns)
HYM 72V1005GU-50	Q67100-Q2178	L-DIM-168-10	1M x 72 DRAM module (access time 50 ns)
HYM 72V1005GU-60	Q67100-Q2179	L-DIM-168-10	1M x 72 DRAM module (access time 60 ns)
HYM 72V1005GU-70		L-DIM-168-10	1M x 72 DRAM module (access time 70 ns)

Pin Names

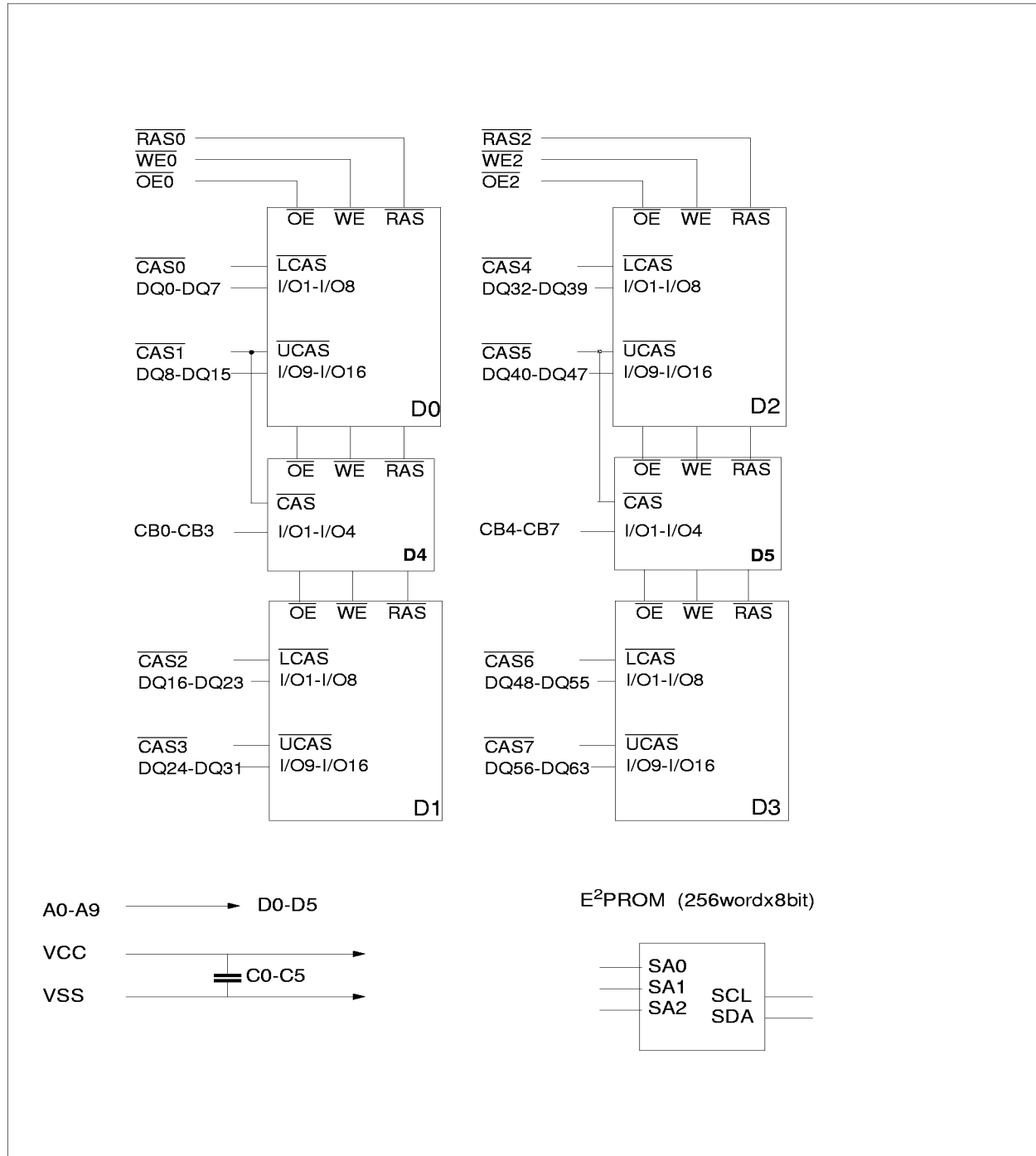
A0-A9	Address Input
DQ0 - DQ63	Data Input/Output
CB0-CB7	Check Bit Data Input/Output (x72 only)
RAS0, RAS2	Row Address Strobe
CAS0 - CAS7	Column Address Strobe
WE0, WE2	Read / Write Input
OE0, OE2	Output Enable
Vcc	Power (+3.3 Volt)
Vss	Ground
SCL	Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
SA0-SA2	Serial Presence Detect Addresses
N.C.	No Connection
DU	Don't use

Pin Configuration

PIN #	Symbol	PIN #	Symbol	PIN #	Symbol	PIN #	Symbol
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	OE2	86	DQ32	128	DU
3	DQ1	45	RAS2	87	DQ33	129	NC
4	DQ2	46	CAS2	88	DQ34	130	CAS6
5	DQ3	47	CAS3	89	DQ35	131	CAS7
6	VCC	48	WE2	90	VCC	132	DU
7	DQ4	49	VCC	91	DQ36	133	VCC
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB3	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VCC	101	DQ45	143	VCC
18	VCC	60	DQ20	102	VCC	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	DU	104	DQ47	146	DU
21	CB0	63	NC	105	CB4	147	NC
22	CB1	64	VSS	106	CB5	148	VSS
23	VSS	65	DQ21	107	VSS	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VCC	68	VSS	110	VCC	152	VSS
27	WE0	69	DQ24	111	DU	153	DQ56
28	CAS0	70	DQ25	112	CAS4	154	DQ57
29	CAS1	71	DQ26	113	CAS5	155	DQ58
30	RAS0	72	DQ27	114	NC	156	DQ59
31	OE0	73	VCC	115	DU	157	VCC
32	VSS	74	DQ28	116	VSS	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	NC	121	A9	163	NC
38	NC	80	NC	122	NC	164	NC
39	NC	81	NC	123	NC	165	SA0
40	VCC	82	SDA	124	VCC	166	SA1
41	VCC	83	SCL	125	DU	167	SA2
42	DU	84	VCC	126	DU	168	VCC



1M x 64 DIMM Module Block Diagram



1M x 72 DIMM Module Block Diagram

TRUTH TABLE

FUNCTION		$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	WRITE	$\overline{\text{OE}}$	ROW ADDR	COL ADDR	DQ0-DQ63
Standby		H	X	X	X	X	X	High Impedance
Read		L	L	H	L	ROW	COL	Data Out
Early-Write		L	L	L	X	ROW	COL	Data In
Late-Write		L	L	H - L	H	ROW	COL	Data In
Read-Modify-Write (RMW)		L	L	H - L	L - H	ROW	COL	Data Out, Data In
EDO Page Mode Read	1st Cycle	L	H - L	H	L	ROW	COL	Data Out
	2nd Cycle	L	H - L	H	L	n/a	COL	Data Out
EDO Page Mode Write	1st Cycle	L	H - L	L	X	ROW	COL	Data In
	2nd Cycle	L	H - L	L	X	n/a	COL	Data In
EDO Page Mode RMW	1st Cycle	L	H - L	H - L	L - H	ROW	COL	Data Out, Data In
	2st Cycle	L	H - L	H - L	L - H	n/a	COL	Data Out, Data In
$\overline{\text{RAS}}$ only refresh		L	H	X	X	ROW	n/a	High Impedance
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh		H - L	L	H	X	X	n/a	High Impedance
Hidden Refresh	READ	L-H-L	L	H	L	ROW	COL	Data Out
	WRITE	L-H-L	L	L	X	ROW	COL	Data In
Self Refresh		H - L	L	H	X	X	X	High Impedance

Absolute Maximum Ratings

Operating temperature range	0 to + 70 °C
Storage temperature range.....	– 55 to + 125 °C
Input/output voltage	–0.5 to min (V _{CC} +0.5, 4.6) V
Power supply voltage.....	–0.5 to 4.6 V
Power dissipation.....	4.42 W
Data out current (short circuit)	50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = 0$ to 70 °C; $V_{CC} = 3.3$ V $\pm$ 0.3 V

Parameter	Symbol	x 64/ x72		Unit	Notes
		min.	max.		
Input high voltage	V_{IH}	2.0	$V_{CC} + 0.5$	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
Output high voltage (LVTTL) Output „H“ level voltage ($I_{OUT} = - 2$ mA)	V_{OH}	2.4	–	V	1)
Output low voltage (LVTTL) Output „L“ level voltage ($I_{OUT} = + 2$ mA)	V_{OL}	–	0.4	V	1)
Output high voltage (LVCMOS) Output „H“ level voltage ($I_{OUT} = - 100\mu A$)	V_{OH}	$V_{CC}-0.2$	–	V	1)
Output low voltage (LVCMOS) Output „L“ level voltage ($I_{OUT} = +100 \mu A$)	V_{OL}	–	0.4	V	1)
Input leakage current ($0 V < V_{IN} < V_{CC}$, all other pins = 0 V)	$I_{I(L)}$	– 10	10	μA	1)
Output leakage current (DO is disabled, $0 V < V_{OUT} < V_{CC}$)	$I_{O(L)}$	– 10	+10	μA	1)

DC Characteristics (cont'd)

$T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$; $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$

Parameter	Symbol	x 64		x 72		Unit	Notes
		min.	max.	min.	max.		
Average V_{CC} supply current: -50 version -60 version -70 version ($\overline{\text{RAS}}, \overline{\text{CAS}}$, address cycling, $t_{RC} = t_{RC} \text{ min.}$)	I_{CC1}	—	800 720 640	—	940 840 750	mA mA mA	2) 3) 4)
Standby V_{CC} supply current ($\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$, one address change)	I_{CC2}	—	16	—	18	mA	—
Average V_{CC} supply current during $\overline{\text{RAS}}$ only refresh cycles: -50 version -60 version -70 version ($\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH}$, $t_{RC} = t_{RC} \text{ min.}$)	I_{CC3}	—	800 720 640	—	940 840 750	mA mA mA	2) 4)
Average V_{CC} supply current during hyper page mode (EDO): -50 version -60 version -70 version ($\overline{\text{RAS}} = V_{IL}$, $\overline{\text{CAS}}$, address cycling $t_{PC} = t_{PC} \text{ min.}$)	I_{CC4}	—	360 300 240	—	500 420 350	mA mA mA	2) 3) 4)
Standby V_{CC} supply current ($\overline{\text{RAS}} = \overline{\text{CAS}} = V_{CC} - 0.2 \text{ V}$, one address change)	I_{CC5}	—	8	—	9	mA	—
Average V_{CC} supply current during $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh mode: -50 version -60 version -70 version ($\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling, $t_{RC} = t_{RC} \text{ min.}$)	I_{CC6}	—	800 720 640	—	940 840 750	mA mA mA	2) 4)

AC Characteristics ⁵⁾⁶⁾

16E

 $T_A = 0 \text{ to } 70 \text{ } ^\circ\text{C}, V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, t_T = 2 \text{ ns}$

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		

common parameters

Random read or write cycle time	t_{RC}	84	—	104	—	124	—	ns	
$\overline{\text{RAS}}$ precharge time	t_{RP}	30	—	40	—	50	—	ns	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	50	10k	60	10k	70	10k	ns	
$\overline{\text{CAS}}$ pulse width	t_{CAS}	8	10k	10	10k	12	10k	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	8	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	8	—	10	—	12	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}	12	37	14	45	14	53	ns	
$\overline{\text{RAS}}$ to column address delay	t_{RAD}	10	25	12	30	12	35	ns	
$\overline{\text{RAS}}$ hold time	t_{RSH}	13		15	—	17	—	ns	
$\overline{\text{CAS}}$ hold time	t_{CSH}	40		50	—	60	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	5	—	5	—	5	—	ns	
Transition time (rise and fall)	t_T	1	50	1	50	1	50	ns	7
Refresh period	t_{REF}	—	16	—	16	—	16	ms	

Read Cycle

Access time from $\overline{\text{RAS}}$	t_{RAC}	—	50	—	60	—	70	ns	8, 9
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	13	—	15	—	17	ns	8, 9
Access time from column address	t_{AA}	—	25	—	30	—	35	ns	8,10
$\overline{\text{OE}}$ access time	t_{OEA}	—	13	—	15	—	17	ns	
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	25	—	30	—	35	—	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	ns	11
Read command hold time referenced to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	0	—	ns	11
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	0	—	0	—	0	—	ns	8
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	17	ns	12
Output turn-off delay from $\overline{\text{OE}}$	t_{OEZ}	0	13	0	15	0	17	ns	12

AC Characteristics (cont'd) ⁵⁾⁶⁾

16E

 $T_A = 0 \text{ to } 70 \text{ } ^\circ\text{C}, V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, t_T = 2 \text{ ns}$

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		
Data to $\overline{\text{CAS}}$ low delay	t_{DZC}	0	—	0	—	0	—	ns	13
Data to $\overline{\text{OE}}$ low delay	t_{DZO}	0	—	0	—	0	—	ns	13
$\overline{\text{CAS}}$ high to data delay	t_{CDD}	10	—	13	—	15	—	ns	14
$\overline{\text{OE}}$ high to data delay	t_{ODD}	10	—	13	—	15	—	ns	14

Write Cycle

Write command hold time	t_{WCH}	8	—	10	—	10	—	ns	
Write command pulse width	t_{WP}	8	—	10	—	10	—	ns	
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	15
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	13	—	15	—	17	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	13	—	15	—	17	—	ns	
Data setup time	t_{DS}	0	—	0	—	0	—	ns	16
Data hold time	t_{DH}	8	—	10	—	12	—	ns	16

Read-modify-Write Cycle

Read-write cycle time	t_{RWC}	113	—	138	—	162	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t_{RWD}	64	—	77	—	89	—	ns	15
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	t_{CWD}	27	—	32	—	36	—	ns	15
Column address to $\overline{\text{WE}}$ delay time	t_{AWD}	39	—	47	—	54	—	ns	15
$\overline{\text{OE}}$ command hold time	t_{OEh}	10	—	13	—	15	—	ns	

Hyper Page Mode (EDO) Cycle

Hyper page mode (EDO) cycle time	t_{HPC}	20	—	25	—	30	—	ns	
$\overline{\text{CAS}}$ precharge time	t_{CP}	8	—	10	—	10	—	ns	
Access time from $\overline{\text{CAS}}$ precharge	t_{CPA}	—	27	—	32	—	37	ns	7
Output data hold time	t_{COH}	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ pulse width in EDO mode	t_{RAS}	50	200k	60	200k	70	200k	ns	
$\overline{\text{CAS}}$ precharge to $\overline{\text{RAS}}$ Delay	t_{RHPC}	27	—	32	—	37	—	ns	

AC Characteristics (cont'd) ⁵⁾⁶⁾

16E

 $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}, V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}, t_T = 2 \text{ ns}$

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		

Hyper Page Mode (EDO) Read-modify-Write Cycle

Hyper page mode (EDO) read-write cycle time	t_{PRWC}	58	—	68	—	77	—	ns	
CAS precharge to $\overline{WE}$	t_{CPWD}	41	—	49	—	56	—	ns	

$\overline{CAS}$ -before- $\overline{RAS}$ Refresh Cycle

CAS setup time	t_{CSR}	10	—	10	—	10	—	ns	
CAS hold time	t_{CHR}	10	—	10	—	10	—	ns	
RAS to $\overline{CAS}$ precharge time	t_{RPC}	5	—	5	—	5	—	ns	
Write to $\overline{RAS}$ precharge time	t_{WRP}	10	—	10	—	10	—	ns	
Write hold time referenced to $\overline{RAS}$	t_{WRH}	10	—	10	—	10	—	ns	

Capacitance

 $T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}; V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}; f = 1 \text{ MHz}$

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input Capacitance (A0 to A9)	C_{I1}	—	55	pF
Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{I2}	—	50	pF
Input Capacitance ($\overline{CAS0}$ - $\overline{CAS7}$)	C_{I3}	—	10	pF
Input Capacitance ($\overline{WE0}$, $\overline{WE2}$, $\overline{OE0}$, $\overline{OE2}$)	C_{I4}	—	50	pF
I/O Capacitance (DQ0-DQ63, CB0-CB8)	C_{IO1}	—	11	pF
Input Capacitance (SCL, SA0-2)	C_s	—	8	pF
Input/Output Capacitance (SDA)	C_s	—	10	pF

Notes:

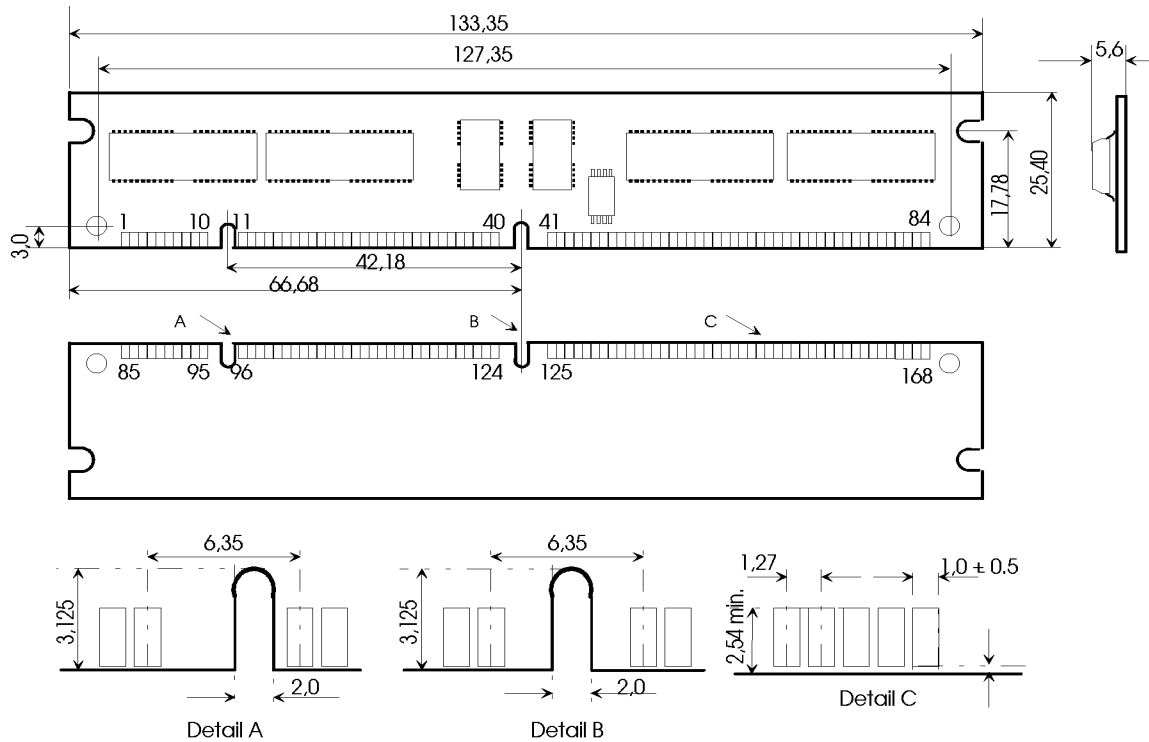
- 1) All voltages are referenced to V_{SS} .
- 2) I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} depend on cycle rate.
- 3) I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
- 4) Address can be changed once or less while $RAS = V_{il}$. In case of ICC4 it can be changed once or less during a hyper page mode (EDO) cycle
- 5) An initial pause of 200 μs is required after power-up followed by 8 RAS cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS cycles are required.
- 6) AC measurements assume $t_T = 2 \text{ ns}$.
- 7) $V_{IH (min.)}$ and $V_{IL (max.)}$ are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL} .
- 8) Measured with the specified current load and 100 pF at $V_{ol} = 0.8 \text{ V}$ and $V_{oh} = 2.0 \text{ V}$. Access time is determined by the latter of t_{RAC} , t_{CAC} , t_{AA} , t_{CPA} , t_{OEA} . t_{CAC} is measured from tristate.
- 9) Operation within the $t_{RCD (max.)}$ limit ensures that $t_{RAC (max.)}$ can be met. $t_{RCD (max.)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD (max.)}$ limit, then access time is controlled by t_{CAC} .
- 10) Operation within the $t_{RAD (max.)}$ limit ensures that $t_{RAC (max.)}$ can be met. $t_{RAD (max.)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD (max.)}$ limit, then access time is controlled by t_{AA} .
- 11) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- 12) $t_{OFF (max.)}$, $t_{OEZ (max.)}$ define the time at which the output achieves the open-circuit conditions and are not referenced to output voltage levels. t_{OFF} is referenced from the rising edge of RAS or CAS, whichever occurs last.
- 13) Either t_{DZC} or t_{DZO} must be satisfied.
- 14) Either t_{CDD} or t_{ODD} must be satisfied.
- 15) t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS (min.)}$, the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle; if $t_{RWD} > t_{RWD (min.)}$, $t_{CWD} > t_{CWD (min.)}$ and $t_{AWD} > t_{AWD (min.)}$, the cycle is a read-write cycle and I/O will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of I/O (at access time) is indeterminate.
- 16) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.

Serial Presence Detects:

A serial presence detect storage device -- EEPROM 24C02 -- is assembled on to the module. Information about the modul confuguration, speed, etc. is written into the EEPROM device during module production using a serial presence detect protocol (I²C synchronous 2-wire bus).

Byte# Description SPD Entry Value			Hex					
			HYM					
			64 V1005 GU-50	64 V1005 GU-60	64 V1005 GU-70	72 V1005 GU-50	72 V1005 GU-60	72 V1005 GU-70
0	Number of SPD bytes	128	80	80	80	80	80	80
1	Total bytes in Serial PD	256	08	08	08	08	08	08
2	Memory Type	EDO	02	02	02	02	02	02
3	Number of Row Addresses	10	0A	0A	0A	0A	0A	0A
4	Number of Column Addresses	10	0A	0A	0A	0A	0A	0A
5	Number of DIMM Banks	1	01	01	01	01	01	01
6	Module Data Width	x64 / x72	40	40	40	48	48	48
7	Module Data Width (cont'd)	0	00	00	00	00	00	00
8	Module Interface Levels	LVTTL	01	01	01	01	01	01
9	RAS access time	50 / 60 / 70 ns	32	3C	46	32	3C	46
10	CAS access time	13 / 15 / 20 ns	0D	0F	14	0D	0F	14
11	Dimm Config (Error Det/Corr.)	none / ECC	00	00	00	02	02	02
12	Refresh Rate/Type	normal 15.6µs	00	00	00	00	00	00
13	Primary DRAM Organisation	x16	16	16	16	16	16	16
14	Secondary DRAMOrgansation	undefined/ x4	00	00	00	04	04	04
15-31	reserved for future offerings		FF	FF	FF	FF	FF	FF
32	Superset Memory Type	NA	FF	FF	FF	FF	FF	FF
33-61	Superset information (may be used in future)	NA	FF	FF	FF	FF	FF	FF
62	SPD Revision Designator	Rev. 1.0	01	01	01	01	01	01
63	Checksum for bytes 0-62		XX	XX	XX	XX	XX	XX
64-127	Manufacturer Information (optional)		FF	FF	FF	FF	FF	FF
128- 255	Unused Storage Locations		FF	FF	FF	FF	FF	FF

L-DIM-168-10
Module package
(168 pin, dual read-out, single in-line memory module)



DM168-10.WMF

preliminary drawing