
HM62V16256CBP Series

4 M SRAM (256-kword × 16-bit)

HITACHI

ADE-203-1259 (Z)
Preliminary
Rev. 0.0
Mar. 21, 2001

Description

The Hitachi HM62V16256CBP Series is 4-Mbit static RAM organized 262,144-word × 16-bit. HM62V16256CBP Series has realized higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is packaged in 48 bumps chip size package with 0.75 mm bump pitch for high density surface mounting.

Features

- Single 2.5 V and 3.0 V supply: 2.2 V to 3.6 V
- Fast access time: 55 ns/70 ns (max)
- Power dissipation:
 - Active: 5.0 mW/MHz (typ)($V_{CC} = 2.5$ V)
: 6.0 mW/MHz (typ) ($V_{CC} = 3.0$ V)
 - Standby: 2 μ W (typ) ($V_{CC} = 2.5$ V)
: 2.4 μ W (typ) ($V_{CC} = 3.0$ V)
- Completely static memory.
 - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
 - Three state output
- Battery backup operation.
 - 2 chip selection for battery backup

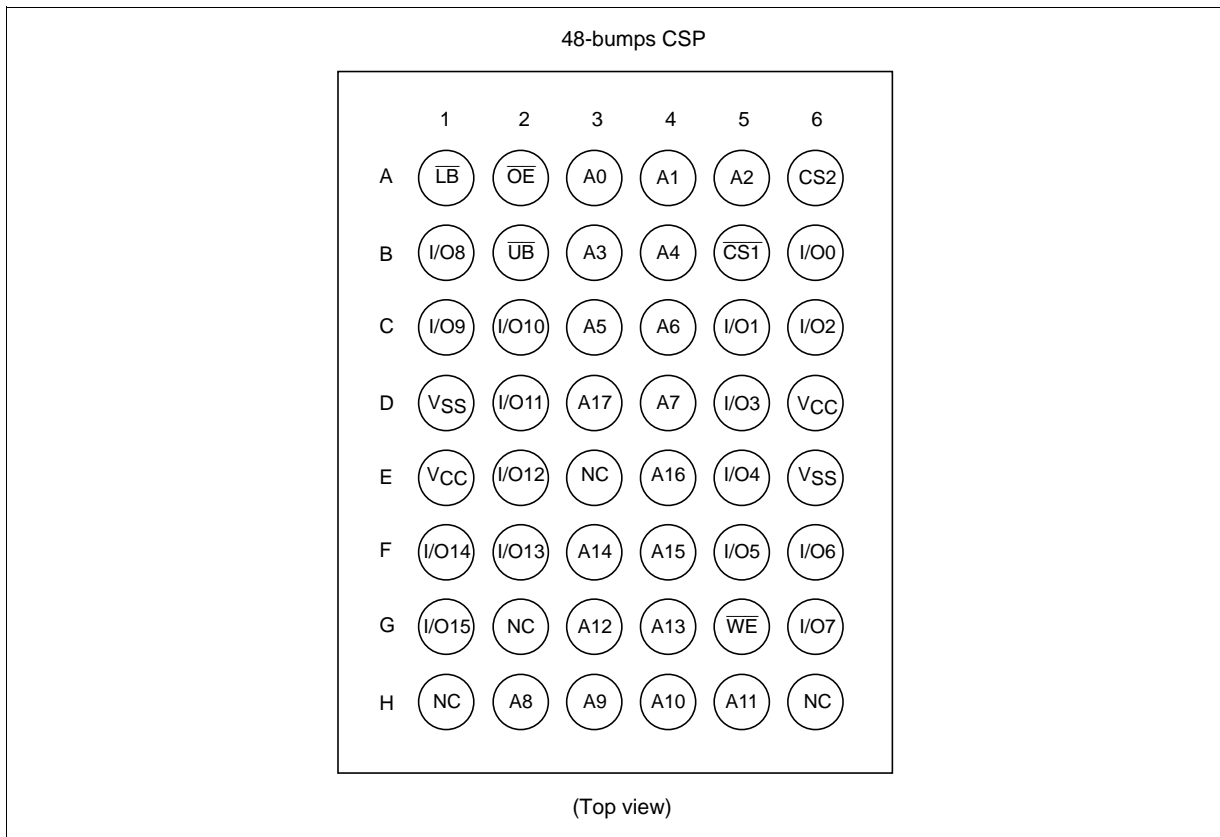
Preliminary: The specification of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specification.

HM62V16256CBP Series

Ordering Information

Type No.	Access time	Package
HM62V16256CLBP-5	55 ns	48-bumps CSP with 0.75 mm bump pitch (TBP-48)
HM62V16256CLBP-7	70 ns	
HM62V16256CLBP-5SL	55 ns	
HM62V16256CLBP-7SL	70 ns	

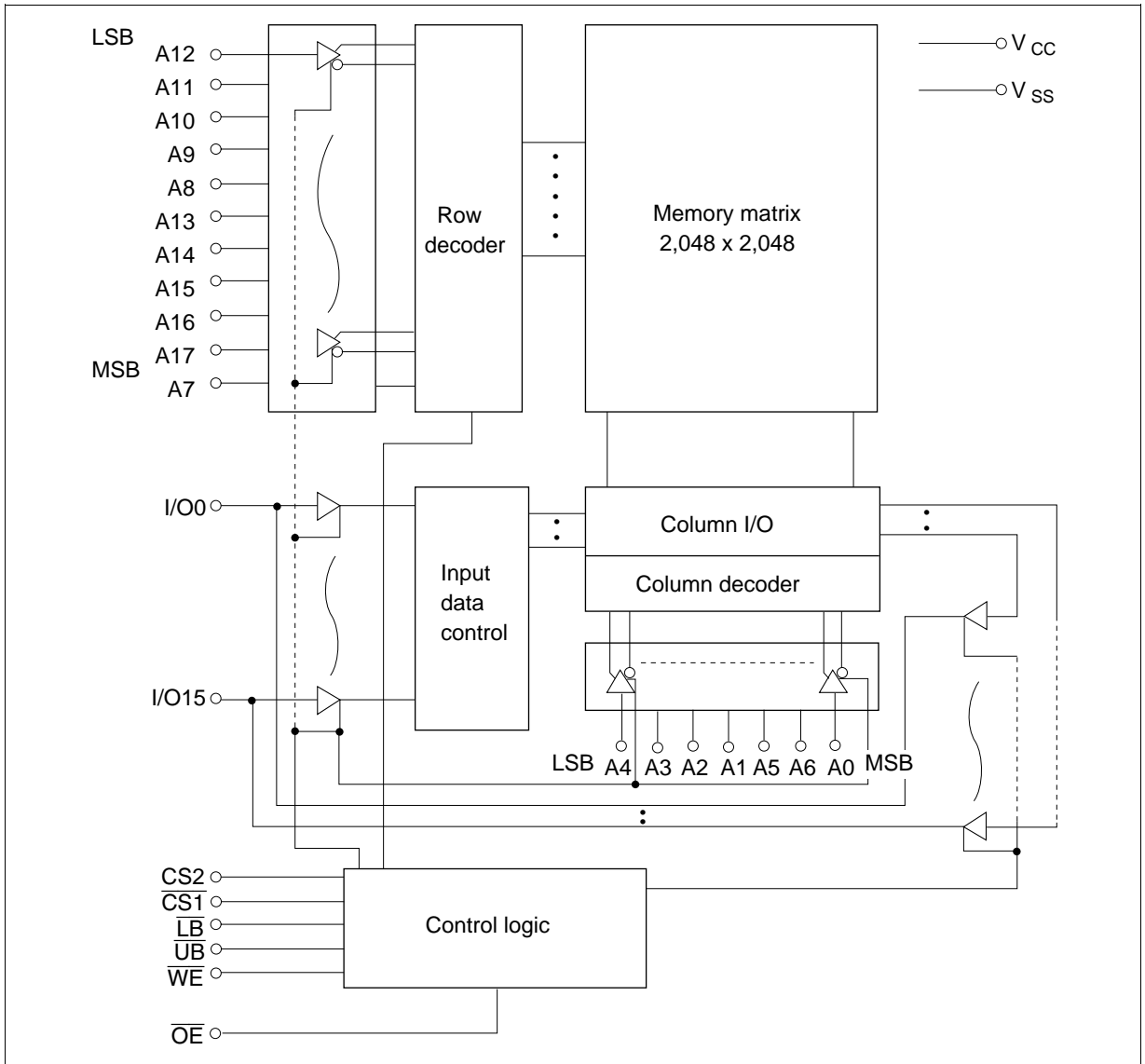
Pin Arrangement



Pin Description

Pin name	Function
A0 to A17	Address input
I/O0 to I/O15	Data input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
\overline{WE}	Write enable
\overline{OE}	Output enable
\overline{LB}	Lower byte select
\overline{UB}	Upper byte select
V_{cc}	Power supply
V_{ss}	Ground
NC	No connection

Block Diagram



Operation Table

$\overline{CS1}$	CS2	\overline{WE}	\overline{OE}	\overline{UB}	\overline{LB}	I/O0 to I/O7	I/O8 to I/O15	Operation
H	x	x	x	x	x	High-Z	High-Z	Standby
x	L	x	x	x	x	High-Z	High-Z	Standby
x	x	x	x	H	H	High-Z	High-Z	Standby
L	H	H	L	L	L	Dout	Dout	Read
L	H	H	L	H	L	Dout	High-Z	Lower byte read
L	H	H	L	L	H	High-Z	Dout	Upper byte read
L	H	L	x	L	L	Din	Din	Write
L	H	L	x	H	L	Din	High-Z	Lower byte write
L	H	L	x	L	H	High-Z	Din	Upper byte write
L	H	H	H	x	x	High-Z	High-Z	Output disable

Note: H: V_{IH} , L: V_{IL} , x: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Terminal voltage on any pin relative to V_{SS}	V_T	-0.5* ¹ to $V_{CC} + 0.3$ * ²	V
Power dissipation	P_T	1.0	W
Storage temperature range	Tstg	-55 to +125	°C
Storage temperature range under bias	Tbias	-20 to +85	°C

Notes: 1. V_T min: -3.0 V for pulse half-width \leq 30 ns.

2. Maximum voltage is +4.6 V.

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	2.2	2.5/3.0	3.6	V	
	V_{SS}	0	0	0	V	
Input high voltage	$V_{CC} = 2.2$ V to 2.7 V V_{IH}	2.0	—	$V_{CC} + 0.3$	V	
	$V_{CC} = 2.7$ V to 3.6 V V_{IH}	2.0	—	$V_{CC} + 0.3$	V	
Input low voltage	$V_{CC} = 2.2$ V to 2.7 V V_{IL}	-0.2	—	0.4	V	1
	$V_{CC} = 2.7$ V to 3.6 V V_{IL}	-0.3	—	0.6	V	1
Ambient temperature range	Ta	-20	—	70	°C	

Note: 1. V_{IL} min: -3.0 V for pulse half-width \leq 30 ns.

DC Characteristics

Parameter	Symbol	Min	Typ* ¹	Max	Unit	Test conditions
Input leakage current	$ I_{LI} $	—	—	1	μA	$V_{in} = V_{SS} \text{ to } V_{CC}$
Output leakage current	$ I_{LO} $	—	—	1	μA	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{LB} = \overline{UB} = V_{IH}$, $V_{I/O} = V_{SS} \text{ to } V_{CC}$
Operating current	I_{CC}	—	5	20	mA	$\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, Others = V_{IH}/V_{IL} , $I_{I/O} = 0 \text{ mA}$
Average operating current	I_{CC1}	—	18	25	mA	Min. cycle, duty = 100%, $I_{I/O} = 0 \text{ mA}$, $\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, Others = V_{IH}/V_{IL}
	I_{CC2}	—	2	5	mA	Cycle time = 1 μs , duty = 100%, $I_{I/O} = 0 \text{ mA}$, $\overline{CS1} \leq 0.2 \text{ V}$, $CS2 \geq V_{CC} - 0.2 \text{ V}$ $V_{IH} \geq V_{CC} - 0.2 \text{ V}$, $V_{IL} \leq 0.2 \text{ V}$
Standby current	I_{SB}	—	0.1	0.3	mA	$CS2 = V_{IL}$
Standby current	I_{SB1}^{*2}	—	0.8	20	μA	$0 \text{ V} \leq V_{in}$ (1) $0 \text{ V} \leq CS2 \leq 0.2 \text{ V}$ or (2) $\overline{CS1} \geq V_{CC} - 0.2 \text{ V}$, $CS2 \geq V_{CC} - 0.2 \text{ V}$ or (3) $\overline{LB} = \overline{UB} \geq V_{CC} - 0.2 \text{ V}$ $CS2 \geq V_{CC} - 0.2 \text{ V}$ $\overline{CS1} \leq 0.2 \text{ V}$
	I_{SB1}^{*3}	—	0.8	10	μA	
Output high voltage	$V_{CC} = 2.2 \text{ V to } 2.7 \text{ V}$ V_{OH}	2.0	—	—	V	$I_{OH} = -0.5 \text{ mA}$
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ V_{OH}	2.4	—	—	V	$I_{OH} = -1 \text{ mA}$
	$V_{CC} = 2.2 \text{ V to } 3.6 \text{ V}$ V_{OH}	$V_{CC} - 0.2$	—	—	V	$I_{OH} = -100 \mu\text{A}$
Output low voltage	$V_{CC} = 2.2 \text{ V to } 2.7 \text{ V}$ V_{OL}	—	—	0.4	V	$I_{OL} = 0.5 \text{ mA}$
	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$ V_{OL}	—	—	0.4	V	$I_{OL} = 2 \text{ mA}$
	$V_{CC} = 2.2 \text{ V to } 3.6 \text{ V}$ V_{OL}	—	—	0.2	V	$I_{OL} = 100 \mu\text{A}$

Notes: 1. Typical values are at $V_{CC} = 2.5 \text{ V}/3.0 \text{ V}$, $T_a = +25^\circ\text{C}$ and not guaranteed.

2. This characteristic is guaranteed only for L-version.

3. This characteristic is guaranteed only for L-SL version.

Capacitance ($T_a = +25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

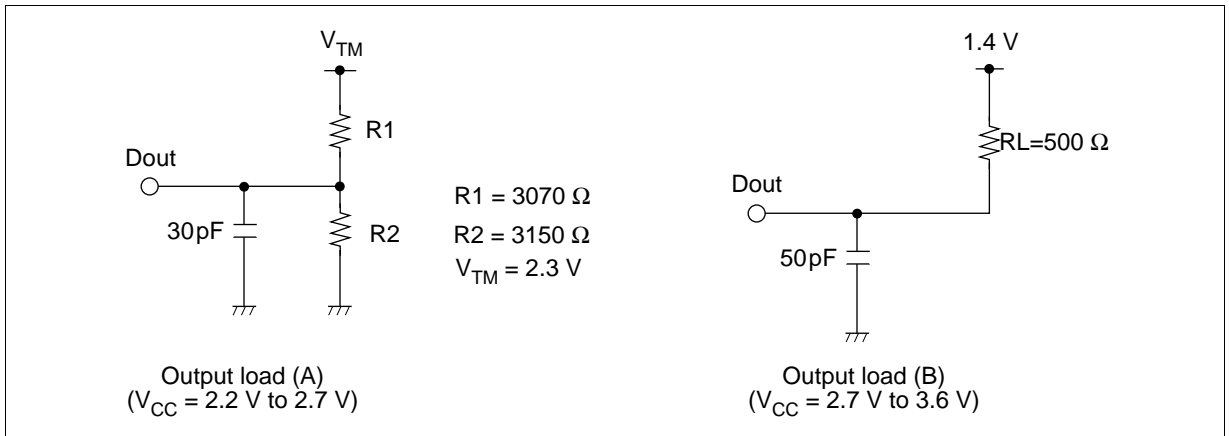
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	C_{in}	—	—	8	pF	$V_{in} = 0\text{ V}$	1
Input/output capacitance	$C_{i/o}$	—	—	10	pF	$V_{i/o} = 0\text{ V}$	1

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics ($T_a = -20$ to $+70^\circ\text{C}$, $V_{CC} = 2.2$ V to 3.6 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: $V_{IL} = 0.4$ V, $V_{IH} = 2.0$ V ($V_{CC} = 2.2$ V to 2.7 V)
 $V_{IL} = 0.4$ V, $V_{IH} = 2.2$ V ($V_{CC} = 2.7$ V to 3.6 V)
- Input rise and fall time: 5 ns
- Input timing reference levels: 1.1 V ($V_{CC} = 2.2$ V to 2.7 V)
- Output timing reference levels: 1.1 V ($V_{CC} = 2.2$ V to 2.7 V)
- Input timing reference levels: 1.4 V ($V_{CC} = 2.7$ V to 3.6 V)
- Output timing reference levels: 1.4 V (HM62V16256CBP-5, $V_{CC} = 2.7$ V to 3.6 V)
: 2.0 V/0.8 V (HM62V16256CBP-7, $V_{CC} = 2.7$ V to 3.6 V)
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	HM62V16256CBP				Unit	Notes
		-5		-7			
		Min	Max	Min	Max		
Read cycle time	t_{RC}	55	—	70	—	ns	
Address access time	t_{AA}	—	55	—	70	ns	
Chip select access time	t_{ACS1}	—	55	—	70	ns	
	t_{ACS2}	—	55	—	70	ns	
Output enable to output valid	t_{OE}	—	35	—	40	ns	
Output hold from address change	t_{OH}	10	—	10	—	ns	
\overline{LB} , \overline{UB} access time	t_{BA}	—	55	—	70	ns	
Chip select to output in low-Z	t_{CLZ1}	10	—	10	—	ns	2, 3
	t_{CLZ2}	10	—	10	—	ns	2, 3
\overline{LB} , \overline{UB} enable to low-z	t_{BLZ}	5	—	5	—	ns	2, 3
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	2, 3
Chip deselect to output in high-Z	t_{CHZ1}	0	20	0	25	ns	1, 2, 3
	t_{CHZ2}	0	20	0	25	ns	1, 2, 3
\overline{LB} , \overline{UB} disable to high-Z	t_{BHZ}	0	20	0	25	ns	1, 2, 3
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	ns	1, 2, 3

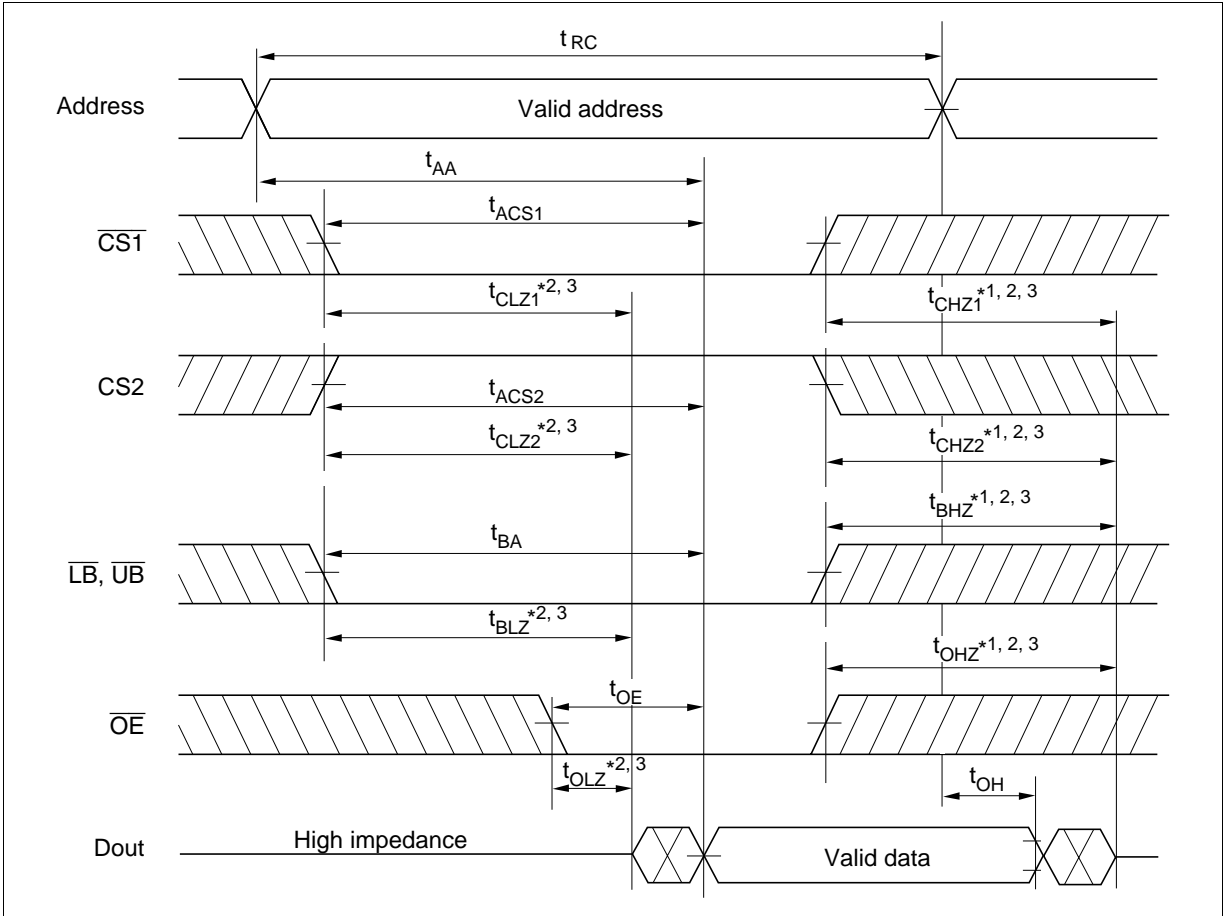
Write Cycle

Parameter	Symbol	HM62V16256CBP				Unit	Notes
		-5		-7			
		Min	Max	Min	Max		
Write cycle time	t_{WC}	55	—	70	—	ns	
Address valid to end of write	t_{AW}	50	—	60	—	ns	
Chip selection to end of write	t_{CW}	50	—	60	—	ns	5
Write pulse width	t_{WP}	40	—	50	—	ns	4
\overline{LB} , \overline{UB} valid to end of write	t_{BW}	50	—	55	—	ns	
Address setup time	t_{AS}	0	—	0	—	ns	6
Write recovery time	t_{WR}	0	—	0	—	ns	7
Data to write time overlap	t_{DW}	25	—	30	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	ns	2
Output disable to output in High-Z	t_{OHZ}	0	20	0	25	ns	1, 2
Write to output in high-Z	t_{WHZ}	0	20	0	25	ns	1, 2

- Notes:
- t_{CHZ} , t_{OHZ} , t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
 - This parameter is sampled and not 100% tested.
 - At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
 - A write occurs during the overlap of a low $\overline{CS1}$, a high CS2, a low \overline{WE} and a low \overline{LB} or a low \overline{UB} . A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high, \overline{WE} going low and \overline{LB} going low or \overline{UB} going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low, \overline{WE} going high and \overline{LB} going high or \overline{UB} going high. t_{WP} is measured from the beginning of write to the end of write.
 - t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
 - t_{AS} is measured from the address valid to the beginning of write.
 - t_{WR} is measured from the earliest of $\overline{CS1}$ or \overline{WE} going high or CS2 going low to the end of write cycle.

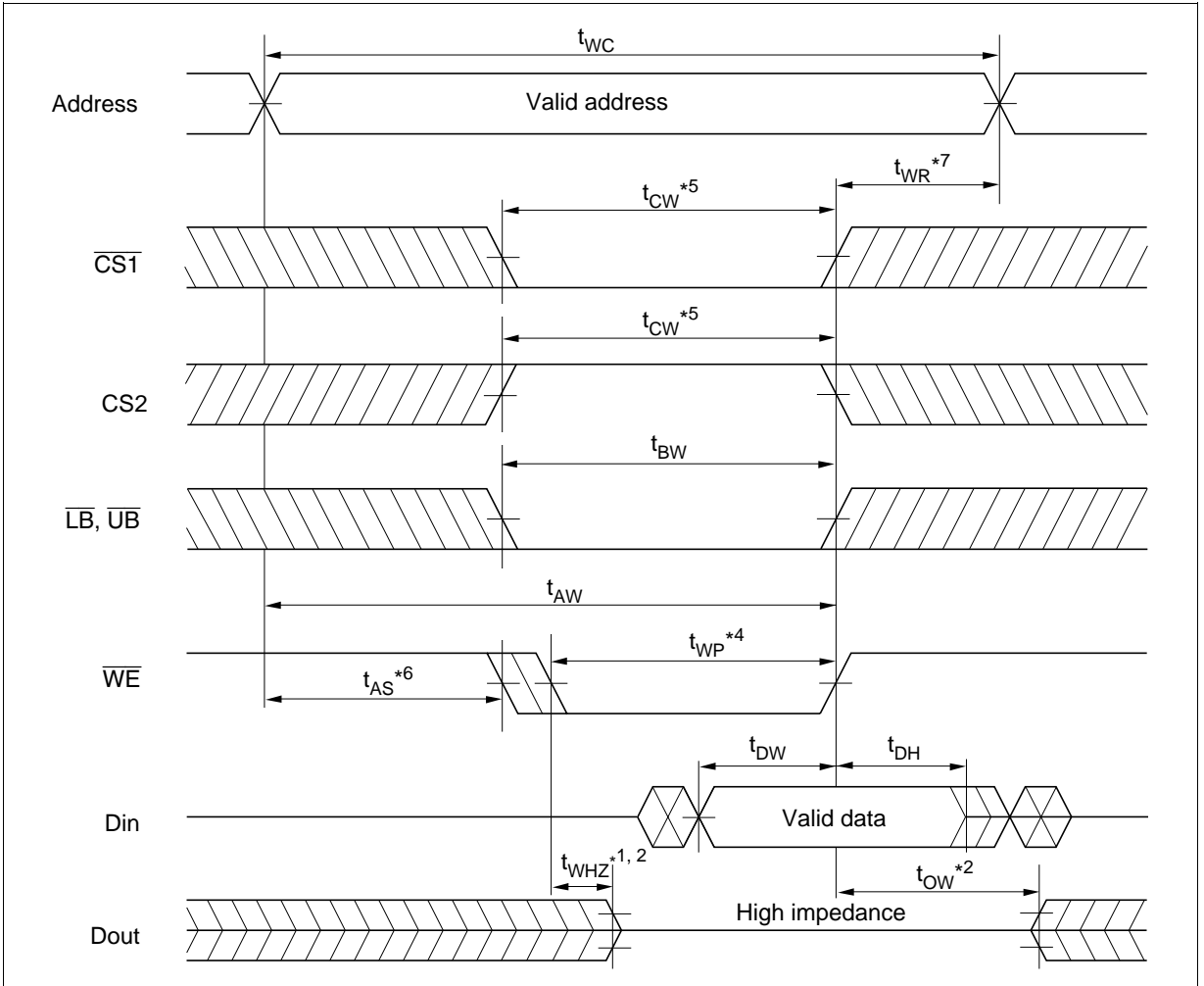
Timing Waveform

Read Cycle

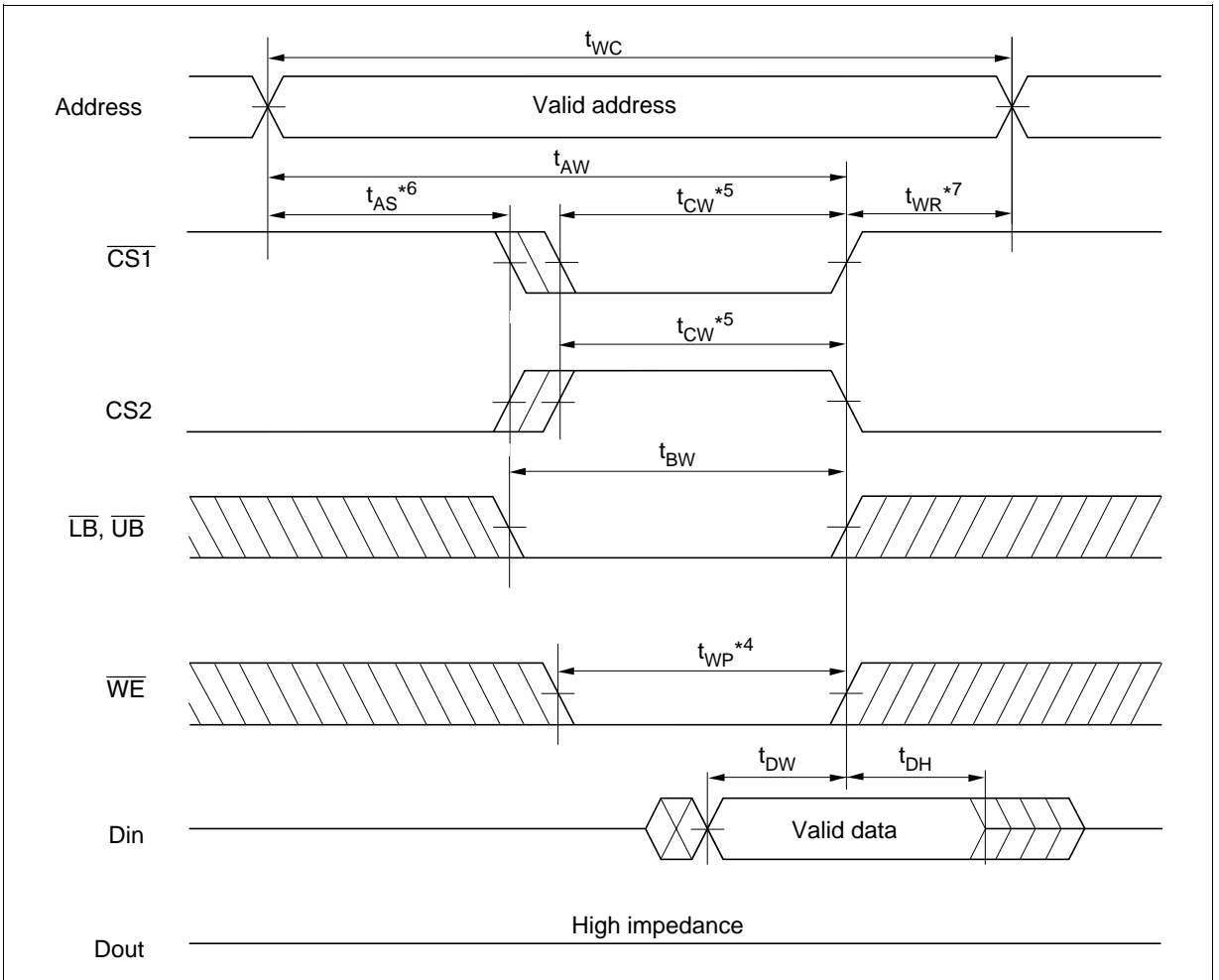


HM62V16256CBP Series

Write Cycle (1) (\overline{WE} Clock)

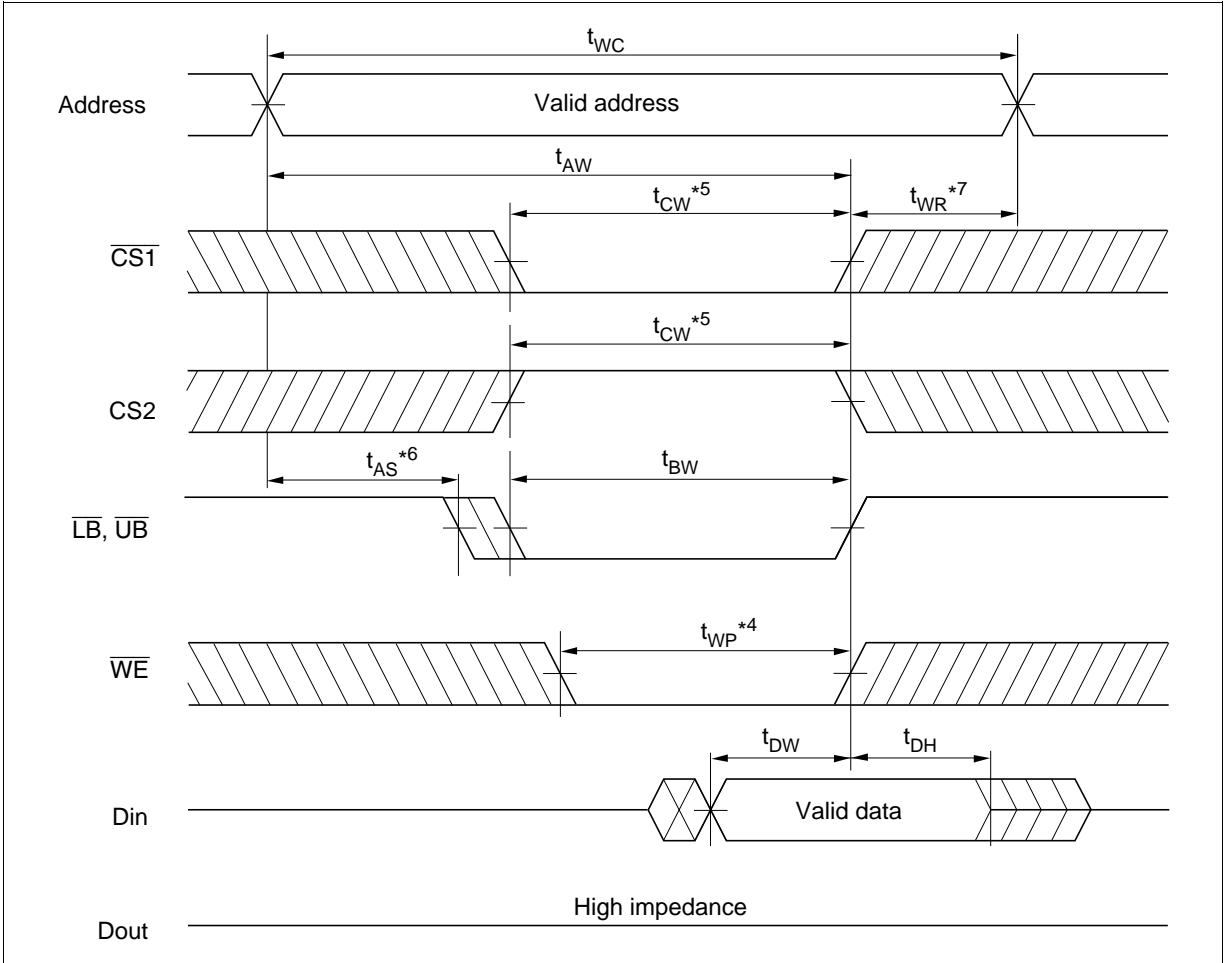


Write Cycle (2) (\overline{CS} Clock, $\overline{OE} = V_{IH}$)



HM62V16256CBP Series

Write Cycle (3) (\overline{LB} , \overline{UB} Clock, $\overline{OE} = V_{IH}$)

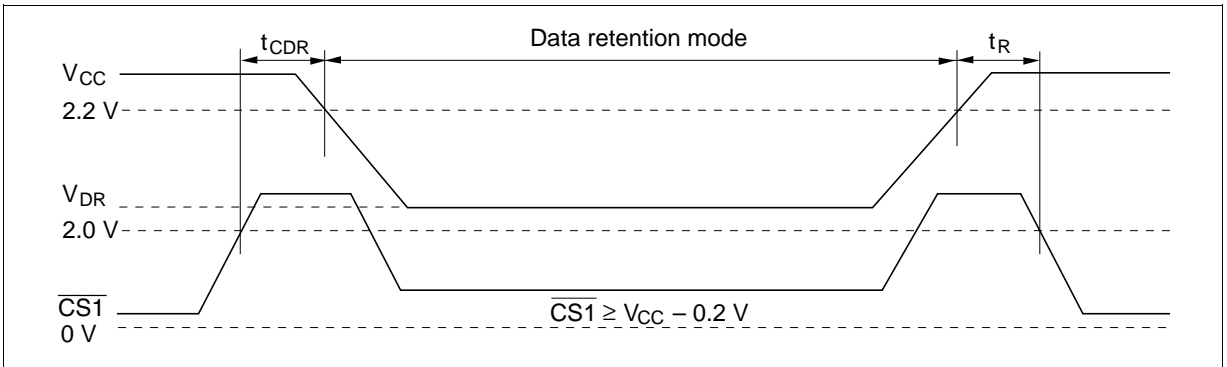


Low V_{CC} Data Retention Characteristics ($T_a = -20$ to $+70^\circ\text{C}$)

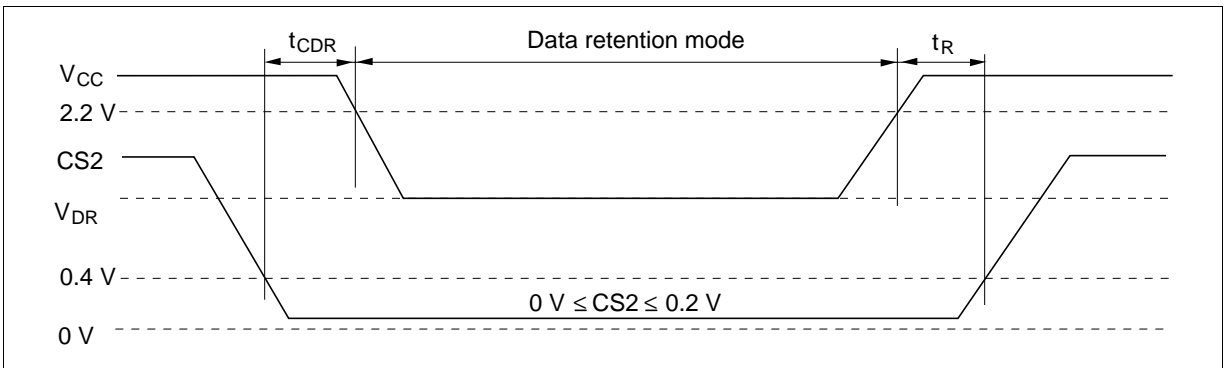
Parameter	Symbol	Min	Typ ^{*4}	Max	Unit	Test conditions ^{*3}
V_{CC} for data retention	V_{DR}	2.0	—	3.6	V	$V_{in} \geq 0\text{V}$ (1) $0\text{V} \leq \overline{\text{CS2}} \leq 0.2\text{V}$ or (2) $\overline{\text{CS2}} \geq V_{CC} - 0.2\text{V}$, $\overline{\text{CS1}} \geq V_{CC} - 0.2\text{V}$ or (3) $\overline{\text{LB}} = \overline{\text{UB}} \geq V_{CC} - 0.2\text{V}$, $\overline{\text{CS2}} \geq V_{CC} - 0.2\text{V}$, $\overline{\text{CS1}} \leq 0.2\text{V}$
Data retention current	I_{CCDR}^{*1}	—	0.8	20	μA	$V_{CC} = 3.0\text{V}$, $V_{in} \geq 0\text{V}$ (1) $0\text{V} \leq \overline{\text{CS2}} \leq 0.2\text{V}$ or (2) $\overline{\text{CS2}} \geq V_{CC} - 0.2\text{V}$, $\overline{\text{CS1}} \geq V_{CC} - 0.2\text{V}$ or (3) $\overline{\text{LB}} = \overline{\text{UB}} \geq V_{CC} - 0.2\text{V}$, $\overline{\text{CS2}} \geq V_{CC} - 0.2\text{V}$, $\overline{\text{CS1}} \leq 0.2\text{V}$
	I_{CCDR}^{*2}	—	0.8	10	μA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}^{*5}	—	—	ns	

- Notes:
1. This characteristic is guaranteed only for L-version, 10 μA max. at $T_a = -20$ to $+40^\circ\text{C}$.
 2. This characteristic is guaranteed only for L-SL version, 3 μA max. at $T_a = -20$ to $+40^\circ\text{C}$.
 3. CS2 controls address buffer, $\overline{\text{WE}}$ buffer, $\overline{\text{CS1}}$ buffer, $\overline{\text{OE}}$ buffer, $\overline{\text{LB}}$, $\overline{\text{UB}}$ buffer and Din buffer. If CS2 controls data retention mode, V_{in} levels (address, $\overline{\text{WE}}$, $\overline{\text{OE}}$, $\overline{\text{CS1}}$, $\overline{\text{LB}}$, $\overline{\text{UB}}$, I/O) can be in the high impedance state. If $\overline{\text{CS1}}$ controls data retention mode, CS2 must be $\overline{\text{CS2}} \geq V_{CC} - 0.2\text{V}$ or $0\text{V} \leq \overline{\text{CS2}} \leq 0.2\text{V}$. The other input levels (address, $\overline{\text{WE}}$, $\overline{\text{OE}}$, $\overline{\text{LB}}$, $\overline{\text{UB}}$, I/O) can be in the high impedance state.
 4. Typical values are at $V_{CC} = 3.0\text{V}$, $T_a = +25^\circ\text{C}$ and not guaranteed.
 5. t_{RC} = read cycle time.

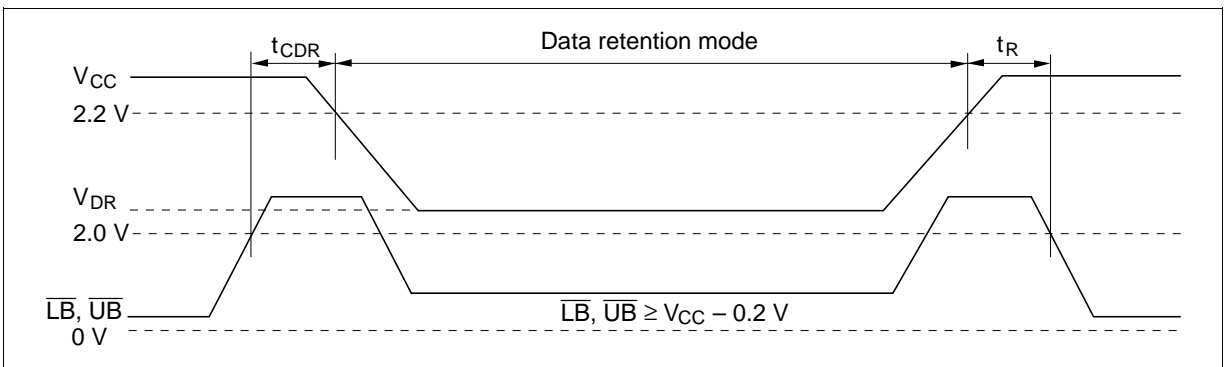
Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)



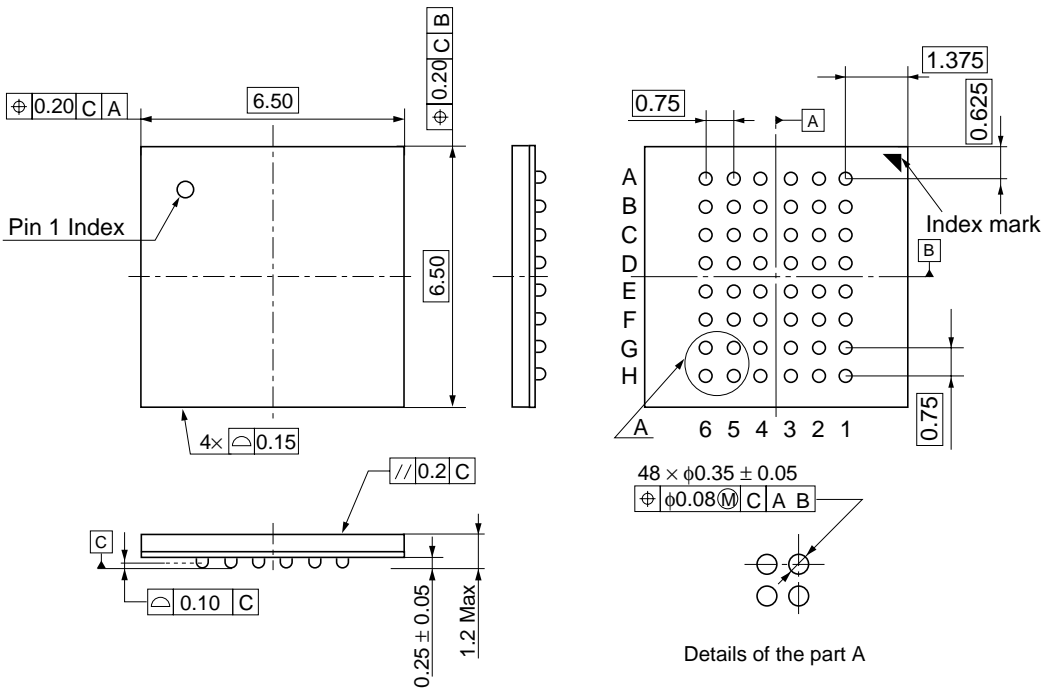
Low V_{CC} Data Retention Timing Waveform (3) (\overline{LB} , \overline{UB} Controlled)



Package Dimensions

HM62V16256CLBP Series (TBP-48)

Unit: mm



Hitachi Code	TBP-48
JEDEC	—
EIAJ	—
Mass	0.09 g

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