DSP56F827

Product Brief
DSP56F827 16-bit Digital Signal Processor

- Up to 40 MIPS at 80 MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- Hardware DO and REP loops
- 64K × 16-bit words Program Flash
- 1K × 16-bit words Program RAM
- 4K × 16-bit words Data Flash
- 4K × 16-bit words Data RAM
- Up to 64K × 16-bit words external memory expansion each for Program and Data memory
- JTAG/OnCE™ for debugging
- General Purpose Quad Timer

- MCU-friendly instruction set supports both DSP and controller functions: MAC, bit manipulation unit, 14 addressing modes
- 8-channel Programmable Chip Select
- 10-channel, 12-bit ADC
- Synchronous Serial Interface (SSI)
- Serial Port Interface (SPI)
- Serial Communications Interface (SCI)
- Time-of-Day (TOD) Timer
- 128-pin LQFP Package
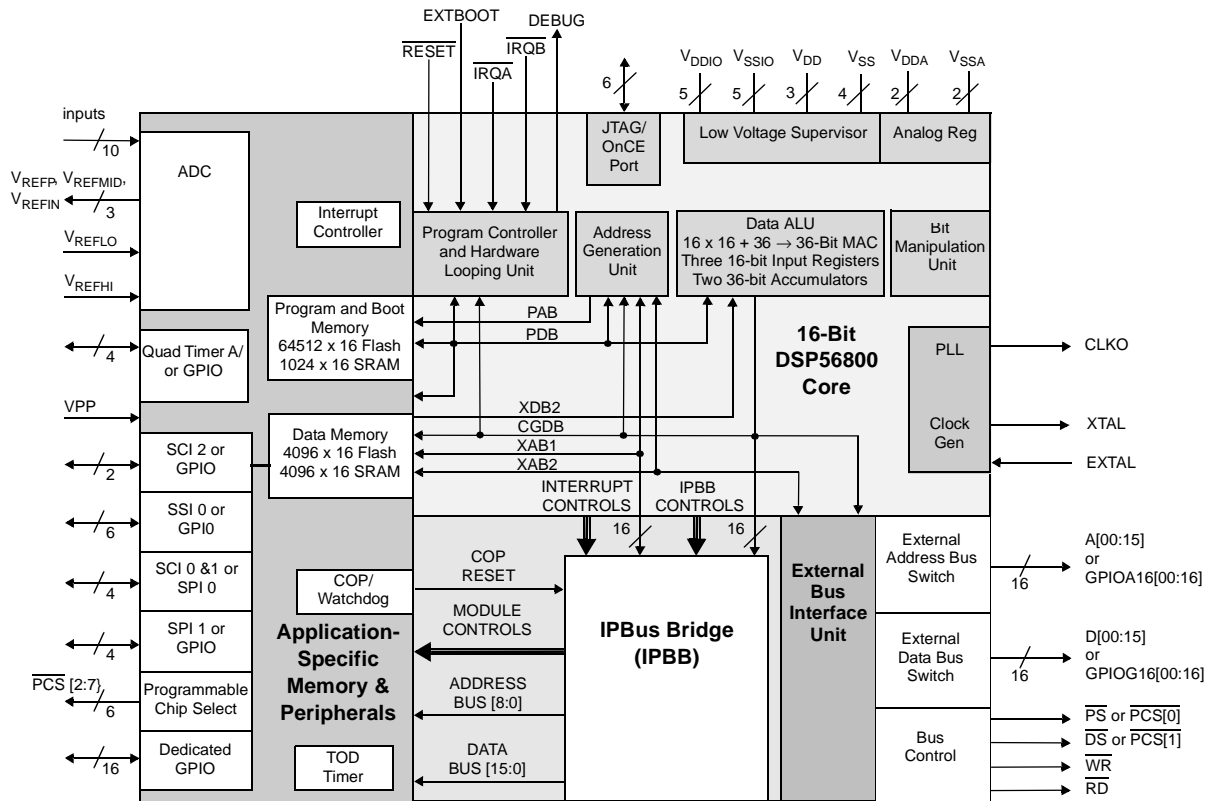- 16-dedicated and 48 shared GPIO

Figure 1. DSP56F827 Block Diagram

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DSP56800 Digital Signal Processing Core Features

- Efficient 16-bit DSP56800 family DSP engine with dual Harvard architecture
- As many as 40 Million Instructions Per Second (MIPS) at 80 MHz core frequency
- Single-cycle 16×16-bit parallel Multiplier-Accumulator (MAC)
- Two 36-bit accumulators including extension bits
- 16-bit bidirectional shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses and one external address bus
- Four internal data buses and one external data bus
- Instruction set supports both DSP and controller functions
- Controller style addressing modes and instructions for compact code
- Efficient C Compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/OnCE Debug Programming Interface

DSP56F827 Memory Features

- Harvard architecture permits as many as three simultaneous accesses to program and data memory
- On-chip memory including a low cost, high volume flash solution
    - 64K words of Program Flash
    - 1K words of Program RAM
    - 4K words of Data RAM
    - 4K words of Data Flash
- Off-chip memory expansion capabilities programmable for 0, 4, 8, or 12 wait states
    - As much as $64\,K \times 16$ data memory
    - As much as $64\,K \times 16$ program memory

DSP56F827 Peripheral Circuit Features

- One 10 channel, 12-bit, Analog to Digital Converter (ADC)
- One General Purpose Quad Timer totaling 4 pins
- One Serial Peripheral Interface with configurable four-pin port multiplexed with two Serial Communications Interfaces totalling 4 pins or 4 GPIO pins
- Three Serial Communication Interfaces with 2 pins (or 4 additional GPIO pins)
- Two Serial Peripheral Interface with configurable four-pin port (or 4 additional GPIO pins)
- One Synchronous Serial Interface with 6 pins (or 6 additional GPIO pins)
- One 8 channel Programmable Chip Select
- Sixteen dedicated and forty eight multiplexed GPIO pins

- Computer-Operating Properly (COP) Watchdog timer
- Two external interrupt pins
- External reset pin for hardware reset
- JTAG/On-Chip Emulation (OnCE™) for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase Lock Loop-based frequency synthesizer for the DSP core clock
- Fabricated in high-density EMOS with 5V tolerant, TTL-compatible digital inputs
- One Time of Day (TOD) Timer

Energy Information

- Dual power supply, 3.3V and 2.5V
- Wait and Multiple Stop modes available

DSP56F827 Description

The DSP56F827 is a member of the DSP56800 core-based family of Digital Signal Processors (DSPs). It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution for general purpose applications. Because of its low cost, configuration flexibility, and compact program code, the DSP56F827 is well-suited for many applications. The DSP56F827 includes many peripherals that are especially useful for applications such as: noise suppression, ID tag readers, sonic/subsonic detectors, security access devices, remote metering, sonic alarms.

The DSP56800 core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for C/C++ Compilers to enable rapid development of optimized control applications.

"Best in Class" Development Environment

The SDK (Software Development Kit) provides fully debugged peripheral drivers, libraries and interfaces that allow programmers to create their unique C application code independent of component architecture. The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, the SDK, CodeWarrior, and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

Product Documentation

The four documents listed in Table 1 are required for a complete description and proper design with the DSP56F827. Documentation is available from local Motorola distributors, Motorola semiconductor sales offices, Motorola Literature Distribution Centers, or online at www.motorola.com/SPS/DSP.

Table 1. DSP56F827 Chip Documentation

Topic	Description	Order Number
DSP56800 Family Manual	Detailed description of the DSP56800 family architecture, and 16-bit DSP core processor and the instruction set	DSP56800FM/D
DSP56F826/827 User's Manual	Detailed description of memory, peripherals, and interfaces of the DSP56F826/827	DSP56F826-827UM/D
DSP56F827 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions	DSP56F827/D
DSP56F827 Product Brief	Summary description and block diagram of the DSP56F827 core, memory, peripherals and interfaces (this document)	DSP56F827PB

Ordering Information

Consult a Motorola Semiconductor sales office or authorized distributor to order parts.

Table 2. DSP56F827 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
DSP56F827	3.0–3.6 V	Low Profile Quad Flat (LQFP)	128	80	DSP56F827FG80

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado 80217. 1–303–675–2140 or 1–800–441–2447

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ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong. 852–26668334

Technical Information Center: 1–800–521–6274

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