PRELIMINARY

CY2305C
CY2309C

3.3V Zero Delay Clock Buffer

Features

- 10 MHz to 100-133 MHz operating range, compatible with CPU and PCI bus frequencies
- Zero input and output propagation delay
- Multiple low skew outputs
- One input drives five outputs (CY2305C)
- One input drives nine outputs, grouped as 4 + 4 + 1 (CY2309C)
- 50 ps typical cycle-cycle jitter (15 pF, 66 MHz)
- Test Mode to bypass phase locked loop (PLL) (CY2309C) only, see "Select Input Decoding for CY2309C" on page 3
- Available in space saving 16-pin 150 Mil SOIC or 4.4 mm TSSOP packages (CY2309C), and 8-pin, 150 Mil SOIC package (CY2305C)
- 3.3V operation
- Industrial temperature available

Functional Description

The CY2305C and CY2309C are die replacement parts for CY2305 and CY2309.

The CY2309C is a low cost 3.3V zero delay buffer designed to distribute high speed clocks and is available in a 16-pin SOIC or TSSOP package. The CY2305C is an 8-pin version of the CY2309C. It accepts one reference input and drives out five low skew clocks. The -1H versions of each device operate up to 100-133 MHz frequencies and have higher drive than the -1 devices. All parts have on-chip PLLs which lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad.

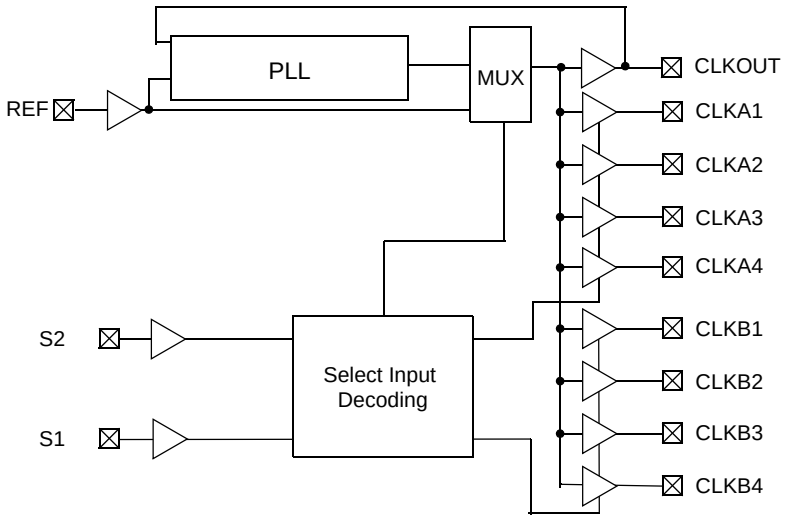
The CY2309C has two banks of four outputs each that are controlled by the select inputs as shown in the "Select Input Decoding for CY2309C" on page 3. If all output clocks are not required, BankB is three-stated. The input clock is directly applied to the outputs by the select inputs for chip and system testing purposes.

The CY2305C and CY2309C PLLs enter a power down mode when there are no rising edges on the REF input. In this state, the outputs are three-stated and the PLL is turned off. This results in less than 12.0 µA of current draw for commercial temperature devices and 25.0 µA for industrial temperature parts. The CY2309C PLL shuts down in one additional case as shown in the "Select Input Decoding for CY2309C" on page 3.

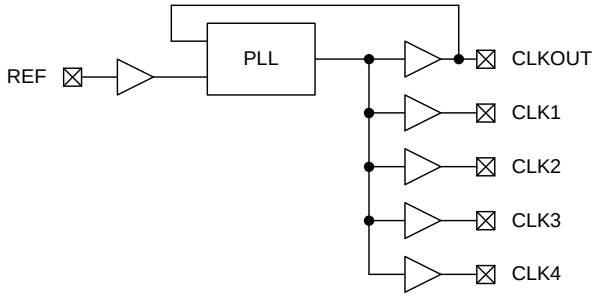
In the special case when S2:S1 is 1:0, the PLL is bypassed and REF is output from DC to the maximum allowable frequency. The part behaves like a non-zero delay buffer in this mode and the outputs are not three-stated.

The CY2305C or CY2309C is available in two or three different configurations as shown in the "Ordering Information" on page 11. The CY2305C-1 or CY2309C-1 is the base part. The CY2305-1H or CY2309-1H is the high drive version of the -1. Its rise and fall times are much faster than the -1s.

Logic Block Diagram for CY2309C



Logic Block Diagram for CY2305C



Pinouts

CY2309C

Figure 1. Pin Diagram - 16 Pin SOIC/TSSOP

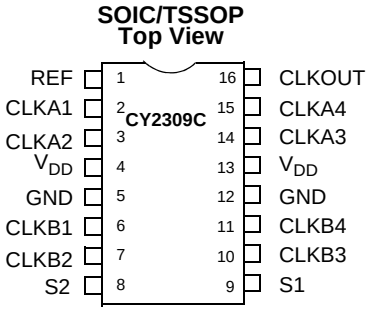


Table 1. Pin Definition - 16 Pin SOIC/TSSOP

Pin	Signal	Description
1	REF[1]	Input reference frequency
2	CLKA1[2]	Buffered clock output, Bank A
3	CLKA2[2]	Buffered clock output, Bank A
4	V_{DD}	3.3V supply
5	GND	Ground
6	CLKB1[2]	Buffered clock output, Bank B
7	CLKB2[2]	Buffered clock output, Bank B
8	S2[3]	Select input, bit 2
9	S1[3]	Select input, bit 1
10	CLKB3[2]	Buffered clock output, Bank B
11	CLKB4[2]	Buffered clock output, Bank B
12	GND	Ground
13	V_{DD}	3.3V supply
14	CLKA3[2]	Buffered clock output, Bank A
15	CLKA4[2]	Buffered clock output, Bank A
16	CLKOUT[2]	Buffered output, internal feedback on this pin

Table 2. Select Input Decoding for CY2309C

S2	S1	CLOCK A1–A4	CLOCK B1–B4	CLKOUT[4]	Output Source	PLL Shutdown
0	0	Three state	Three state	Driven	PLL	N
0	1	Driven	Three state	Driven	PLL	N
1	0	Driven	Driven	Driven	Reference	Y
1	1	Driven	Driven	Driven	PLL	N

Notes
1. Weak pull down.
2. Weak pull down on all outputs.
3. Weak pull ups on these inputs.
4. This output is driven and has an internal feedback for the PLL. The load on this output is adjusted to change the skew between the reference and output.

CY2305C

Figure 2. Pin Diagram - 8 Pin SOIC

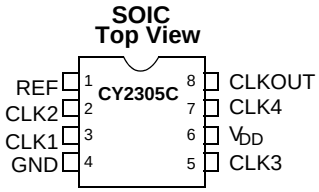


Table 3. Pin Description - 8 Pin SOIC

Pin	Signal	Description
1	REF[1]	Input reference frequency
2	CLK2[2]	Buffered clock output
3	CLK1[2]	Buffered clock output
4	GND	Ground
5	CLK3[2]	Buffered clock output
6	V_{DD}	3.3V supply
7	CLK4[2]	Buffered clock output
8	CLKOUT[2]	Buffered clock output, internal feedback on this pin

Zero Delay and Skew Control

All outputs should be uniformly loaded to achieve Zero Delay between the input and output. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input or output delay.

For applications requiring zero input or output delay, all outputs including CLKOUT are equally loaded. Even if CLKOUT is not used, it must have a capacitive load equal to that on other outputs for obtaining zero input or output delay.

For zero output or output skew, all outputs are loaded equally. For further information refer to the application note entitled “CY2305 and CY2309 as PCI and SDRAM Buffers”.

Absolute Maximum Conditions

Supply Voltage to Ground Potential.....–0.5V to +4.6V
DC Input Voltage (Except REF) .....–0.5V to V_{DD} + 0.5V
DC Input Voltage REF .....–0.5V to V_{DD} + 0.5V

Storage Temperature ..... –65°C to +150°C
Junction Temperature..... 150°C
Static Discharge Voltage
(per MIL-STD-883, Method 3015) .....> 2,000V

Operating Conditions for CY2305CSXC-XX and CY2309CSXC-XX

Operating Conditions table for CY2305CSXC-XX and CY2309CSXC-XX Commercial Temperature Devices.

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	0	70	°C
C_L	Load Capacitance, below 100 MHz		30	pF
C_L	Load Capacitance, from 100 MHz to 133 MHz		10	pF
C_{IN}	Input Capacitance		7	pF
t_{PU}	Power up time for all V_{DD}s to reach minimum specified voltage (power ramps are monotonic)	0.05	50	ms

Electrical Characteristics for CY2305CSXC-XX and CY2309CSXC-XX

Electrical Characteristics table for CY2305CSXC-XX and CY2309CSXC-XX Commercial Temperature Devices.

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW Voltage[5]		–0.3	0.8	V
V_{IH}	Input HIGH Voltage[5]		2.0	V_{DD} + 0.3	V
I_{IL}	Input LOW Current	V_{IN} = 0V	–	50	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}	–	100	µA
V_{OL}	Output LOW Voltage[6]	I_{OL} = 8 mA (–1) I_{OH} = 12 mA (–1H)	–	0.4	V
V_{OH}	Output HIGH Voltage[6]	I_{OH} = –8 mA (–1) I_{OL} = –12 mA (–1H)	2.4	–	V
I_{DD} (PD mode)	Power Down Supply Current	REF = 0 MHz	–	12.0	µA
I_{DD}	Supply Current	Unloaded outputs at 66.67 MHz, SEL inputs at V_{DD}	–	32	mA

Notes
5. .REF input has a threshold voltage of V_{DD}/2.
6. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Characteristics for CY2305CSXC-XX and CY2309CSXC-XX

Switching characteristics table for CY2305CSXC-1 and CY2309CSXC-1 Commercial Temperature Devices. All parameters are specified with loaded outputs.

Parameter	Name	Test Conditions	Min	Typ	Max	Unit
t_1	Output Frequency	30 pF load 10 pF load	10 10	–	100 133.33	MHz MHz
	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{out} = 66.67 MHz	40.0	50.0	60.0	%
t_3	Rise Time[6]	Measured between 0.8V and 2.0V	–	–	2.25	ns
t_4	Fall Time[6]	Measured between 0.8V and 2.0V	–	–	2.25	ns
t_5	Output to Output Skew[6]	All outputs equally loaded	–	–	200	ps
t_{6A}	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at $V_{DD}/2$	–	0	±350	ps
t_{6B}	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode, CY2309C device only.	1	5	8.7	ns
t_7	Device to Device Skew[6]	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	–	0	700	ps
t_J	Cycle to Cycle Jitter, peak[6]	Measured at 66.67 MHz, loaded outputs	–	50	175	ps
t_{LOCK}	PLL Lock Time[6]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

Switching characteristics table for CY2305CSXC-1H and CY2309CSXC-1H Commercial Temperature Devices. All parameters are specified with loaded outputs.

Parameter	Name	Description	Min	Typ	Max	Unit
t_1	Output Frequency	30-pF load 10-pF load	10 10	–	100 133.33	MHz MHz
	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{out} = 66.67 MHz	40.0	50.0	60.0	%
	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{out} < 50.0 MHz	45.0	50.0	55.0	%
t_3	Rise Time[6]	Measured between 0.8V and 2.0V	–	–	1.5	ns
t_4	Fall Time[6]	Measured between 0.8V and 2.0V	–	–	1.5	ns
t_5	Output to Output Skew[6]	All outputs equally loaded	–	–	200	ps
t_{6A}	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at $V_{DD}/2$	–	0	±350	ps
t_{6B}	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode, CY2309C device only.	1	5	8.7	ns
t_7	Device to Device Skew[6]	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	–	0	700	ps
t_8	Output Slew Rate[6]	Measured between 0.8V and 2.0V using Test Circuit #2	1	–	–	V/ns
t_J	Cycle to Cycle Jitter, peak[6]	Measured at 66.67 MHz, loaded outputs	–	–	175	ps
t_{LOCK}	PLL Lock Time[6]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

Operating Conditions for CY2305CSXI-XX and CY2309CSXI-XX

Operating conditions table for CY2305CSXI-XX and CY2309CSXI-XX Industrial Temperature Devices.

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	–40	85	°C
C_L	Load Capacitance, below 100 MHz	–	30	pF
C_L	Load Capacitance, from 100 MHz to 133 MHz	–	10	pF
C_{IN}	Input Capacitance	–	7	pF

Electrical Characteristics for CY2305CSXI-XX and CY2309CSXI-XX

Electrical characteristics table for CY2305CSXI-XX and CY2309CSXI-XX Industrial Temperature Devices.

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW Voltage[5]		–0.3	0.8	V
V_{IH}	Input HIGH Voltage[5]		2.0	V_{DD} + 0.3	V
I_{IL}	Input LOW Current	V_{IN} = 0V	–	50.0	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}	–	100.0	µA
V_{OL}	Output LOW Voltage[6]	I_{OL} = 8 mA (–1) I_{OH} =12 mA (–1H)	–	0.4	V
V_{OH}	Output HIGH Voltage[6]	I_{OH} = –8 mA (–1) I_{OL} = –12 mA (–1H)	2.4	–	V
I_{DD} (PD mode)	Power down Supply Current	REF = 0 MHz	–	25.0	µA
I_{DD}	Supply Current	Unloaded outputs at 66.67 MHz, SEL inputs at V_{DD}	–	35	mA

Switching Characteristics for CY2305CSXI-XX and CY2309CSXI-XX

Switching characteristics table for CY2305CSXI-1and CY2309CSXI-1 Industrial Temperature Devices. All parameters are specified with loaded outputs.

Parameter	Name	Test Conditions	Min	Typ	Max	Unit
t_1	Output Frequency	30 pF load 10 pF load	10 10		100 133.33	MHz MHz
	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{out} = 66.67 MHz	40.0	50.0	60.0	%
t_3	Rise Time[6]	Measured between 0.8V and 2.0V	–	–	2.25	ns
t_4	Fall Time[6]	Measured between 0.8V and 2.0V	–	–	2.25	ns
t_5	Output to Output Skew[6]	All outputs equally loaded	–	–	200	ps
t_{6A}	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at $V_{DD}/2$	–	0	±350	ps
t_{6B}	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode, CY2309C device only.	1	5	8.7	ns
t_7	Device to Device Skew[6]	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	–	0	700	ps
t_J	Cycle to Cycle Jitter, peak[6]	Measured at 66.67 MHz, loaded outputs	–	50	175	ps
t_{LOCK}	PLL Lock Time[6]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

Switching characteristics table for CY2305CSXI-1H and CY2309CSXI-1H Industrial Temperature Device. All parameters are specified with loaded outputs.

Parameter	Name	Description	Min	Typ	Max	Unit
t_1	Output Frequency	30 pF load 10 pF load	10 10	–	100 133.33	MHz MHz
	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{out} = 66.67 MHz	40.0	50.0	60.0	%
	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{out} < 50.0 MHz	45.0	50.0	55.0	%
t_3	Rise Time[6]	Measured between 0.8V and 2.0V	–	–	1.5	ns
t_4	Fall Time[6]	Measured between 0.8V and 2.0V	–	–	1.5	ns
t_5	Output to Output Skew[6]	All outputs equally loaded	–	–	200	ps
t_{6A}	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at $V_{DD}/2$	–	0	±350	ps
t_{6B}	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode, CY2309C device only.	1	5	8.7	ns
t_7	Device to Device Skew[6]	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	–	0	700	ps
t_8	Output Slew Rate[6]	Measured between 0.8V and 2.0V using Test Circuit #2	1	–		V/ns
t_J	Cycle to Cycle Jitter, peak[6]	Measured at 66.67 MHz, loaded outputs	–	–	175	ps
t_{LOCK}	PLL Lock Time[6]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

Switching Waveforms

Figure 3. Duty Cycle Timing

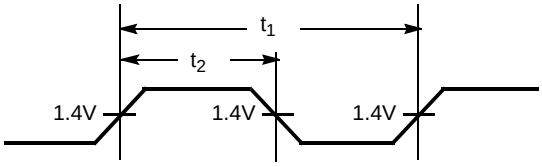


Figure 4. All Outputs Rise/Fall Time

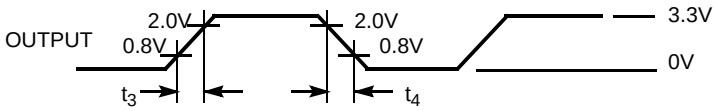


Figure 5. Output-Output Skew

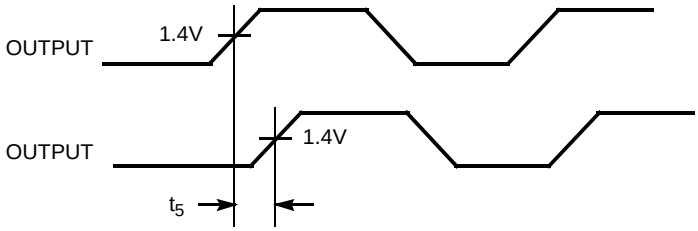


Figure 6. Input-Output Propagation Delay

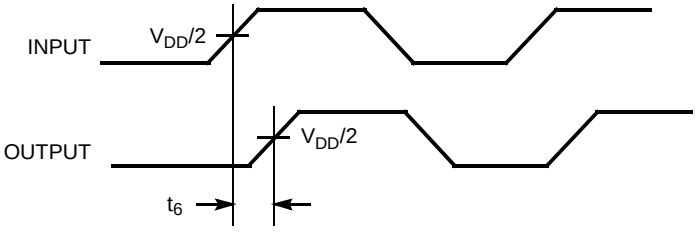
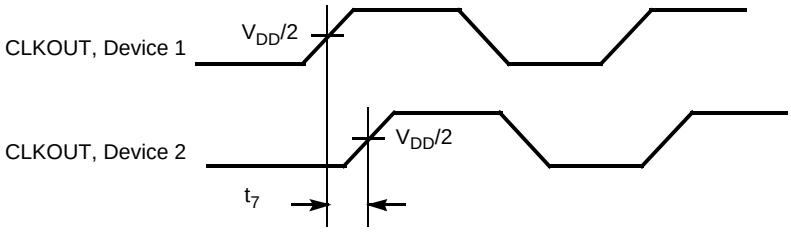
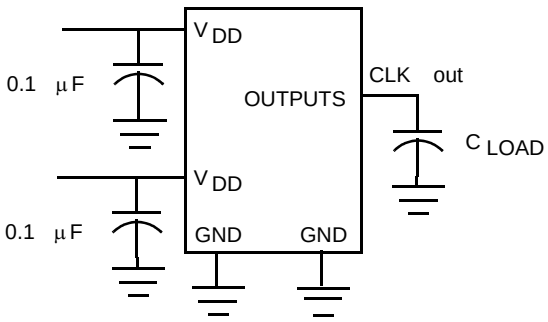


Figure 7. Device-Device Skew

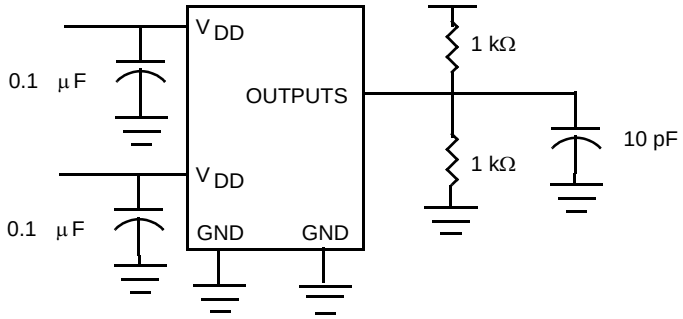


Test Circuits

Test Circuit # 1



Test Circuit # 2



For parameter t_8 (output slew rate) on -1H devices

Ordering Information

Ordering Code	Package Type	Operating Range
Pb-Free - CY2305C		
CY2305CSXC-1	8-pin 150 Mil SOIC	Commercial
CY2305CSXC-1T	8-pin 150 Mil SOIC – Tape and Reel	Commercial
CY2305CSXC-1H	8-pin 150 Mil SOIC	Commercial
CY2305CSXC-1HT	8-pin 150 Mil SOIC – Tape and Reel	Commercial
CY2305CSXI-1	8-pin 150 Mil SOIC	Industrial
CY2305CSXI-1T	8-pin 150 Mil SOIC – Tape and Reel	Industrial
CY2305CSXI-1H	8-pin 150 Mil SOIC	Industrial
CY2305CSXI-1HT	8-pin 150 Mil SOIC – Tape and Reel	Industrial
Pb-Free- CY2309C		
CY2309CSXC-1	16-pin 150 Mil SOIC	Commercial
CY2309CSXC-1T	16-pin 150 Mil SOIC – Tape and Reel	Commercial
CY2309CSXC-1H	16-pin 150 Mil SOIC	Commercial
CY2309CSXC-1HT	16-pin 150 Mil SOIC – Tape and Reel	Commercial
CY2309CSXI-1	16-pin 150 Mil SOIC	Industrial
CY2309CSXI-1T	16-pin 150 Mil SOIC – Tape and Reel	Industrial
CY2309CSXI-1H	16-pin 150 Mil SOIC	Industrial
CY2309CSXI-1HT	16-pin 150 Mil SOIC – Tape and Reel	Industrial
CY2309CZXC-1	16-pin 4.4 mm TSSOP	Commercial
CY2309CZXC-1T	16-pin 4.4 mm TSSOP – Tape and Reel	Commercial
CY2309CZXC-1H	16-pin 4.4 mm TSSOP	Commercial
CY2309CZXC-1HT	16-pin 4.4 mm TSSOP – Tape and Reel	Commercial
CY2309CZXI-1	16-pin 4.4 mm TSSOP	Industrial
CY2309CZXI-1T	16-pin 4.4 mm TSSOP – Tape and Reel	Industrial
CY2309CZXI-1H	16-pin 4.4 mm TSSOP	Industrial
CY2309CZXI-1HT	16-pin 4.4 mm TSSOP – Tape and Reel	Industrial

Package Drawing and Dimensions

Figure 8. 8-Pin (150 Mil) SOIC S8

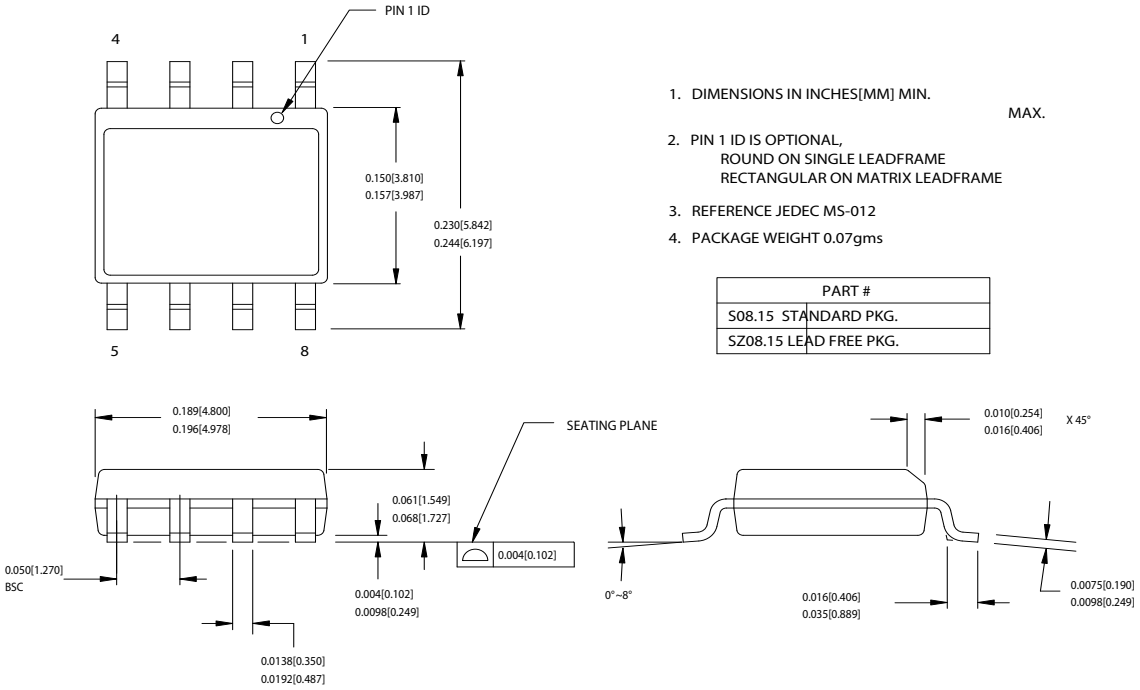


Figure 9. 16-Pin (150 Mil) SOIC S16

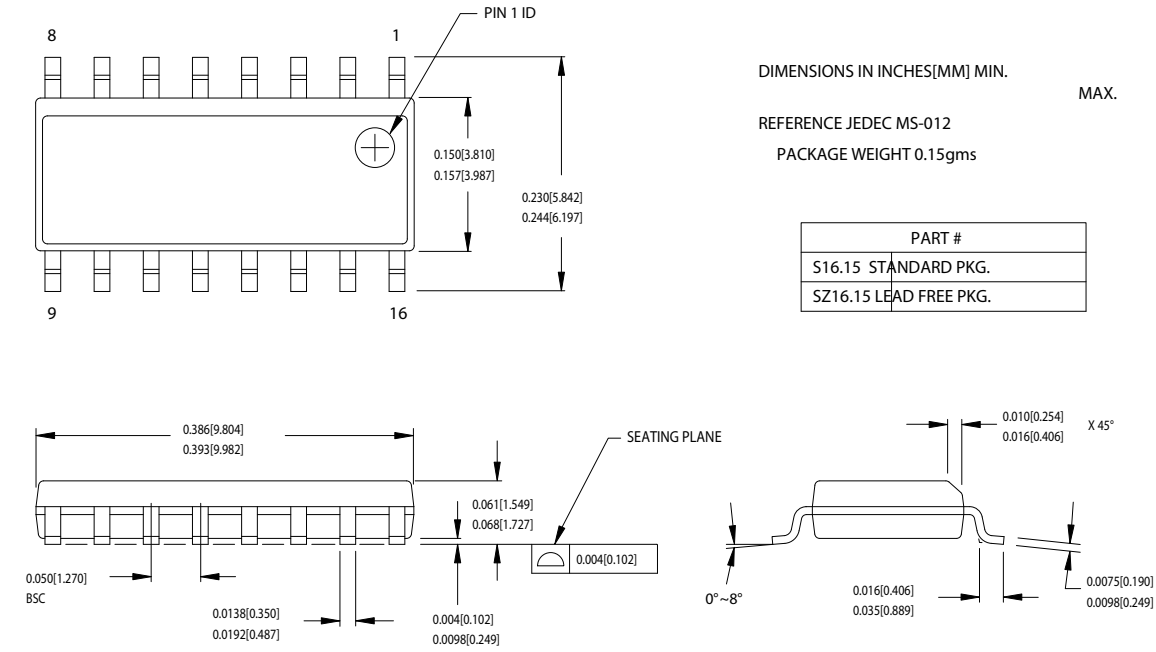
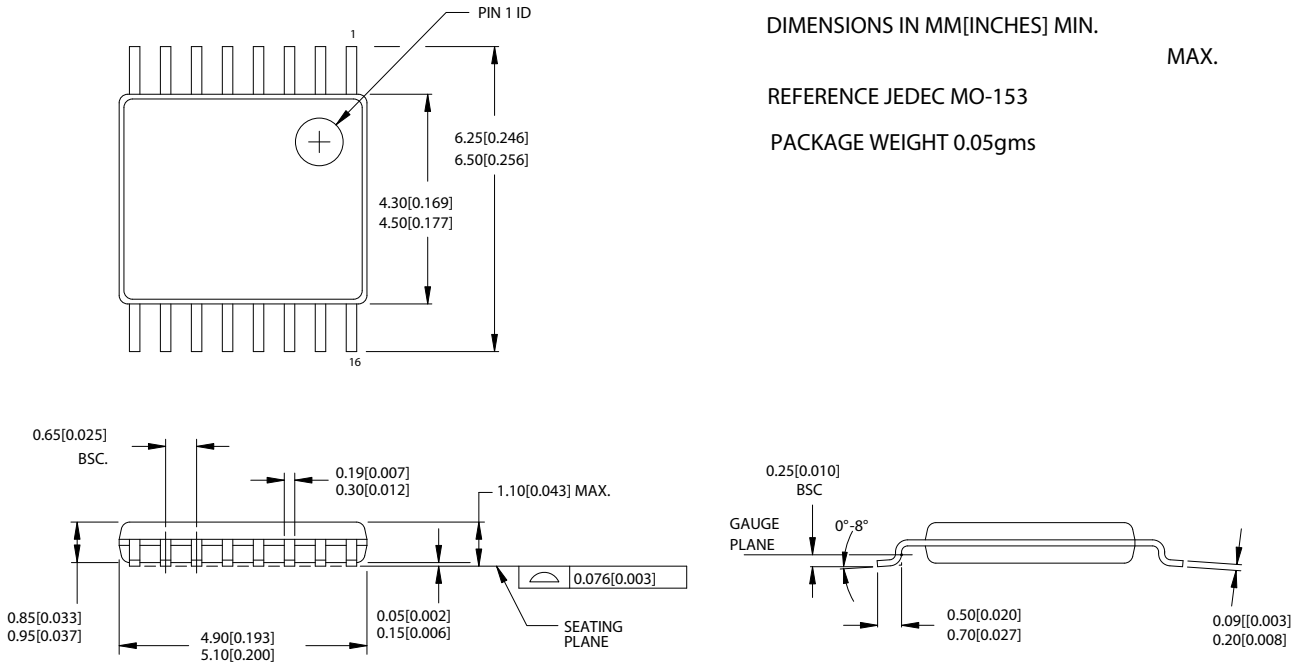


Figure 10. 16-Pin TSSOP 4.40 MM Body Z16.173



Document History Page

Document Title: CY2305C CY2309C 3.3V Zero Delay Clock Buffer Document Number: 38-07672				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	224421	See ECN	RGL	New datasheet
*A	268571	See ECN	RGL	Added bullet for 5V tolerant inputs in the features
*B	276453	See ECN	RGL	Minor Change: Moved one sentence from the features to the Functional Description
*C	303063	See ECN	RGL	Updated datasheet as per characterization data
*D	318315	See ECN	RGL	Datasheet rewrite
*E	344815	See ECN	RGL	Minor Error: Corrected the header of all the AC/DC tables with the right part numbers.
*F	1279889	See ECN	KVM	Changed title from “Low Cost 3.3V Zero Delay Buffer” to “3.3V Zero Delay Clock Buffer” Specified the VIL minimum value to -0.3V Specified the VIH maximum value to VDD + 0.3V Changed DC Input Voltage (REF) maximum value in Absolute Maximum section Removed references to 5V tolerant inputs (pages 1 and 2) Removed Pentium compatibility reference Added CY2305C block diagram Added “peak” to the jitter specifications Changed typical jitter from 75 ps to 50 ps for standard drive devices For standard drive devices, tightened rise/fall times from 2.5 ns to 2.25 ns Tightened cycle-to-cycle jitter from 200 ps to 175 ps Tightened output-to-output skew from 250 ps to 200 ps