FOUR PORT BYPASS FOR FC-AL S2071

FEATURES

- Micropower Bipolar Technology
- ANSI X3T11 Fibre Channel Compatible
- Four Port Bypass Circuits
- Suitable for both Coaxial and Optical Link
- Nominal deterministic Jitter ± 10ps
- Low Power Operation 0.73 W Typical
- 44 Pin PQFP Package
- 3.3V Supply

APPLICATIONS

- RAID
- JBOD
- FC-AL Nodes

GENERAL DESCRIPTION

The Four Port Bypass for FC-AL Circuit is used in full-speed (1.0625 Gbps) Disk Arrays. It contains four port bypass circuits. The S2071 may be used to implement a single chip Arbitrated Loop Port Bypass Node. The S2071 performs the function of four port bypass circuits.

FUNCTIONAL DESCRIPTION

The S2071 functional block diagram is shown in Figure 1. The S2071 performs the function of a Port Bypass Circuit (PBC) for nodes in a FC-AL system. The low jitter accumulation of the port bypass path is essential in these systems.

Jitter Performance

The primary AC parameter of importance is determinsitic jitter accumulation (data eye degradation) inserted by the port bypass circuit. The S2071 utilizes high bandwidth, low skew differential circuitry to provide symmetric rise and fall times and excellent noise immunity.

For arrays of disk drives greater than 4, it is recommended that the S2071 be cascaded with the S2058 (Port Bypass with Repeater) in a ratio of 1:1 to perform clock and data retiming. This ensures optimal jitter performance for the disk array system.

Figure 1. S2071 Functional Block Diagram

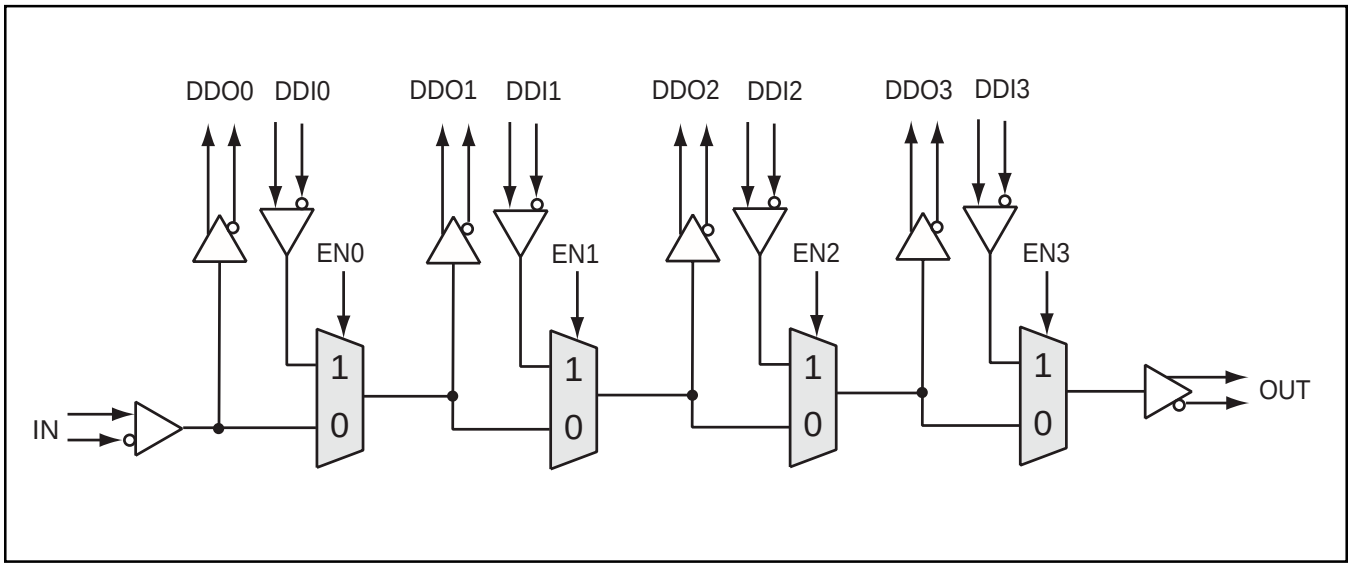


Figure 2. FC-AL JBOD Application for Repeaters

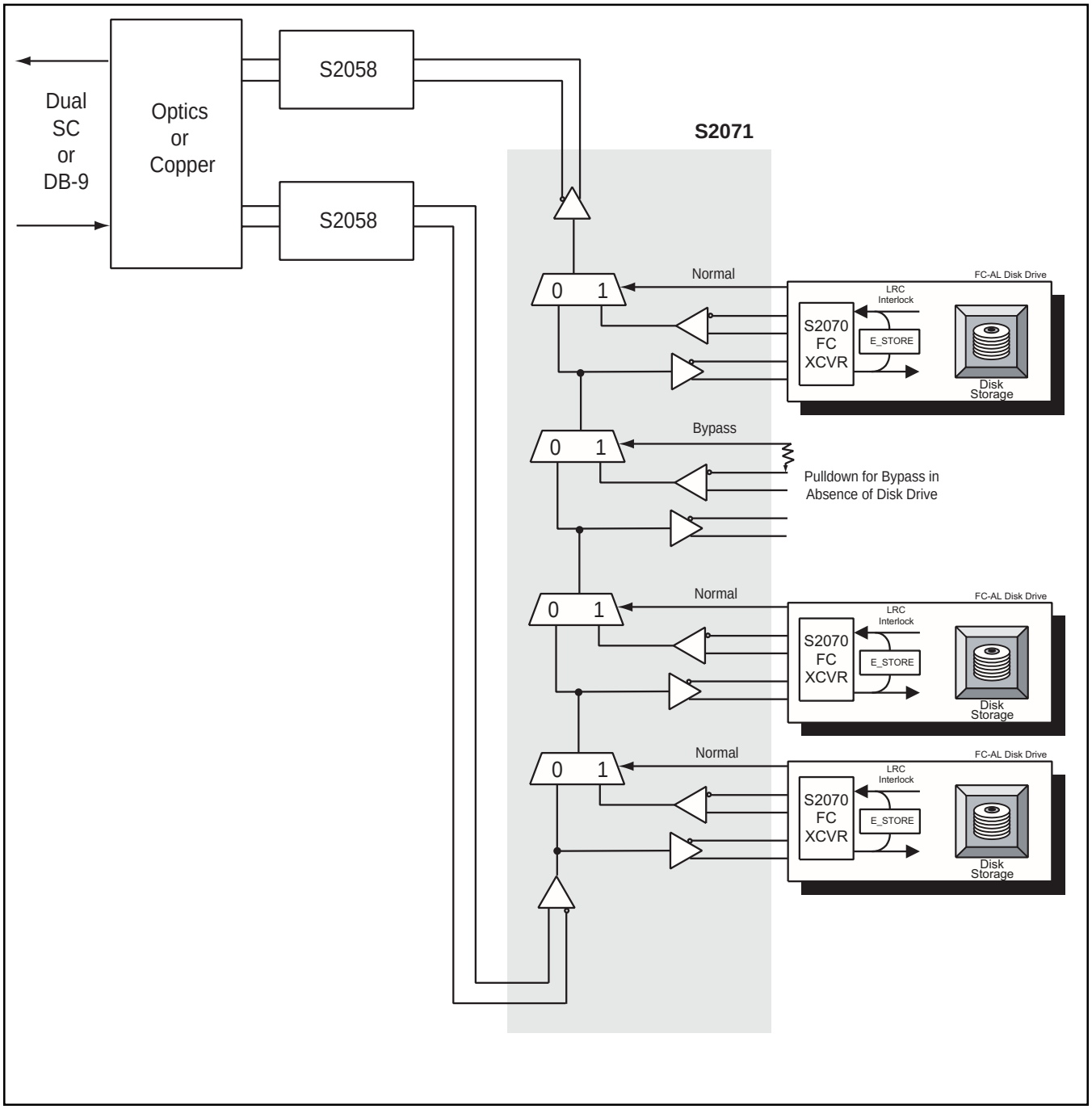


Table 1. Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin#	Description
OUTP OUTN	Diff. LVPECL	O	24 25	Serial output to be connected to the next PBC in the loop. (See Figure 2.)
INN INP	Diff. LVPECL	I	9 10	Serial input from the previous Port Bypass Circuit.
DDI0P DDI0N DDI1P DDI1N DDI2P DDI2N DDI3P DDI3N	Diff. LVPECL	I	4 3 41 40 35 34 28 27	Serial input to the port bypass. These inputs should be driven by the FC-AL disk drive connected to the port bypass.
DDO0P DDO0N DDO1P DDO1N DDO2P DDO2N DDO3P DDO3N	LVPECL	O	7 6 44 43 38 37 31 30	Port bypass output pairs. These outputs should drive the input ports of the FC-AL disk drive.
EN0 EN1 EN2 EN3	TTL	I	15 16 17 18	Port Bypass Control. Active High. When EN is inactive, the port bypass will be in bypass mode. When EN is active, port bypass will be in normal mode.
GND	Ground		1, 8, 11, 12,13, 19, 22, 23, 33, 39,	Ground pins are physically mounted to the die surface, and are an important part of the thermal path. For best thermal performance, all ground pins should be connected to a ground plane, using multiple vias if possible.
VCC			2, 5, 14, 20, 21, 26, 29, 32, 36, 42	+3.3V Power supply.

Figure 3. S2071 Pinout Package

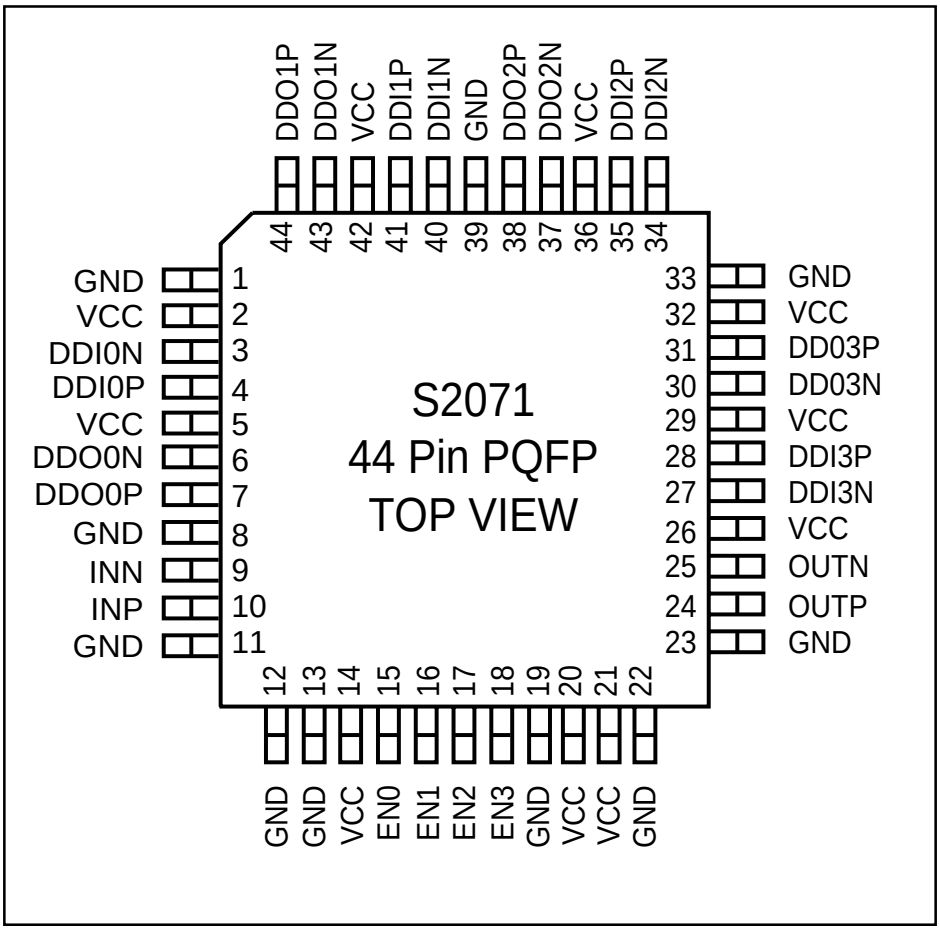
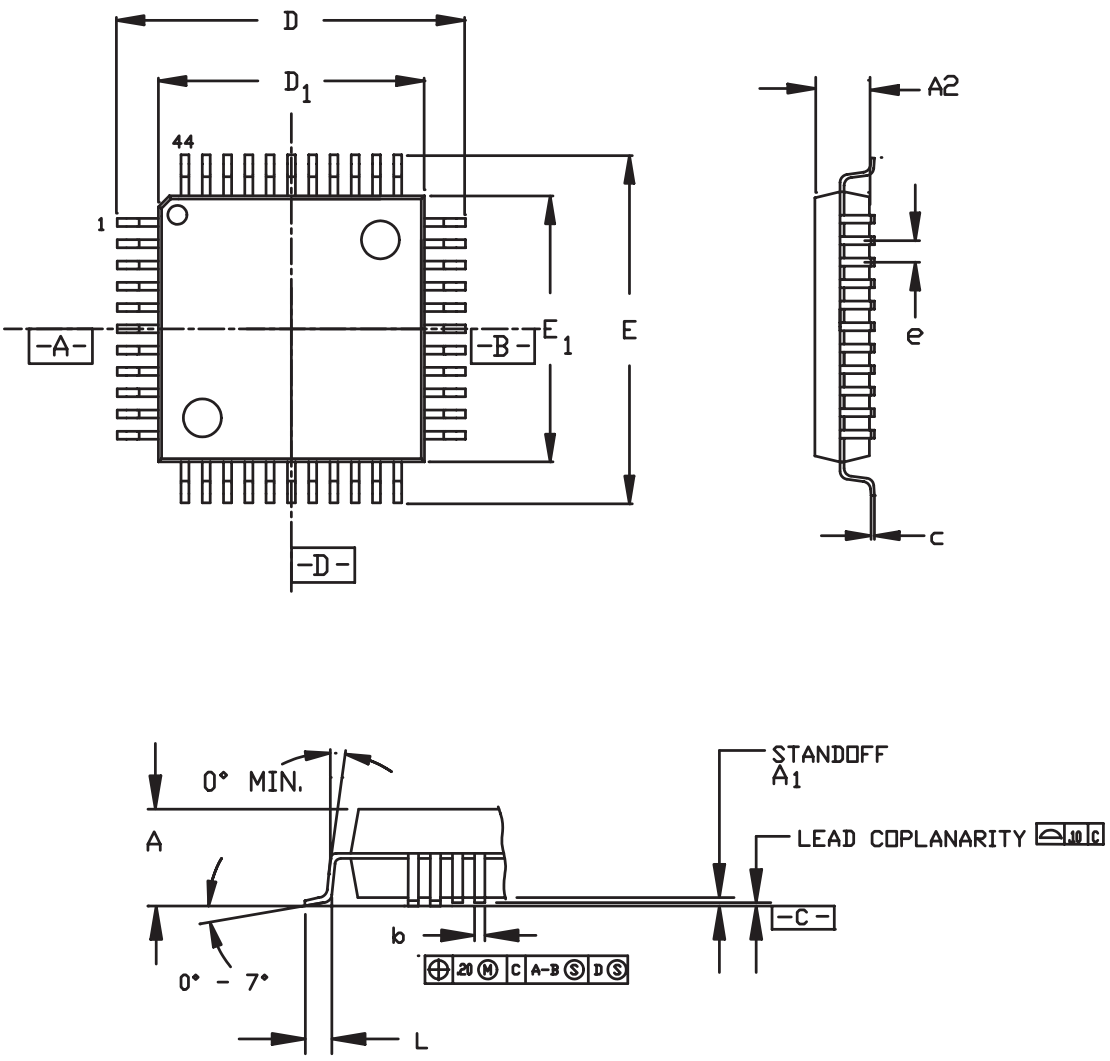


Figure 4. S2071 44 Pin PQFP Package



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	e	b	c
MIN		0.10	1.95	12.95	9.90	12.95	9.90	0.78	0.80 BSC.	0.30	
NOM			2.00	13.20	10.00	13.20	10.00	0.88		0.35	
MAX	2.45	0.50	2.10	13.45	10.10	13.45	10.10	1.03		0.45	0.17

Thermal Management

Device	Max Package Power[1]	Θ_{JA}
S2071	0.99 W	55 ° C/W

1. Power is measured with outputs terminated.

Table 2. AC Charateristics *(Over recommended operating conditions)*

Parameter	Description	Min	Typ	Max	Units	Conditions
T_{RDDO} T_{FDDO}	Serial Data Rise and Fall time DDO, OUT.		185	350	ps	20% to 80% tested on a sample basis.
T_{DD}	Any input to any output.			4	ns	Prop. delay. See Figure 5.
ΔV_{OUT}	LVPECL Output differential peak-to-peak voltage swing.	1000		2200	mVp-p	Tested with 50 Ω to V_{CC} -2.0V. See Figure 6.
ΔV_{IN}	Receiver differential peak-to-peak input sensitivity.	200		2600	mVp-p	V_{CC} = 3.3 V, AC coupled. Internally DC biased to V_{CC} -0.5V. See Figure 6.
T_{jitter}RMS	Random jitter accumulation, any input to any output.		3	5	ps	RMS output jitter accumulated with K28.7 code. Tested on a sample basis.
T_{jitter}DJ	Deterministic jitter accumulation, any input to any output.		±10	±40	ps	Deterministic output jitter accumulated K28.5 pattern. Tested on a sample basis.

Table 3. LVTTL DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input High Voltage (TTL)	2.0			V	
V_{IL}	Input Low Voltage (TTL)			0.8	V	
I_{IH}	Input High Current (TTL)			50	µA	V_{IN} = 2.4V
I_{IL}	Input Low Current (TTL)	-500		0	µA	V_{IN} = 0.5V

Table 4. LVPECL Input/Output DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage	Vcc -1.15			V	
V_{OL}	Output Low Voltage			Vcc -1.65	V	
V_{IH}	Input High Voltage	Vcc -1.2		Vcc -0.5	V	
V_{IL}	Input Low Voltage	Vcc -2.0		Vcc -1.4	V	
I_{IH}	Input High Current	-250		200	µA	
I_{IL}	Input Low Current	-250		200	µA	

Table 5. Absolute Maximum Ratings[1]

Parameter	Min	Typ	Max	Units
TTL Power Supply Voltage (V_{CC})	0.5		+4	V
PECL DC Input Voltage (V_{INP})	-0.5		V_{CC}+0.5	V
TTL DC Input Voltage (V_{INP})	-0.5		5.5	V
DC Voltage applied to outputs for High output state ($V_{IN\ TTL}$)	-0.5		V_{CC}+0.5	V
PECL Output Current (I_{OUT}) (DC, Output High)			24	mA
Storage Temperature (T_{STG})	-65		150	˚C

1. CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Eletrostatic Discharge (ESD) Ratings

The S2071 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1000 V.

Table 6. Recommended Operating Conditions [1]

Parameter	Min	Typ	Max	Units
Power Supply Voltage (V_{CC})	+3.13		+3.47	V
Junction Temperature Under Bias			130	˚C
Ambient Operating Temperature Range (T)	0		70	˚C
ICC Current Supply[2]		220	260	mA
Voltage on an input pin	V_{CC}–2		V_{CC}	V

1. AMCC guarantees the functional and parametric operation of the part under "Recommended Operating Conditions," except where specifically noted in the AC and DC Parametric Tables.
2. ICC is measured with outputs not terminated.

POWER SEQUENCING

When the S2071 is operated with a 5 volt controller, it is recommended that power be applied to the S2071 before or simultaneously (time difference less than 1 ms) with the application of power to the 5 volt controller. If this condition cannot be met, series resistance of at least 33 Ohms is required on all TTL inputs driven from the 5 volt environment.

Static control lines such as EN[3:0] should also be provided with series resistors of at least 33 Ohms (100 Ohms recommended) to limit input current if the 5 volt environment is powered while the 3.3 volt VCC of the S2071 is off.

Figure 5. Timing Waveforms

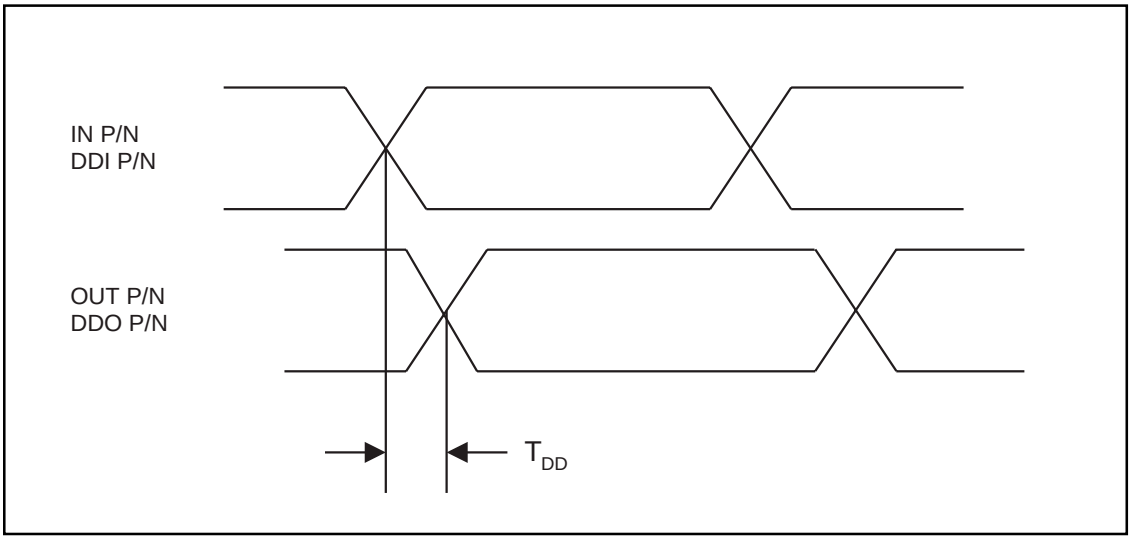
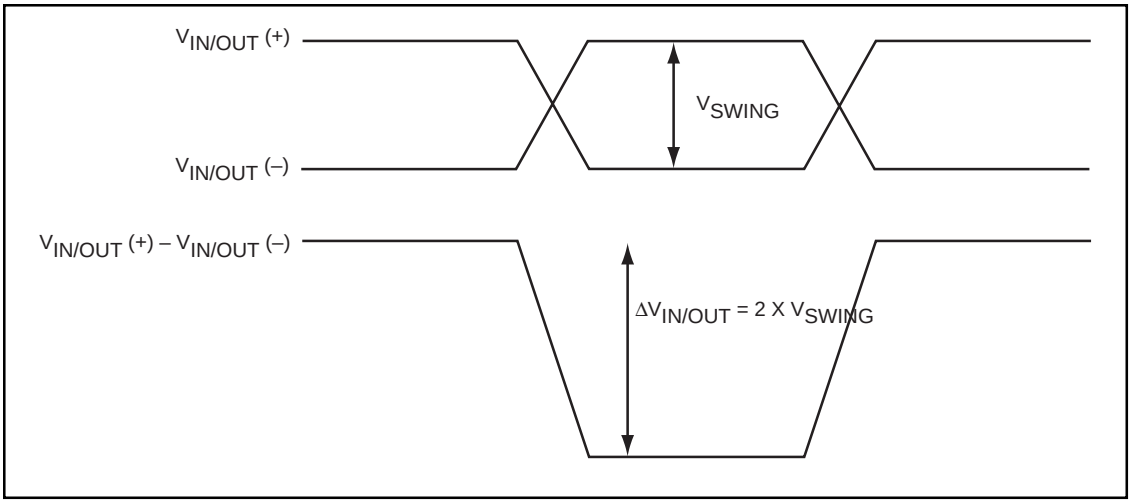


Figure 6. Differential Input/Output Voltage



Note: $V_{IN/OUT}$ (+) – $V_{IN/OUT}$ (–) is the algebraic difference of the input/output signals.

Figure 7. Output Circuit

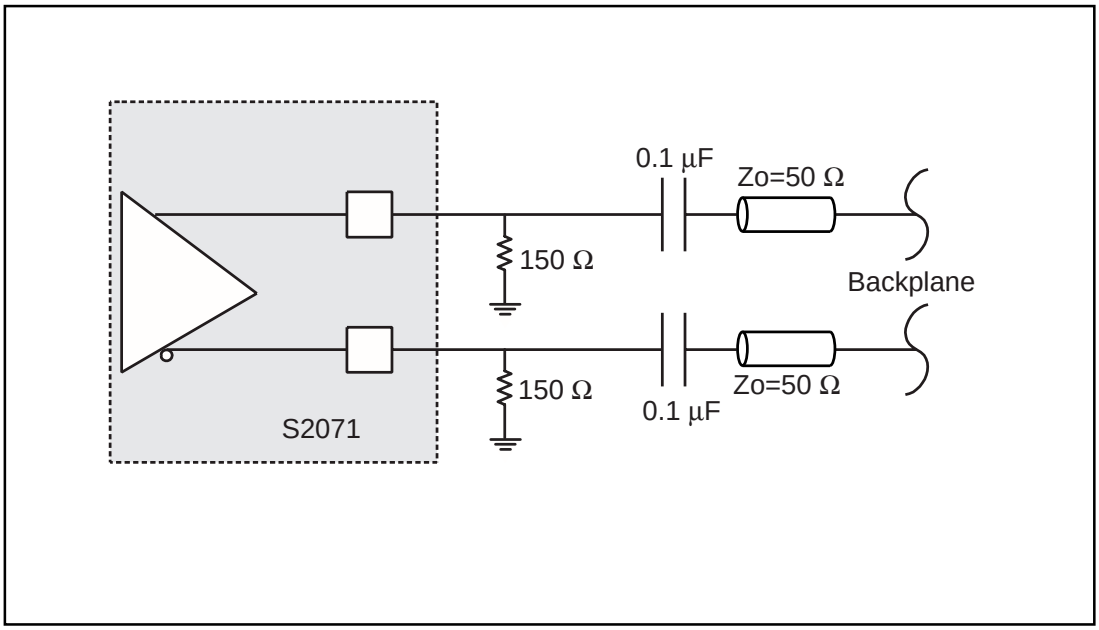
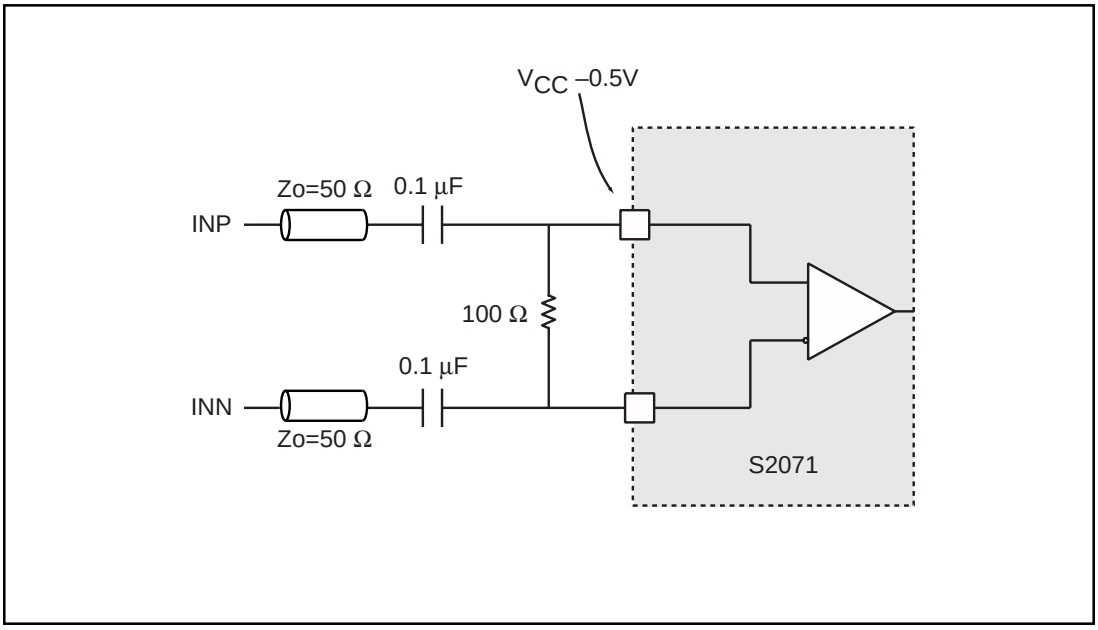
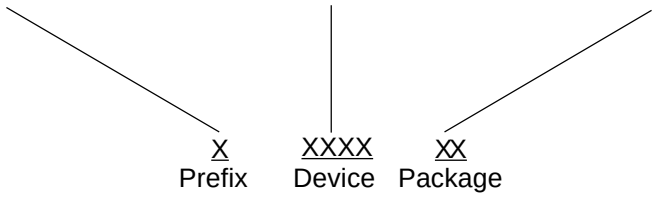


Figure 8. High Speed Differential Inputs



Ordering Information

PREFIX	DEVICE	PACKAGE
S- Integrated Circuit	2071	QF – 44 Pin PQFP



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