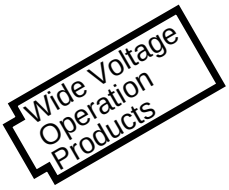
EPSON

E0C6274

4-bit Single Chip Microcomputer



- Core CPU Architecture
- Dual Slope Type A/D Converter
- Reference Voltage Generation Circuit
- General Purpose Operating Amplifier
- SVD Circuit

■ DESCRIPTION

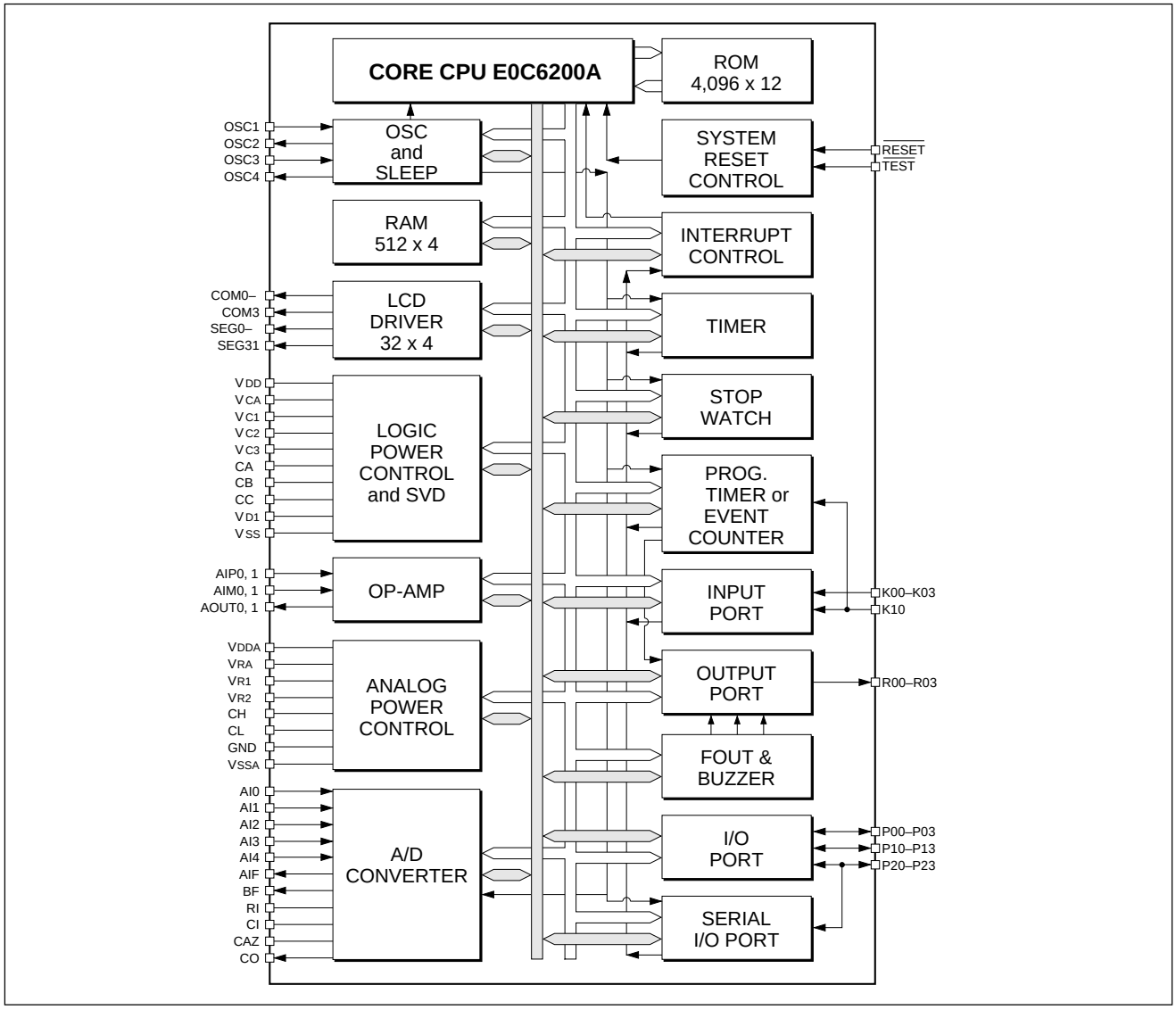
The E0C6274 is a single-chip microcomputer made up of the 4-bit core CPU E0C6200A, ROM, RAM, LCD driver, input ports, output ports, I/O ports, clock timer, stopwatch timer, programmable timer, clock-synchronized serial interface, general purpose operational amplifier, dual slope type A/D converter and watchdog timer. Because of its low-voltage operation and low power consumption, this series is ideal for a wide range of applications, and is especially suitable for battery-driven systems.

■ FEATURES

- CMOS LSI 4-bit parallel processing
- Clock ..... 32.768kHz/1MHz (Typ.)
- Instruction set ..... 109 instructions
- Instruction execution time ..... When operated 32kHz : 153µsec, 214µsec, 366µsec
  When operated 1MHz : 5µsec, 7µsec, 12µsec
- ROM capacity ..... 4,096 words, 12 bits per word
- RAM capacity ..... 512 words, 4 bits per word
- A/D converter ..... Dual slope A/D converter
  Resolution/conversion speed: programmable
  (Need changed external parts)
  6400 count: 500ms/3200 count: 250ms
  1600 count: 125ms/800 count: 62.5ms
  A/D conversion accuracy: ±0.2%
  (Zone of temperature: 0°C to 50°C)
  Analog measuring: programmable
  (Voltage/difference voltage/resistor: measuring)
  Analog voltage inputs: 5 channels
  Reference voltage generation circuit
  Middle electric potential (GND) generation circuit
- Built-in operational amplifier ..... 2 MOS input Op-Amps
- Input port ..... 5 bits
  (Selected by mask option: with or without pull-up resistor)
- Output port ..... 4 bits
  (Clock output and buzzer output are available by mask option)
- Built-in stopwatch timer
- Built-in watchdog timer
- I/O port ..... 12 bits
  (Combine serial I/O ports clock: changed through software)
- Serial I/O port ..... 1 port (Clock synchronous/8 bits)
- LCD driver ..... Either 32 segments × 1, 2, 3 or 4 commons
  (Selected through software)
  Regulated voltage circuit and booster voltage circuit built-in
  (Correspond to 3.0V to 4.5V LCD: VR adjustment)
- Timer ..... Time base counter 2ch.
  Programmable timer/event counter (8 bits) 1ch.

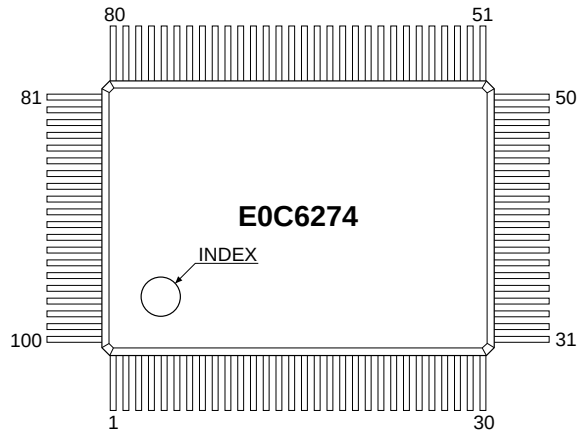
- Supply voltage detective (SVD) circuit built-in ..... 2.3V/2.4V/2.5V/2.6V Programmable (accuracy ± 100mV)
- Interrupts ..... External : Input interrupt 2 lines
  Internal : Timer interrupt 3 lines
  Serial I/O interrupt 1 line
  A/D interrupt 1 line
- Supply voltage ..... Operating : 2.4V to 5.5V (Single external power supply)
  No operating : 1.8V to 5.5V (Single external power supply)
- Current consumption ..... SLEEP mode : 0.7µA (3V, stop oscillation)
  HALT mode : 2.0µA (3V, 32kHz)
  OPERATING mode : 6.0µA (3V, 32kHz)
  : 200µA (3V, 1MHz)
  (A/D operation) : 306µA (3V, 32kHz)
  : 506µA (3V, 32kHz, operated OP-AMP)
- Package ..... QFP5-100pin (plastic), QFP15-100pin (plastic)
  Die form

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

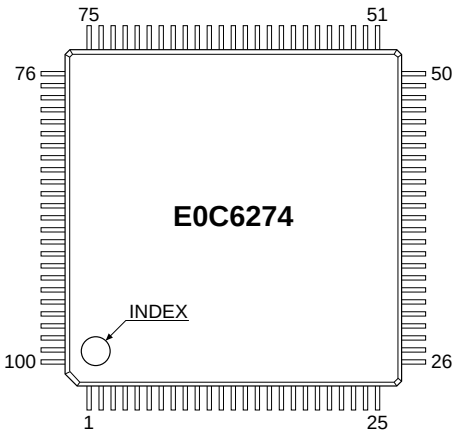
QFP5-100pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	K02	26	P22	51	SEG10	76	AI3
2	K01	27	P23	52	SEG11	77	AI2
3	K00	28	$\overline{\text{RESET}}$	53	SEG12	78	V_{SSA}
4	N.C.	29	$\overline{\text{TEST}}$	54	SEG13	79	AI1
5	N.C.	30	CC	55	SEG14	80	AI0
6	V_{SS}	31	CB	56	SEG15	81	CI
7	OSC1	32	CA	57	SEG16	82	CAZ
8	OSC2	33	V_{C3}	58	SEG17	83	BF
9	OSC3	34	V_{C2}	59	SEG18	84	RI
10	OSC4	35	V_{C1}	60	SEG19	85	CH
11	V_{DD}	36	V_{CA}	61	SEG20	86	CL
12	R03	37	COM3	62	SEG21	87	GND
13	R02	38	COM2	63	SEG22	88	V_{DDA}
14	R01	39	COM1	64	SEG23	89	AOUT0
15	R00	40	COM0	65	SEG24	90	AIP0
16	P00	41	SEG0	66	SEG25	91	AIM0
17	P01	42	SEG1	67	SEG26	92	AIP1
18	P02	43	SEG2	68	SEG27	93	AIM1
19	P03	44	SEG3	69	SEG28	94	AOUT1
20	P10	45	SEG4	70	SEG29	95	V_{R1}
21	P11	46	SEG5	71	SEG30	96	V_{R2}
22	P12	47	SEG6	72	SEG31	97	V_{RA}
23	P13	48	SEG7	73	CO	98	V_{D1}
24	P20	49	SEG8	74	AIF	99	K10
25	P21	50	SEG9	75	AI4	100	K03

N.C. = No Connection

QFP15-100pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	K00	26	$\overline{\text{RESET}}$	51	SEG12	76	V_{SSA}
2	N.C.	27	$\overline{\text{TEST}}$	52	SEG13	77	AI1
3	N.C.	28	CC	53	SEG14	78	AI0
4	V_{SS}	29	CB	54	SEG15	79	CI
5	OSC1	30	CA	55	SEG16	80	CAZ
6	OSC2	31	V_{C3}	56	SEG17	81	BF
7	OSC3	32	V_{C2}	57	SEG18	82	RI
8	OSC4	33	V_{C1}	58	SEG19	83	CH
9	V_{DD}	34	V_{CA}	59	SEG20	84	CL
10	R03	35	COM3	60	SEG21	85	GND
11	R02	36	COM2	61	SEG22	86	V_{DDA}
12	R01	37	COM1	62	SEG23	87	AOUT0
13	R00	38	COM0	63	SEG24	88	AIP0
14	P00	39	SEG0	64	SEG25	89	AIM0
15	P01	40	SEG1	65	SEG26	90	AIP1
16	P02	41	SEG2	66	SEG27	91	AIM1
17	P03	42	SEG3	67	SEG28	92	AOUT1
18	P10	43	SEG4	68	SEG29	93	V_{R1}
19	P11	44	SEG5	69	SEG30	94	V_{R2}
20	P12	45	SEG6	70	SEG31	95	V_{RA}
21	P13	46	SEG7	71	CO	96	V_{D1}
22	P20	47	SEG8	72	AIF	97	K10
23	P21	48	SEG9	73	AI4	98	K03
24	P22	49	SEG10	74	AI3	99	K02
25	P23	50	SEG11	75	AI2	100	K01

N.C. = No Connection

■ PIN DESCRIPTION

Pin name	Pin No.		In/Out	Function
	QFP5-100pin	QFP15-100pin		
V_{DD}	11	9	(I)	Power source (+) terminal
V_{SS}	6	4	(I)	Power source (-) terminal
V_{DDA}	88	86	(I)	Analog system power source (+) terminal
V_{SSA}	78	76	(I)	Analog system power source (-) terminal
GND	87	85	(I/O)	Analog system ground terminal
V_{D1}	98	96	–	Oscillation and internal logic system regulated voltage output terminal
V_{C1}	35	33	–	LCD system regulated voltage output terminal
V_{C2}	34	32	–	LCD system booster output terminal (V_{C1} x 2)
V_{C3}	33	31	–	LCD system booster output terminal (V_{C1} x 3)
V_{CA}	36	34	–	LCD system voltage adjustment terminal
CA–CC	32–30	30–28	–	Booster capacitor connecting terminal
OSC1	7	5	I	Crystal oscillation input terminal
OSC2	8	6	O	Crystal oscillation output terminal
OSC3	9	7	I	Ceramic or CR oscillation input terminal (selected by mask option)
OSC4	10	8	O	Ceramic or CR oscillation output terminal (selected by mask option)
K00–K10	3–1, 100, 99	1, 100–97	I	Input terminal
P00–P13	16–23	14–21	I/O	I/O terminal
P20–P23	24–27	22–25	I/O	I/O terminal or serial input/output terminal
R00–R03	15–12	13–10	O	Output terminal (DC, buzzer or clock output may be selected by mask option)
COM0–3	40–37	38–35	O	LCD common output terminal
SEG0–31	41–72	39–70	O	LCD segment output terminal (Convertible to DC output by mask option)
AI0–AI4	80, 79, 77–75	78, 77, 75–73	I	Analog input terminal
AIF	74	72	–	Analog input filter condenser connecting terminal
CAZ	82	80	–	Auto zero adjustment condenser connecting terminal
CI	81	79	–	Integral condenser connecting terminal
RI	84	82	–	Integral resistance connecting terminal
BF	83	81	–	Buffer amplifier output terminal
CO	73	71	–	Testing output terminal
CH	85	83	–	Reference voltage control condenser connecting terminal
CL	86	84	–	Reference voltage control condenser connecting terminal
V_{R1}	95	93	(I)	Reference voltage for resistance measurement
V_{R2}	96	94	(I)	Reference voltage for voltage measurement
V_{RA}	97	95	–	Reference voltage adjustment terminal
AIP0	90	88	I	AMP 0 non-inverted input terminal
AIM0	91	89	I	AMP 0 inverted input terminal
AOUT0	89	87	O	AMP 0 output terminal
AIP1	92	90	I	AMP 1 non-inverted input terminal
AIM1	93	91	I	AMP 1 inverted input terminal
AOUT1	94	92	O	AMP 1 output terminal
$\overline{RESET}$	28	26	I	Initial reset input terminal
$\overline{TEST}$	29	27	I	Test input terminal

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
Input voltage (1)	V_I	-0.5 to V_{DD} + 0.3	V
Input voltage (2)	V_{IOSC}	-0.5 to V_{D1} + 0.3	V
Permissible total output current *1	ΣI_{VDD}	10	mA
Operating temperature (1)	$Topr_1$	-20 to 70	°C
Operating temperature (2) *2	$Topr_2$	0 to 50	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *3	P_D	250	mW

∗1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
∗2: The A/D converter and AMP circuit are ON status.
∗3: In case of plastic package (QFP5-100pin, QFP15-100pin).

● Recommended Operating Conditions

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	V_{SS}=0V	2.2	3.0	5.5	V
		V_{SS}=0V, When A/D converter or AMP is used	2.4	3.0	5.5	V
Oscillation frequency (1)	f_{OSC1}		–	32.768	–	kHz
Oscillation frequency (2)	f_{OSC3}	duty 50±5%	50	1,000	1,300	kHz

● DC Characteristics

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{D1}/V_{C1}–V_{C3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–K03, K10, SIN, $\overline{SCLK}$ P00–P03, P10–P13, P20–P23	0.8•V_{DD}		V_{DD}	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$, $\overline{TEST}$	0.9•V_{DD}		V_{DD}	V
Low level input voltage (1)	V_{IL1}		K00–K03, K10, SIN, $\overline{SCLK}$ P00–P03, P10–P13, P20–P23	0		0.2•V_D	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$, $\overline{TEST}$	0		0.1•V_{DD}	V
High level input current	I_{IH}	V_{IH}=3.0V	K00–K03, K10, SIN, $\overline{SCLK}$ P00–P03, P10–P13, P20–P23 $\overline{RESET}$, $\overline{TEST}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} With pull up resistor	K00–K03, K10, SIN, $\overline{SCLK}$ P00–P03, P10–P13, P20–P23 $\overline{RESET}$	-20	-10	-5	µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} No pull up resistor	K00–K03, K10, SIN, $\overline{SCLK}$ P00–P03, P10–P13, P20–P23	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.9•V_{DD}	R00, R01, P00–P03, P10–P13 P20–P23, SOUT, $\overline{SCLK}$, $\overline{SRDY}$			-0.9	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.9•V_{DD}	R02, R03			-1.8	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.1•V_{DD}	R00, R01, P00–P03, P10–P13 P20–P23, SOUT, $\overline{SCLK}$, $\overline{SRDY}$	3.0			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.1•V_{DD}	R02, R03	6.0			mA
Common output current	I_{OH3}	V_{OH3}=V_{C3}-0.05V	COM0–COM3			-3	µA
	I_{OL3}	V_{OL3}=0.05V		3			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=V_{C3}-0.05V	SEG0–SEG31			-3	µA
	I_{OL4}	V_{OL4}=0.05V		3			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.9•V_{DD}	SEG0–SEG31			-0.2	mA
	I_{OL5}	V_{OL5}=0.1•V_{DD}		0.2			mA

● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: V_{DD}=V_{DDA}=3.0V, V_{SS}=V_{SSA}=0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{D1}/V_{C1}–V_{C3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{C1}	V_{CA}=V_{C1}, I_{C1}=-5µA		0.95	1.05	1.15	V
	V_{C2}	Connect 1MΩ load resistor between V_{SS} and V_{C2} (without panel load)		2•V_{C1} ×0.9		2•V_{C1} +0.1	V
	V_{C3}	Connect 1MΩ load resistor between V_{SS} and V_{C3} (without panel load)		3•V_{C1} ×0.9		3•V_{C1} +0.1	V
SVD voltage	V_{SVD}	SVDS="0"		2.5	2.6	2.7	V
		SVDS="1"		2.4	2.5	2.6	V
		SVDS="2"		2.3	2.4	2.5	V
		SVDS="3"		2.2	2.3	2.4	V
SVD circuit response time	t_{SVD}					100	µS
Current consumption	I_{OP}	During SLEEP	Current that flows in external parts (loads) such as the LCD panel is not included.		0.7	2.0	µA
		During HALT (32kHz)			2.0	7.0	µA
		During execution (32kHz) *1			6.0	15.0	µA
		During execution (1MHz) *1			200	500	µA
		During execution (32kHz) *2			306	915	µA
		During execution (32kHz) *3			506	1515	µA
		During execution (32kHz) *4			16.0	45.0	µA

∗1: The SVD, A/D converter and AMP circuits are OFF status.
∗2: The A/D converter (reference voltage V_{R1} and middle electric potential GND are supplied from outside) is ON status. The SVD and AMP circuits are OFF status.
∗3: The A/D converter (reference voltage V_{R1} and middle electric potential GND are supplied from outside) and AMP circuits (2 systems) are ON status. The SVD circuit is OFF status.
∗4: The SVD circuit is ON status. The A/D converter and AMP circuits are OFF status.

A/D converter

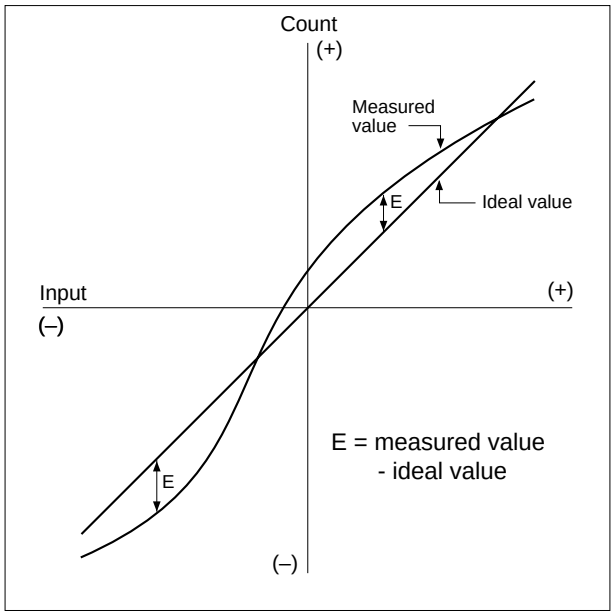
(Unless otherwise specified: V_{DD}=V_{DDA}=3.0V, V_{SS}=V_{SSA}=0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{D1}/V_{C1}–V_{C3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Absolute error	E_{V1}	Voltage measurement mode	6400 counts, R_I = 680 kΩ	0	±3	±13	Count
	E_{V2}		3200 counts, R_I = 330 kΩ	0	±2	±7	
	E_{V3}		1600 counts, R_I = 180 kΩ	0	±1	±4	
	E_{V4}		800 counts, R_I = 82 kΩ	0	±1	±4	
	E_{D1}	Differential voltage measurement mode	6400 counts, R_I = 680 kΩ	0	±4	±16	Count
	E_{D2}		3200 counts, R_I = 330 kΩ	0	±2	±8	
	E_{D3}		1600 counts, R_I = 180 kΩ	0	±1	±5	
	E_{D4}		800 counts, R_I = 82 kΩ	0	±1	±5	
	E_{R1}	Resistance measurement mode	6400 counts, R_I = 680 kΩ	0	±9	±20	Count
	E_{R2}		3200 counts, R_I = 330 kΩ	0	±4	±10	
	E_{R3}		1600 counts, R_I = 180 kΩ	0	±2	±5	
	E_{R4}		800 counts, R_I = 82 kΩ	0	±2	±5	
Zero point error	E_{ZV1}	Voltage measurement mode	6400 counts, R_I = 680 kΩ	0	0	±4	Count
	E_{ZV2}		3200 counts, R_I = 330 kΩ	0	0	±2	
	E_{ZV3}		1600 counts, R_I = 180 kΩ	0	0	±2	
	E_{ZV4}		800 counts, R_I = 82 kΩ	0	0	±2	
	E_{ZD1}	Differential voltage measurement mode	6400 counts, R_I = 680 kΩ	0	1	±5	Count
	E_{ZD2}		3200 counts, R_I = 330 kΩ	0	0	±3	
	E_{ZD3}		1600 counts, R_I = 180 kΩ	0	0	±3	
	E_{ZD4}		800 counts, R_I = 82 kΩ	0	0	±3	
Polarity error	E_{PV1}	Voltage measurement mode	6400 counts, R_I = 680 kΩ	0	±4	±11	Count
	E_{PV2}		3200 counts, R_I = 330 kΩ	0	±2	±6	
	E_{PV3}		1600 counts, R_I = 180 kΩ	0	±1	±4	
	E_{PV4}		800 counts, R_I = 82 kΩ	0	±1	±4	
	E_{PD1}	Differential voltage measurement mode	6400 counts, R_I = 680 kΩ	0	±4	±13	Count
	E_{PD2}		3200 counts, R_I = 330 kΩ	0	±2	±7	
	E_{PD3}		1600 counts, R_I = 180 kΩ	0	±1	±5	
	E_{PD4}		800 counts, R_I = 82 kΩ	0	±1	±5	
Linearity error	E_{LV1}	Voltage measurement mode	6400 counts, R_I = 680 kΩ	0	±1	±8	Count
	E_{LV2}		3200 counts, R_I = 330 kΩ	0	±1	±4	
	E_{LV3}		1600 counts, R_I = 180 kΩ	0	±1	±3	
	E_{LV4}		800 counts, R_I = 82 kΩ	0	±1	±3	
	E_{LD1}	Differential voltage measurement mode	6400 counts, R_I = 680 kΩ	0	±2	±10	Count
	E_{LD2}		3200 counts, R_I = 330 kΩ	0	±1	±5	
	E_{LD3}		1600 counts, R_I = 180 kΩ	0	±1	±3	
	E_{LD4}		800 counts, R_I = 82 kΩ	0	±1	±3	
	E_{LR1}	Resistance measurement mode	6400 counts, R_I = 680 kΩ	0	±2	±10	Count
	E_{LR2}		3200 counts, R_I = 330 kΩ	0	±1	±5	
	E_{LR3}		1600 counts, R_I = 180 kΩ	0	±1	±3	
	E_{LR4}		800 counts, R_I = 82 kΩ	0	±1	±3	
Power current consumption	I_{AD}	Ta = 25°C Current that flows in external parts is not included.			300	900	µA

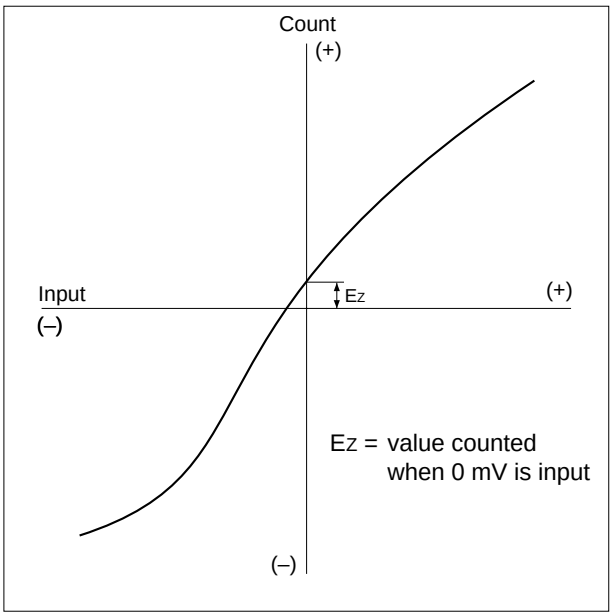
* In case of the voltage measurement mode or differential voltage measurement mode, the reference voltage V_{R2} is adjusted so that the measurement error (absolute error E) of the A/D converter becomes minimum when Ta=25°C, V_{DD}=V_{DDA}=3A, input voltage V_{IN}=+320mV. Error and deviation by the reference voltage V_{R2} are not included.

[Reference curves]

Absolute error E

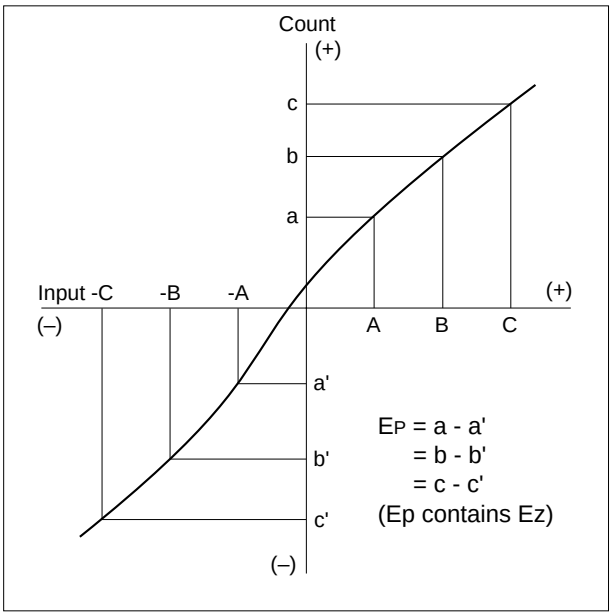


Zero point error EZ



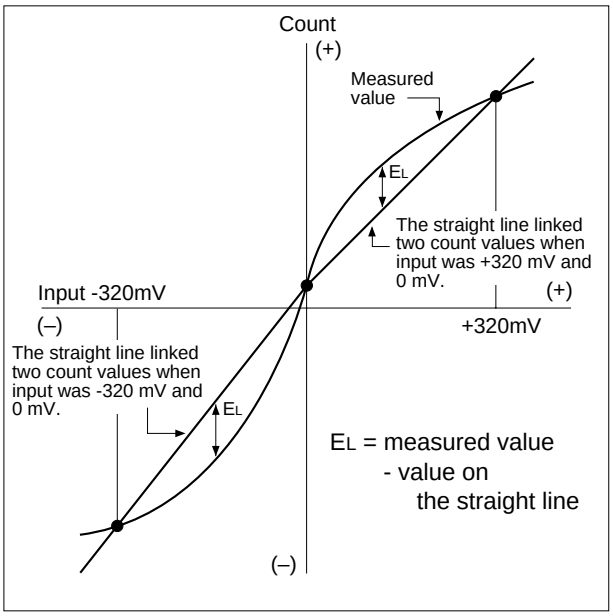
* There is no standard in the resistance measurement mode because 0 mV input has been inhibited.

Polarity error EP



* There is no standard in the resistance measurement mode because it is - (minus) input only.

Linearity error EL



* In the resistance measurement mode, the straight line linked two points at -6400 counts and 0 count.

Reference voltage generation circuit

(Unless otherwise specified: V_{DD}=V_{DDA}=3.0V, V_{SS}=V_{SSA}=0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{D1}/V_{C1}–V_{C3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Output voltage (1)	V_{R1O}	GND reference, Internal adjustment mode VRON = VRAON = "1"			-475		mV
Output voltage (2)	V_{R2O}	GND reference, Internal adjustment mode VRON = VRAON = "1"		-1.0	(-163.8mV)	1.0	%
Input voltage	V_{R1I}	GND reference, External adjustment mode VRON = VRAON = "0", (Input voltage when the measurement error becomes minimum)			-475		mV
Input current	$\lvert I_{VR1} \rvert$	External adjustment mode A/D related are all OFF. VRON = VRAON = "0" Current that flows in external parts is not included.		0		1.0	µA
Temperature characteristics	V_{R2}/Ta	Ta = 0 to 50°C (25°C standard) VRON = "1"	Internal adjustment mode VRAON = "1"	-300	150	600	ppm/°C
			External adjustment mode VRAON = "0"	-300	150	600	
Supply voltage characteristics	V_{R2}/V_{DDA}	V_{DDA} = 2.4 to 5.5 V VRON = "1"	Internal adjustment mode VRAON = "1"	-0.30	0	0.30	%FS
			External adjustment mode VRAON = "0"	-0.15	0	0.15	
Power current consumption	I_{AD1}	Internal adjustment mode VRON = VRAON = "1"			10.0	30.0	µA
	I_{AD2}	External adjustment mode VRON = "1", VRAON = "0"			2.0	5.0	

∗ Error, deviation and power current consumption by external parts are not included.

Middle electric potential (GND) generation circuit

(Unless otherwise specified: V_{DD}=V_{DDA}=3.0V, V_{SS}=V_{SSA}=0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{D1}/V_{C1}–V_{C3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage	GND_O	GNDON = "01, 10, 11"	V_{DDA}/2 -0.05	V_{DDA}/2	V_{DDA}/2 +0.05	V
Input voltage	GND_I	GNDON = "00"	V_{DDA}/2 -0.05	V_{DDA}/2	V_{DDA}/2 +0.05	V
Input current	$\lvert I_{GND} \rvert$	GNDON = "00", A/D related are all OFF. Current that flows in external parts is not included.	0		1.0	µA
High level output current	I_{OH}	GNDON = "01, 10, 11" V_{OH} = GND - 10 mV			-100	µA
Low level output current (1)	I_{OL1}	GNDON = "01" V_{OL1} = GND + 10 mV	10.0			µA
Low level output current (2)	I_{OL2}	GNDON = "10" V_{OL2} = GND + 10 mV	20.0			µA
Low level output current (3)	I_{OL3}	GNDON = "11" V_{OL3} = GND + 10 mV	40.0			µA
Temperature characteristics	GND/Ta	Ta = 0 to 50°C (25°C standard) GNDON = "01, 10, 11"	-30		30	ppm/°C
Supply voltage characteristics	GND/V_{DDA}	V_{DDA} = 2.4 to 5.5 V GNDON = "01, 10, 11"		0.5	10.0	mV/V
Power current consumption	I_{GND1}	GNDON = "01"		125	500	µA
	I_{GND2}	GNDON = "10"		250	1000	
	I_{GND3}	GNDON = "11"		500	2000	

∗ GNDON is mark of GNDON1 or GNDON0.

General-purpose operational amplifier

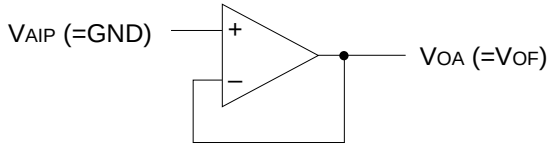
(Unless otherwise specified: V_{DD}=V_{DDA}=3.0V, V_{SS}=V_{SSA}=0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{D1}/V_{C1}–V_{C3} are internal voltage, C1–C6=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level output voltage	V_{OHA}	AMPONx = "1", V_{AIM} = GND V_{AIP} = GND + 10 mV, I_{OHA} = -10 µA		0.9•V_{DDA}		V_{DDA}	V
Low level output voltage	V_{OLA}	AMPONx = "1", V_{AIM} = GND V_{AIP} = GND - 10 mV, I_{OLA} = 10 µA		V_{SSA}		0.1•V_{DDA}	V
High level output current	I_{OHA}	AMPONx = "1", V_{AIP} = GND, AIP = AOUT V_{OHA} = GND - 0.1 V				-20	µA
Low level output current	I_{OLA}	AMPONx = "1", V_{AIP} = GND, AIM = AOUT V_{OLA} = GND + 0.1 V		100			µA
Offset voltage	V_{OF}	AMPONx = "1", V_{AIP} = GND, AIM = AOUT		-10		10	mV
Input voltage range	V_{IA}	AMPONx = "1", V_{AIM} = V_{IA} V_{AIP} = V_{IA} ± 15 mV Comparator operation		V_{SSA}+0.7		V_{DDA}-0.7	V
Slew rate	SR	AMPONx = "1"	Rising	20	200		mV/µS
		Load = 10 pF	Falling		-200	-20	
Response time	t_{AMP}	AMPONx = "1", V_{AIM} = GND V_{AIP} = GND ± 15 mV Comparator operation				3	mS
Power current consumption	I_{AMP1}	AMPON0 = "1", AMPON1 = "0"			100	300	µA
	I_{AMP2}	AMPON0 = "0", AMPON1 = "1"			100	300	

∗ AMPONx indicates AMPON0 or AMPON1.

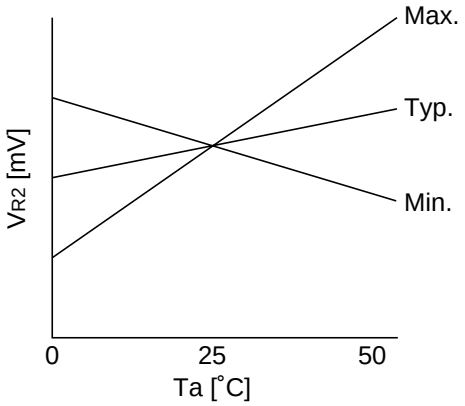
[Diagram for explanation of general-purpose operational amplifier]

I_{OHA}, I_{OLA} and V_{OF} measurement circuits

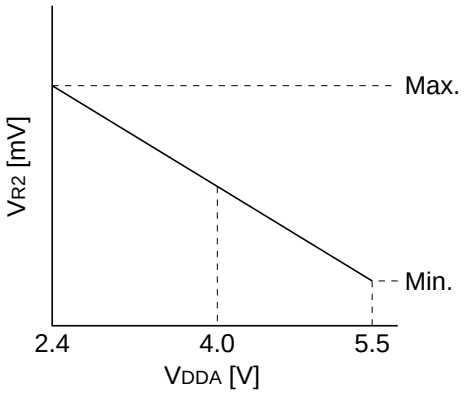


[Diagram for explanation of reference voltage generation circuit]

• Temperature characteristic V_{R2}/Ta



• Supply voltage characteristic V_{R2}/V_{DDA}



∗ Ta = 25°C as the standard

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤3sec (V_{DD})	2.2			V
Oscillation stop voltage	Vstp	tstp≤10sec (V_{DD})	2.2			V
Built-in capacitance (drain)	C_D	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	∂f/∂V	V_{DD}=2.2 to 5.5V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	Vhho	C_G=5pF (V_{DD})			7.0	V
Permitted leak resistance	Rleak	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

OSC3 CR oscillation circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, R_{CR}=39kΩ, Ta=25°C)

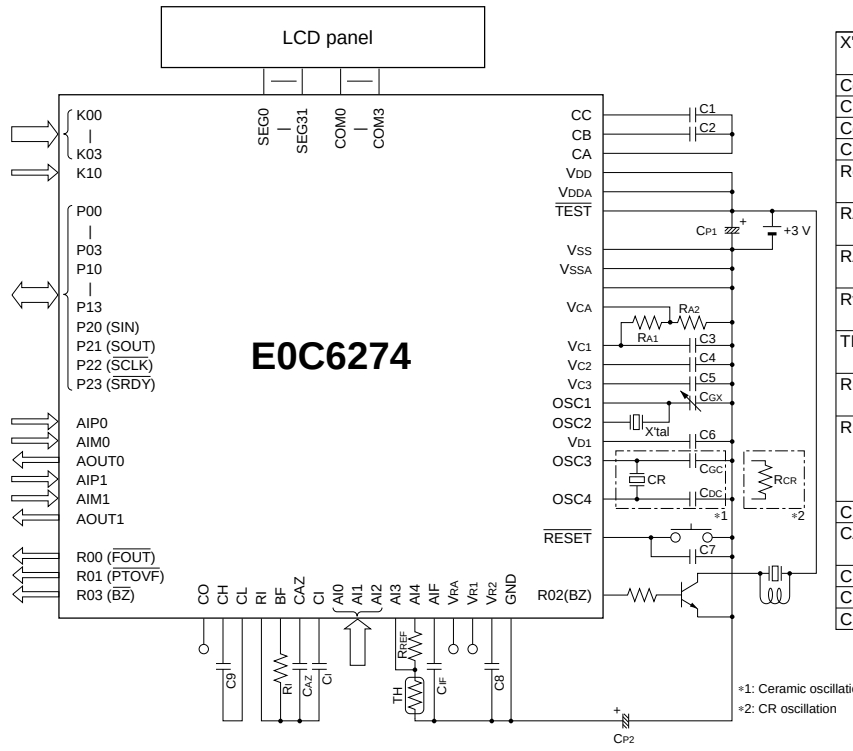
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	(900kHz)	30	%
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 5.5V			3	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

OSC3 ceramic oscillation circuit

(Unless otherwise specified: V_{DD}=3.0V, V_{SS}=0V, ceramic oscillation: 1MHz, C_{GC}=C_{DC}=100pF, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(V_{DD})	2.2			V
Oscillation start time	tsta	V_{DD}=2.2 to 5.5V			3	mS
Oscillation stop voltage	Vstp	(V_{DD})	2.2			V

■ BASIC EXTERNAL CONNECTION DIAGRAM

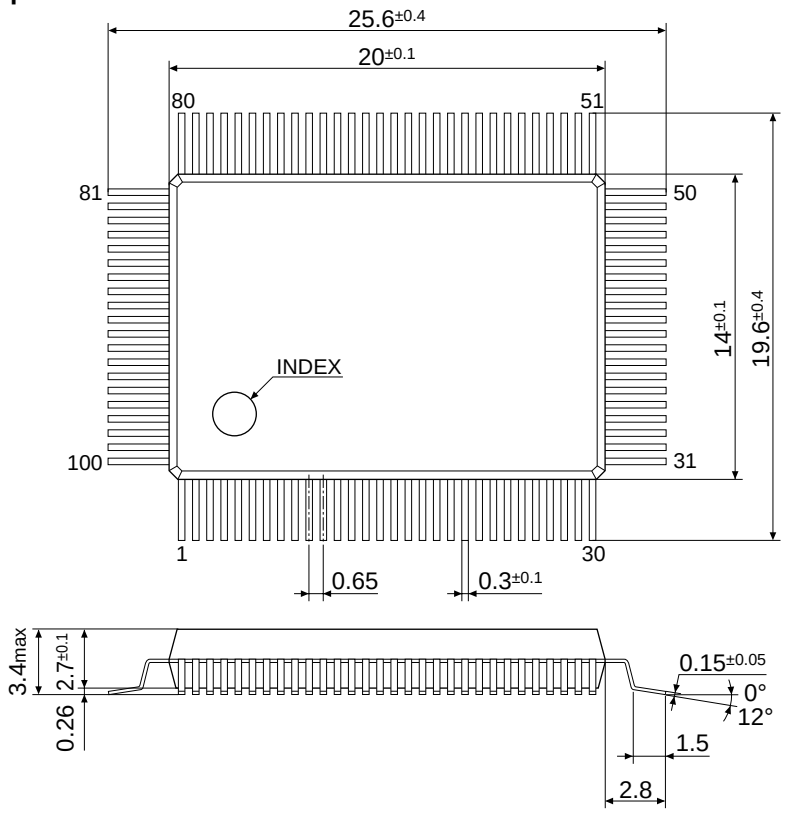


X'tal	Crystal oscillator	32.768kHz CI(Max.)=35kΩ
C_{GX}	Trimmer capacitor	5~25pF
CR	Ceramic oscillator	1MHz
C_{GC}	Gate capacitance	100pF
C_{DC}	Drain capacitance	100pF
R_{CR}	Resistance for CR oscillation	39kΩ (f_{OSC3}≈900kHz)
R_{A1}	Resistance for LCD drive voltage adjustment	1MΩ (V_{C1}≈1.5V)
R_{A2}	Resistance for LCD drive voltage adjustment	2MΩ (V_{C1}≈1.5V)
R_{VR}	Resistance for A/D reference voltage adjustment	3MΩ
TH	Thermistor	10kΩ (5kΩ~20kΩ)
R_{REF}	Reference resistance for resistance measurement	10kΩ
R_I	Integral resistance (resolution)	680kΩ(6400) 330kΩ(3200) 180kΩ(1600) 82kΩ(800)
C_I	Integral capacitor	0.1µF
C_{AZ}	Capacitor for auto zero adjustment	0.1µF
C_{IF}	Analog input filter capacitor	0.01µF
C1~C9		0.1µF
C_{P1}, C_{P2}		3.3µF

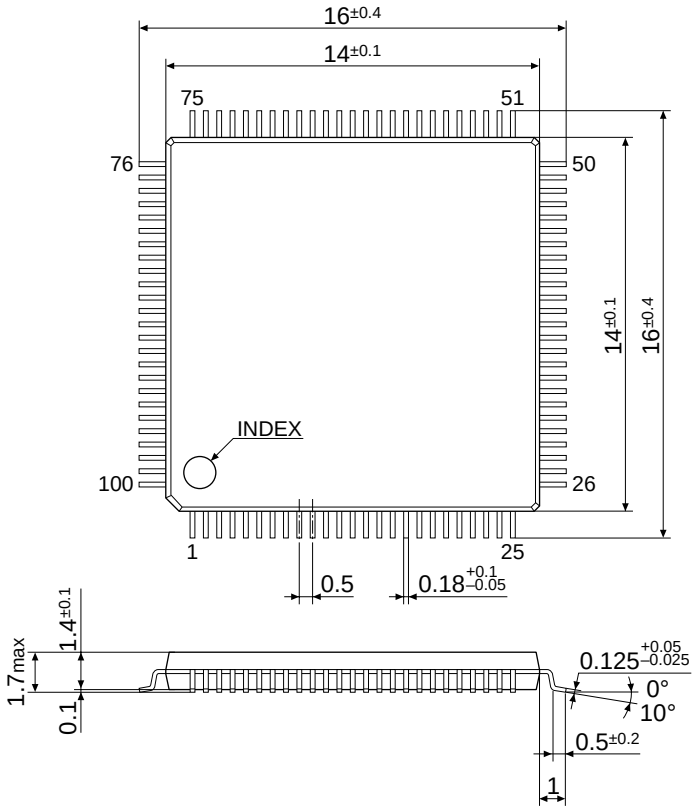
Note: The above table is simply an example, and is not guaranteed to work.

■ PACKAGE DIMENSIONS

Plastic QFP5-100pin



Plastic QFP15-100pin



Unit: mm

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