10-Gigabit Ethernet MAC with XGMII or XAUI v2.1

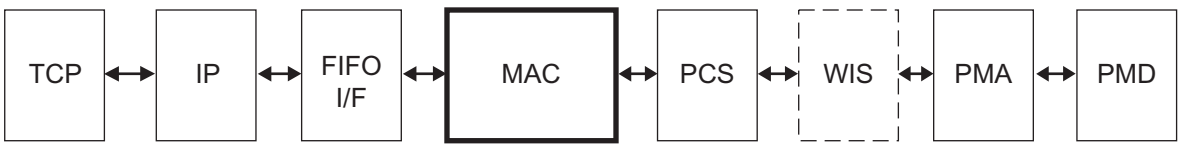
DS201 (v2.1) June 24, 2002

Product Specification

Features

- Single-speed full-duplex 10-gigabits-per-second Ethernet Media Access Controller
- Designed to Draft D4.1 of IEEE P802.3ae specification
- Choice of XGMII or XAUI interface to PHY layer
- Uses Virtex™-II DDR I/O primitives for the optional XGMII interface
- Uses Virtex-II Pro™ Multi Gigabit Transceivers for the optional XAUI interface
- Cut-through operation with minimum buffering for maximum flexibility in 64-bit client bus interfacing
- Configured and monitored through an independent microprocessor-neutral interface
- Uses Virtex-II/Virtex-II Pro Digital Clock Management to implement XGMII and XAUI interface timing
- Powerful statistics gathering to internal counters. Statistics vectors are also output to the user.
- Configurable flow control through MAC Control pause frames; symmetrically or asymmetrically enabled
- New-style Clause 45 MDIO interface to managed objects in PHY layers
- Supports LAN/WAN (OC-192c data rate) functionality through open loop rate control
- Configurable support of VLAN frames to specification IEEE 802.3-2000
- Configurable support of “jumbo frames” of any length
- Configurable interframe gap length adjustment
- Remote Fault/Local Fault signalling at the Reconciliation Sublayer
- Available under terms of the SignOnce IP License

LogiCORE™ Facts	
Core Specifics	
Supported Families	Virtex-II, Virtex-II Pro
Speed Grades	-5 speed grade on Virtex-II (XGMII version only) -7 speed grade on Virtex-II Pro
Performance	156.25 MHz internal clock; 156.25MHz DDR on XGMII interface; 3.125Gbps per lane on XAUI interface
Size	3000-4400 slices
Global Clock Buffers	3
Special Features	Digital Clock Management integrated into core
Provided with Core	
Documentation	Product Specification
Design File Formats	EDIF netlist
Constraints File	.ucf
Design Tools Requirements	
Xilinx Core Tools v4.2i SP2	
Support	
Support provided by Xilinx	



XIP2092

Figure 1: **Typical 10-Gigabit Ethernet Architecture**

Overview

The 10-gigabit Ethernet MAC is part of the 10-gigabit Ethernet architecture displayed in Figure 1. The part of this architecture from the MAC to the right is defined in Draft D4.1 specification of the *IEEE P802.3ae Task Force*, currently under development and due to be ratified in May 2002.

A block diagram of the MAC core can be seen in Figure 2. This shows the major functional blocks of the MAC, which are:

- the client interface
- the transmit engine
- the flow control block
- the receive engine
- the Reconciliation Sublayer (RS)
- the configuration block
- the statistics block
- the MII Management interface (MIIM)
- the optional XGMII interface
- the optional XAUI interface

The client interface has fully independent 64-bit interfaces for both transmit and receive to support full duplex operation; control lines are associated with each port to delineate data lanes within the 64 bits.

The configuration block and the statistics block are both accessed through the management interface, a 32-bit processor-neutral data pathway that is independent of the Ethernet data pathway. The MIIM port is also accessed through this interface.

The RS either converts the internal data representation of the MAC core to the 32-bit DDR data that the XGMII specification requires, or passes it to the XAUI block. It also contains logic to handle local fault and remote fault signalling across the link.

The optional XAUI interface is designed to clause 47 of the IEEE P802.3ae D4.1 draft. It uses the Multi Gigabit Transceivers (MGTs) of the Virtex-II Pro family. It converts the MAC data into 4 lanes of 3.125Gbps data for transmission over current mode differential lines, and also receives four lanes of data at the same rate and passes it to the MAC.

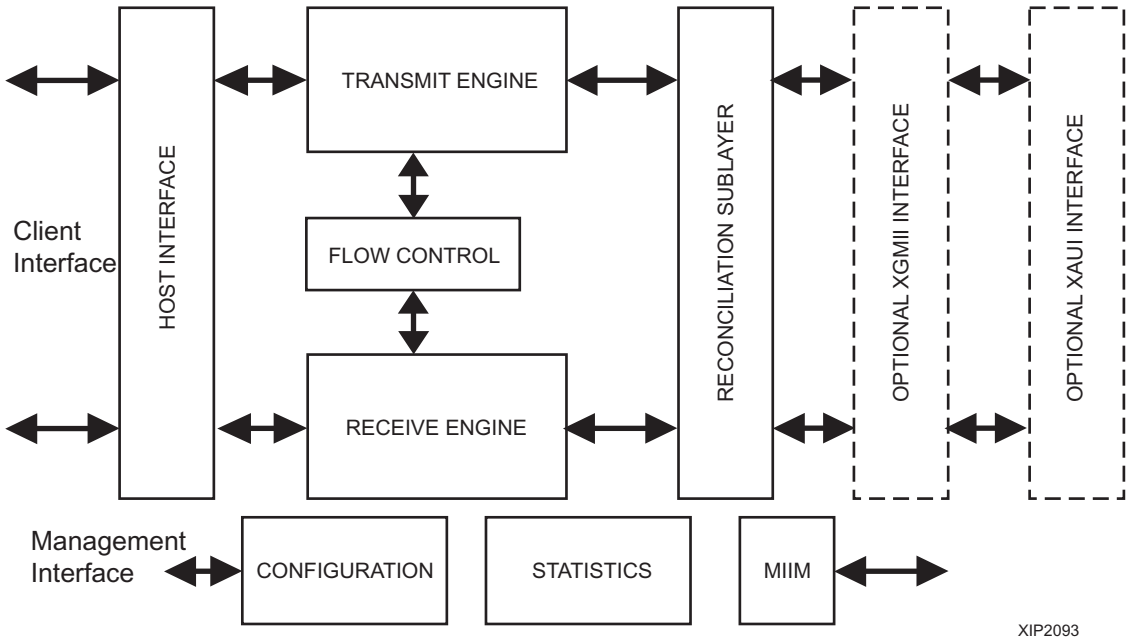


Figure 2: **Functional Block Diagram of the 10-Gigabit Ethernet MAC**

Interface Description

Client Interface Signals

Figure 3 shows the pinout for a MAC core with the optional XGMII interface.

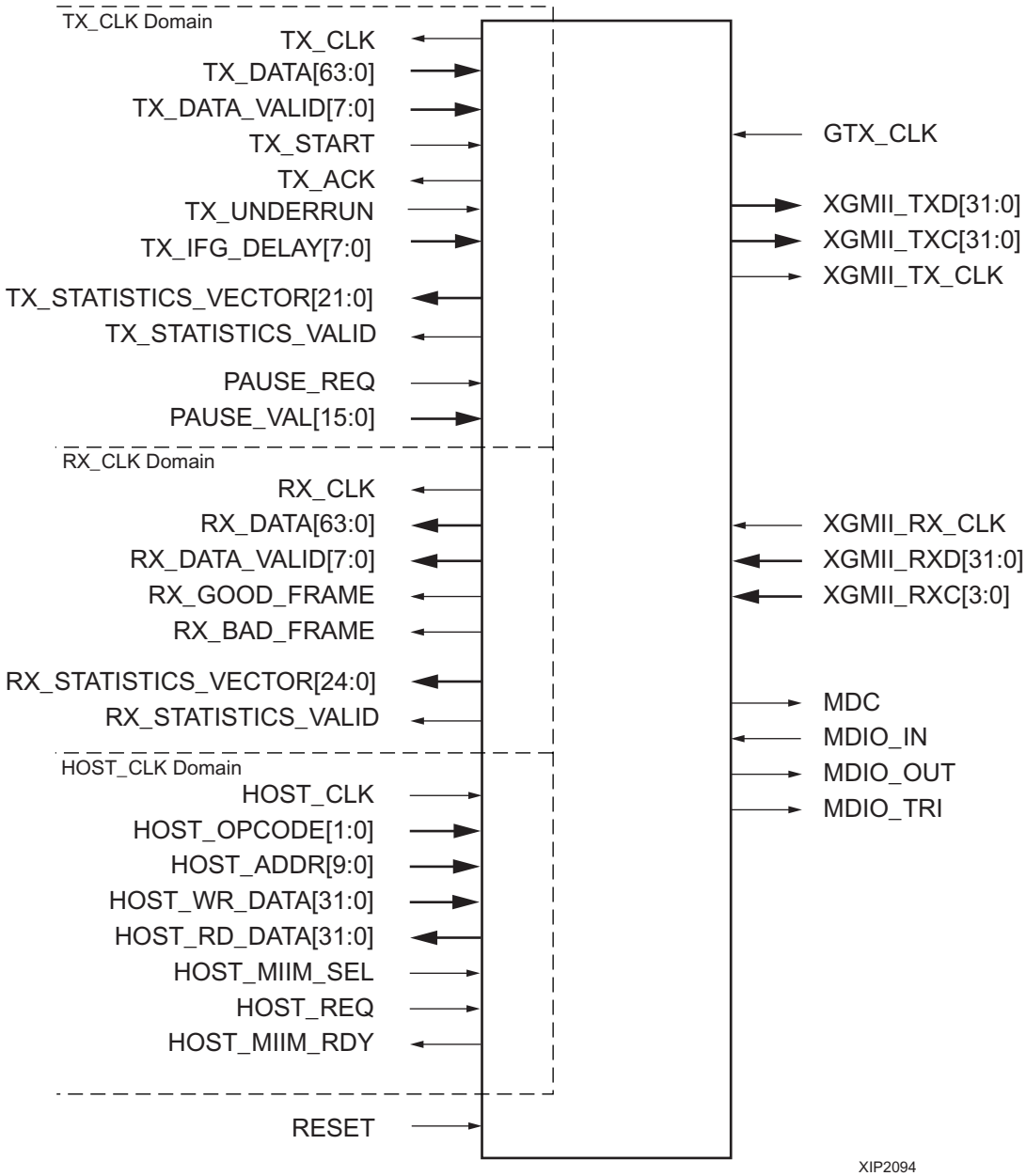


Figure 3: **Core Pinout with XGMII Interface**

Figure 4 shows the pinout of a MAC core with the optional XAUI interface.

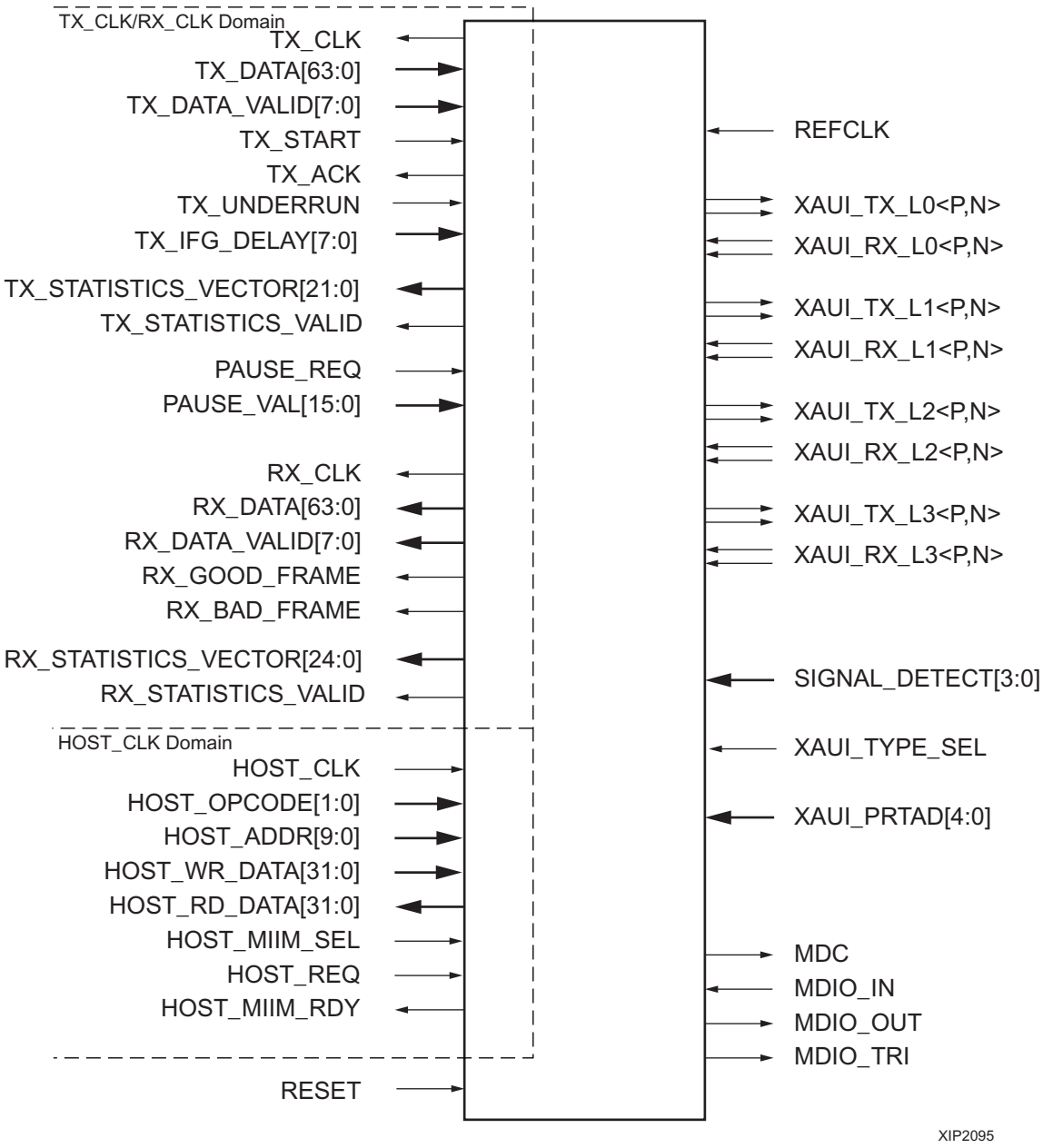


Figure 4: **Core pinout with XAUI interface**

Table 1 describes the client-side transmitter interface signals of the MAC core. These signals are used to transmit data from the client to the MAC core.

Table 1: **Transmit Client Interface Signal Pins**

Signal	Direction	Description
TX_CLK	Output	Clock for transmit client interface. 156.25 MHz nominal.
TX_DATA[63:0]	Input	Frame data to be transmitted is supplied on this port.
TX_DATA_VALID[7:0]	Input	Control signals for TX_DATA port. Each asserted signal on TX_DATA_VALID signifies which bytes of TX_DATA are valid; *i.e.,* if TX_DATA_VALID[0] is 1, the signal TX_DATA[7:0] is valid.

Table 1: **Transmit Client Interface Signal Pins *(Continued)***

Signal	Direction	Description
TX_START	Input	Handshaking signal. Asserted by the client to make data available for transmission. See the timing diagrams in section "Transmitter" on page 8.
TX_ACK	Output	Asserted when the current data on TX_DATA has been accepted. See timing diagrams in section "Transmitter" on page 8.
TX_UNDERRUN	Input	Asserted by client to force MAC to corrupt the current frame.
TX_IFG_DELAY[7:0]	Input	Enables the user to select a minimum interframe gap size. See timing diagrams in section "Transmitter" on page 8.
TX_STATISTICS_VECTOR[21:0]	Output	This gives information on the last frame transmitted. The contents of the vector are described in section "XGMII Interface" on page 29.
TX_STATISTICS_VALID	Output	This is asserted when the data on the TX_STATISTICS_VECTOR is valid.

Notes:
1. All the above signals are synchronous to TX_CLK and Active High.

Table 2 describes the signals used by the host to request a flow control action from the transmit engine. Flow control frames received by the MAC across the XGMII or XAUI are automatically handled (if the MAC is configured to do so).

Table 2: **Flow Control Interface Signal Pinout**

Signal	Direction	Description
PAUSE_REQ	Input	Pause request; sends a pause frame down the link.
PAUSE_VAL[15:0]	Input	Pause value; this value is inserted into the parameter field of the transmitted pause frame.

Notes:
1. These signals are synchronous to TX_CLK and are Active High.

Table 3 describes the client-side receive signals. These signals are used by the MAC core to transfer data to the client.

Table 3: **Receive Client Interface Signal Pins**

Signal	Direction	Description
RX_CLK	Output	Clock for receiving client interface. 156.25 MHz nominal.
RX_DATA[63:0]	Output	Frame data received is supplied on this port.
RX_DATA_VALID[7:0]	Output	Control signals for the RX_DATA port. Each asserted signal on RX_DATA_VALID signifies which bytes of RX_DATA are valid. *E.g.,* if RX_DATA_VALID[0] is 1, the signal RX_DATA[7:0] is valid.
RX_GOOD_FRAME	Output	Asserted at end of reception of compliant frame. See "Receiver" on page 16.
RX_BAD_FRAME	Output	Asserted at end of noncompliant frame. See "Receiver" on page 16.
RX_STATISTICS_VECTOR[24:0]	Output	Information on the last frame received. The contents of the vector are described in section "XGMII Interface" on page 29.
RX_STATISTICS_VALID	Output	This is driven high when the RX_STATISTICS_VECTOR is valid.

Notes:
1. All signals above are synchronous to RX_CLK and Active High.

Table 4 describes the signals used by the host system to access the management features of the MAC core, including configuration, status, statistics and MIIM access.

Table 4: **Management Interface Signal Pinout**

Signal	Direction	Description
HOST_CLK	Input	Clock for management interface. See "Management Interface" on page 22 for the frequency range of this signal.
HOST_OPCODE[1:0]	Input	Defines operation to be performed over management interface.
HOST_ADDR[9:0]	Input	Address of register to be accessed.
HOST_WR_DATA[31:0]	Input	Data to write to register.
HOST_RD_DATA[31:0]	Output	Data read from register.
HOST_MIIM_SEL	Input	When asserted, the MIIM interface is accessed. When disasserted, the MAC internal registers are accessed.
HOST_REQ	Input	Used to signal a transaction on the MIIM interface and to read from the statistic registers. See "Management Interface" on page 22.
HOST_MIIM_RDY	Output	When high, the MIIM interface has completed any pending transaction and is ready for a new transaction.
RESET	Input	Asynchronous reset for entire core. This must be asserted for a minimum of 500 ns for a valid reset to occur. The clocks must be running for the core to come out of the reset state.

Notes:
1. All signals above except RESET are synchronous to HOST_CLK and are Active High.

Table 5 describes the XGMII signals of the MAC core. These signals are optional. These are typically attached to an off-chip PHY module.

Table 5: **XGMII Interface Signal Pinout**

Signal	Direction	Description
GTX_CLK	Input	Clock signal at 156.25MHz. Other transmit clocks are derived from this using DCM. Tolerance must be within that specified in the IEEE P802.3 Ethernet specification.
XGMII_TX_CLK	Output	Clock to PHY; source centred with respect to transmit data.
XGMII_TXD[31:0]	Output	Transmit data to PHY; double data rate (DDR) signalling.
XGMII_TXC[3:0]	Output	Control lines to PHY.
XGMII_RX_CLK	Input	Recovered clock from received data stream by PHY.
XGMII_RXD[31:0]	Input	Received data from PHY; DDR signalling.
XGMII_RXC[3:0]	Input	Control lines from PHY.

Table 6 describes the XAUI signals of the MAC core. These signals are optional and are typically attached to a backplane or PHY module.

Table 6: **XAUI Interface Signal Pinout**

Signal	Direction	Description
REFCLK	Input	Clock signal at 156.25 MHz. All other core clocks are derived from this using a DCM. Must conform to MGT jitter and stability specifications. See Virtex-II Pro databook.
XAUI_TX_L0_<P,N>	Output	Transmit Differential Pair, XAUI Lane 0
XAUI_TX_L1_<P,N>	Output	Transmit Differential Pair, XAUI Lane 1
XAUI_TX_L2_<P,N>	Output	Transmit Differential Pair, XAUI Lane 2
XAUI_TX_L3_<P,N>	Output	Transmit Differential Pair, XAUI Lane 3
XAUI_RX_L0_<P,N>	Input	Receive Differential Pair, XAUI Lane 0
XAUI_RX_L1_<P,N>	Input	Receive Differential Pair, XAUI Lane 1
XAUI_RX_L2_<P,N>	Input	Receive Differential Pair, XAUI Lane 2
XAUI_RX_L3_<P,N>	Input	Receive Differential Pair, XAUI Lane 3
SIGNAL_DETECT[3:0]	Input	Signals from an 10GBASE-LX4 optical module, when the XAUI block is used as a 10GBASE-X PCS. When the XAUI block is used as an XGXS, these signals have no effect.
XAUI_TYPE_SEL	Input	Selects which type of XAUI block is implemented. When XAUI_TYPE_SEL = 0, the block behaves as a 10GBASE-X PCS. When XAUI_TYPE_SEL = 1, the block behaves as a DTE XGXS.
XAUI_PRTAD[4:0]	Input	Sets the port address at which the XAUI block should appear on the MIIM bus.

Table 7 describes the MIIM interface signals of the MAC core. These signals are typically connected to the MIIM port of an off-chip PHY.

Table 7: **MIIM Interface Signal Pinout**

Signal	Direction	Description
MDC	Output	Management Clock; derived from HOST_CLK on basis of supplied configuration data. See "Management Interface" on page 22.
MDIO_IN	Input	Serial MDIO data signal from PHY.
MDIO_OUT	Output	Serial MDIO data signal to PHY
MDIO_TRI	Output	Tristate control for MDIO signals; “0” signals that the value on MDIO_OUT should be asserted onto the MDIO bus.

Functional Description

Client Interface

The client interface is designed for maximum flexibility in matching to a client switching fabric or network processor interface.

The data pathway is 64 bits wide in both the transmit and receive directions, with each pathway synchronous to the TX_CLK and RX_CLK respectively for completely independent full duplex operation. There are 8 control lines associated with each interface to signal which byte lanes are active in each clocked transfer (Table 8). For each of TX_DATA and RX_DATA, the port is logically divided into lane 0 to lane 7, with the corresponding bit of the control word signifying valid data on the TX_DATA, RX_DATA port.

Table 8: **TX_DATA, RX_DATA Lanes**

Lane	TX_DATA, RX_DATA bits
0	7:0
1	15:8
2	23:16
3	31:24
4	39:32
5	47:40
6	55:48
7	63:56

Transmitter

Normal frame transmission

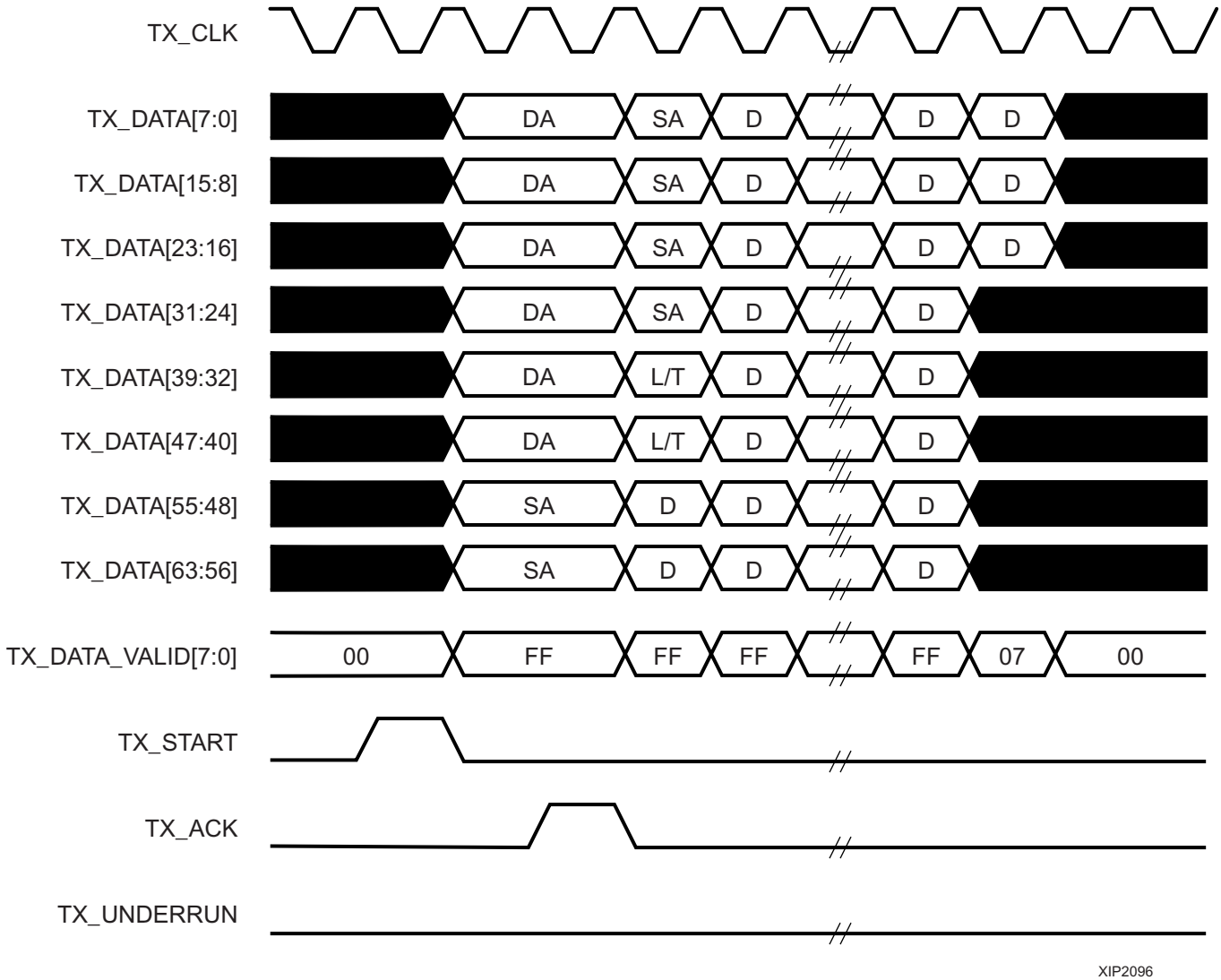


Figure 5: **Normal Frame Transmission across Client Interface**

The timing of a normal outbound frame transfer is shown in Figure 5. When the client wants to transmit a frame, it asserts the TX_START signal, and on the next clock places the first column of data and control onto the TX_DATA and TX_DATA_VALID ports.

When the MAC core has read this first column of data, it will assert the TX_ACK signal; on the next and subsequent clock edges, the client must provide the remainder of the data for the frame.

The end of frame is signalled to the MAC core by having TX_DATA_VALID not equal to hexadecimal “FF”; partially full columns of data are not permitted within a frame. As an example, in Figure 5, the value of TX_DATA_VALID of hexadecimal “07” signals to the MAC core that only the lower three columns of data are valid on the transfer, and additionally that the end of frame has been reached.

Frame parameters (destination address, source address, length/type and optionally FCS) must be supplied on the data bus according to the timing diagram. The definitions of the abbreviations are described in Table 9.

Table 9: **Abbreviations Used in Timing Diagrams**

Abbreviation	Definition
DA	Destination Address
SA	Source Address
L/T	Length/Type Field
FCS	Frame Check Sequence

In-band parameter encoding

For maximum flexibility in switching applications, the Ethernet frame parameters are encoded within the same data stream that the frame payload is transferred upon, rather than on separate ports.

The destination address must be supplied with the first byte in lane 0 and so on. Similarly, the first byte of the Source Address must be supplied in lane 6 of the first transfer.

The length/type field is similarly encoded, with the first byte placed into lane 4.

Client-supplied FCS passing

If the MAC core is configured to have the FCS field passed by the client (see "Configuration Registers" on page 22), the transmission timing is as shown in Figure 6. In this case, it is the responsibility of the client to ensure that the frame meets the Ethernet minimum frame length requirements; the MAC core will not perform any padding of the payload.

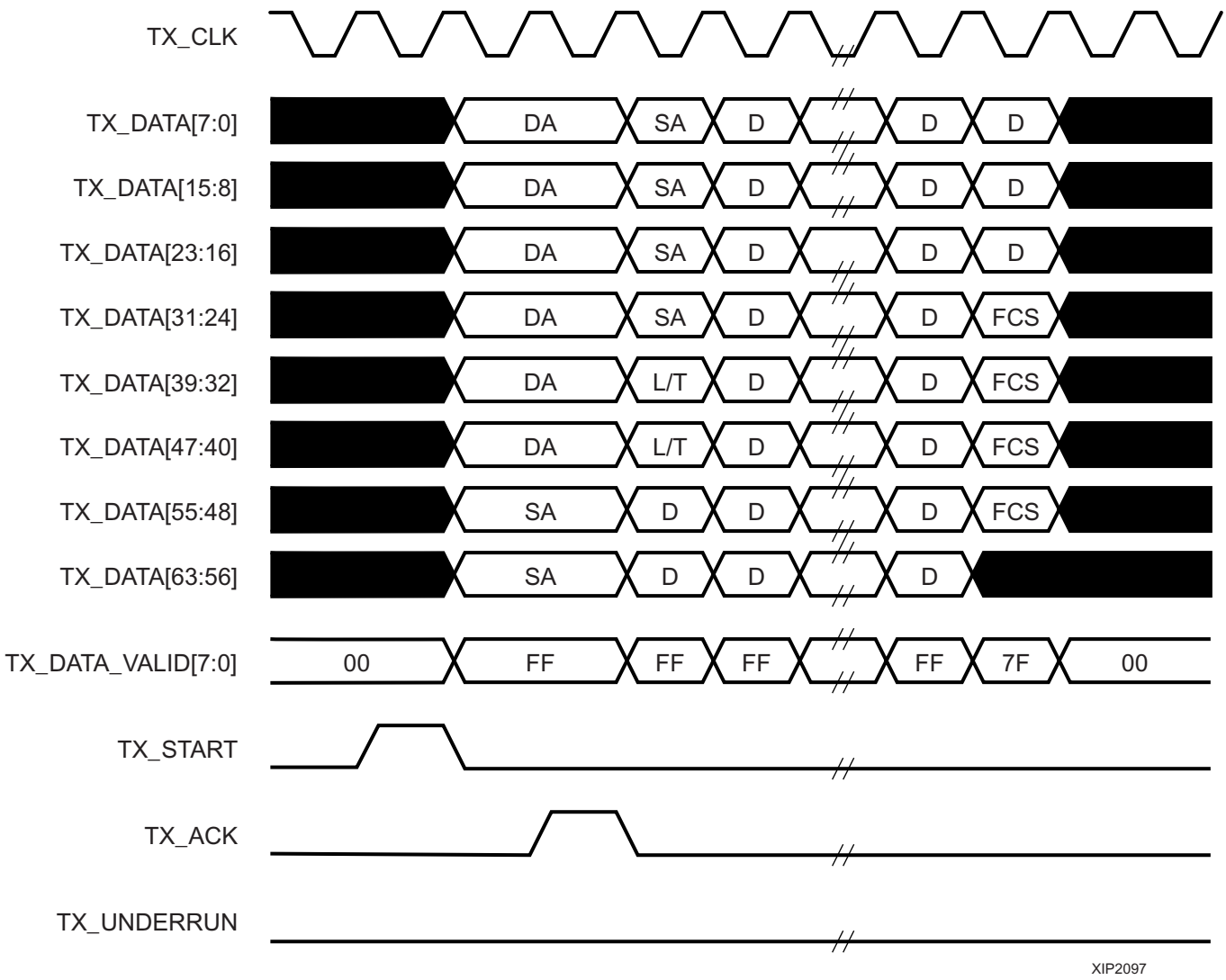


Figure 6: **Frame Transmission with Client-supplied FCS**

Padding

When fewer than 46 bytes of data are supplied by the client to the MAC core, the transmitter module will add padding up to the minimum frame length, unless the MAC core is configured for client-passed FCS. In the latter case, the client must also supply the padding in order to maintain the minimum frame length.

Client Underrun

The timing of an aborted transfer can be seen in Figure 7. This may happen, for instance, if a FIFO in the bus interface empties before a frame is completed. When the client asserts TX_UNDERRUN during a frame transmission, the MAC core will insert error codes into the XGMII data stream in order to corrupt the current frame, then will fall back to idle transmission. It is the responsibility of the client to requeue the aborted frame for transmission.

When an underrun occurs, TX_START may be asserted on the clock cycle after the TX_UNDERRUN assertion to start a new transmission.

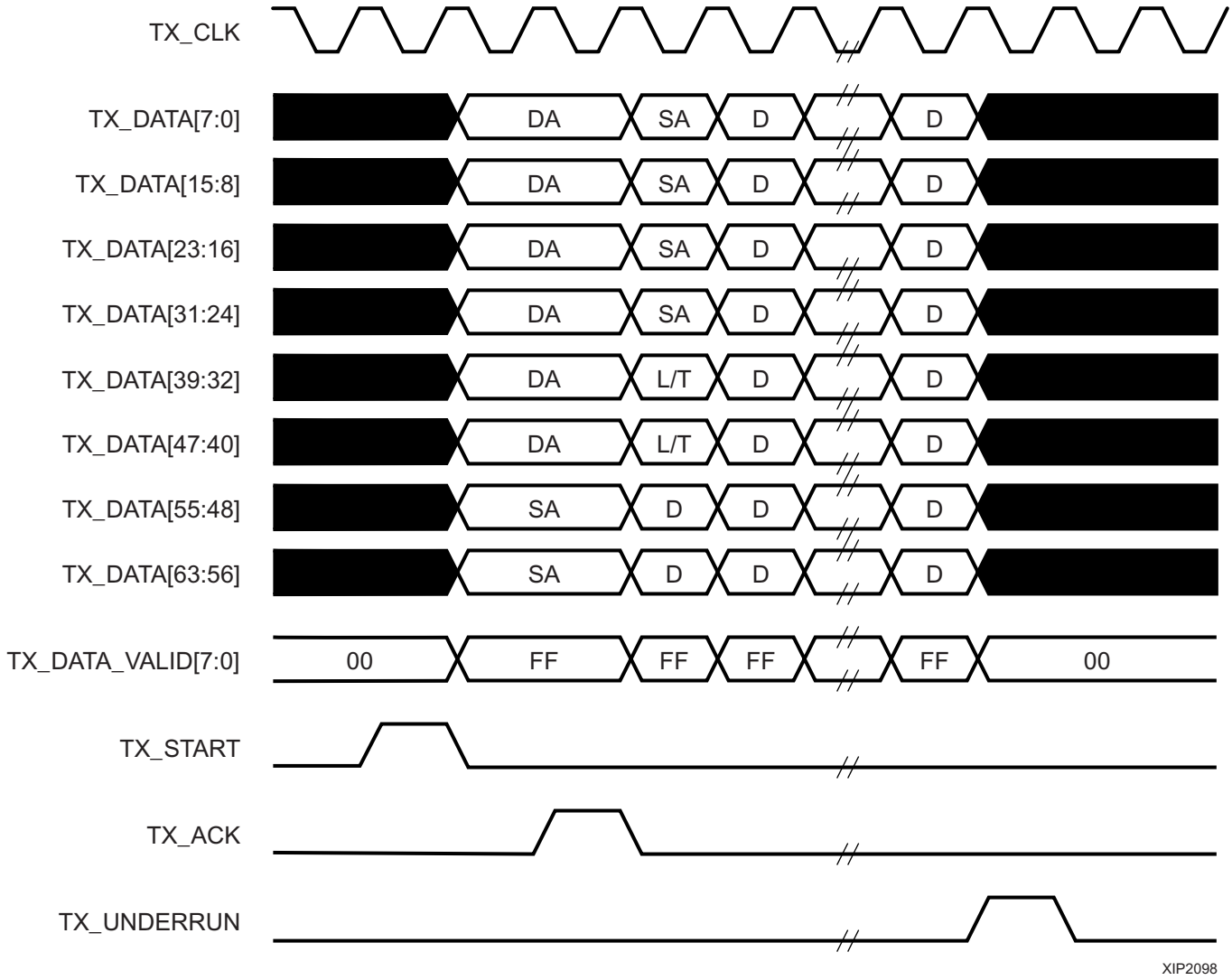


Figure 7: **Frame Transmission with Underrun**

Back-to-back transfers

Two situations can occur during back-to-back transfers; in one, the MAC core is ready to accept data; in the other, the MAC must defer to comply with inter-packet gap requirements, a user request to extend the interframe gap or flow control requests.

Figure 8 shows the case where the MAC is immediately ready to accept the next frame of data. In the column after the last data is transferred for the first frame, the client asserts TX_START to signal that another frame is ready for transmission. The MAC core then asserts TX_ACK to allow the client to begin the burst of frame parameters and data that make up the frame.

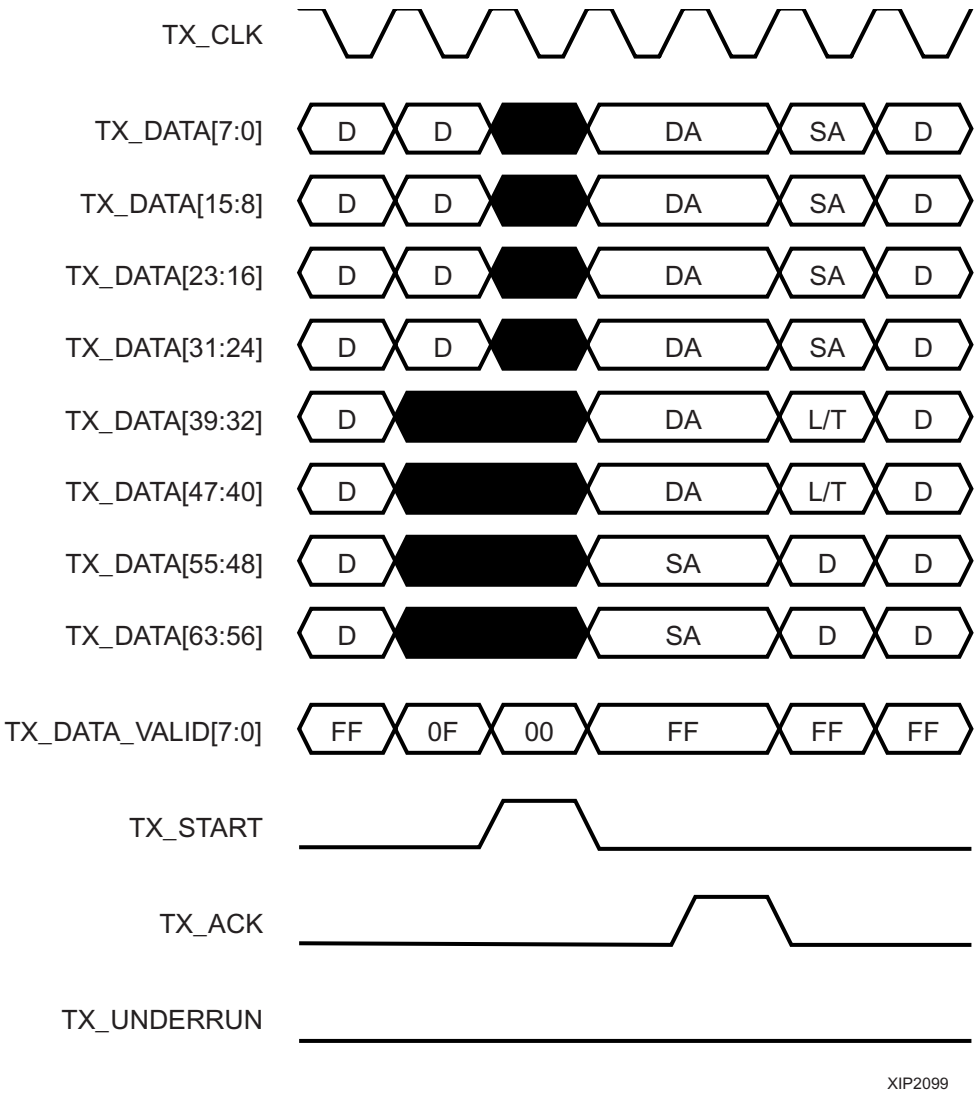


Figure 8: **Back to Back Frame Transmission with no Back Pressure**

Figure 9 shows a case where the MAC is exerting back pressure on the client to delay the start of transmission. In this case, the client has asserted TX_START to signal that another frame is ready for transmission, but the MAC core has delayed the assertion of TX_ACK to allow the data burst to begin. Once this burst has begun, it continues in the same manner as in the cases above. In both cases, as in the case for normal frame transmission, the client must provide a whole frame of data in one burst; there is no mechanism to stop and start transfer within a single frame.

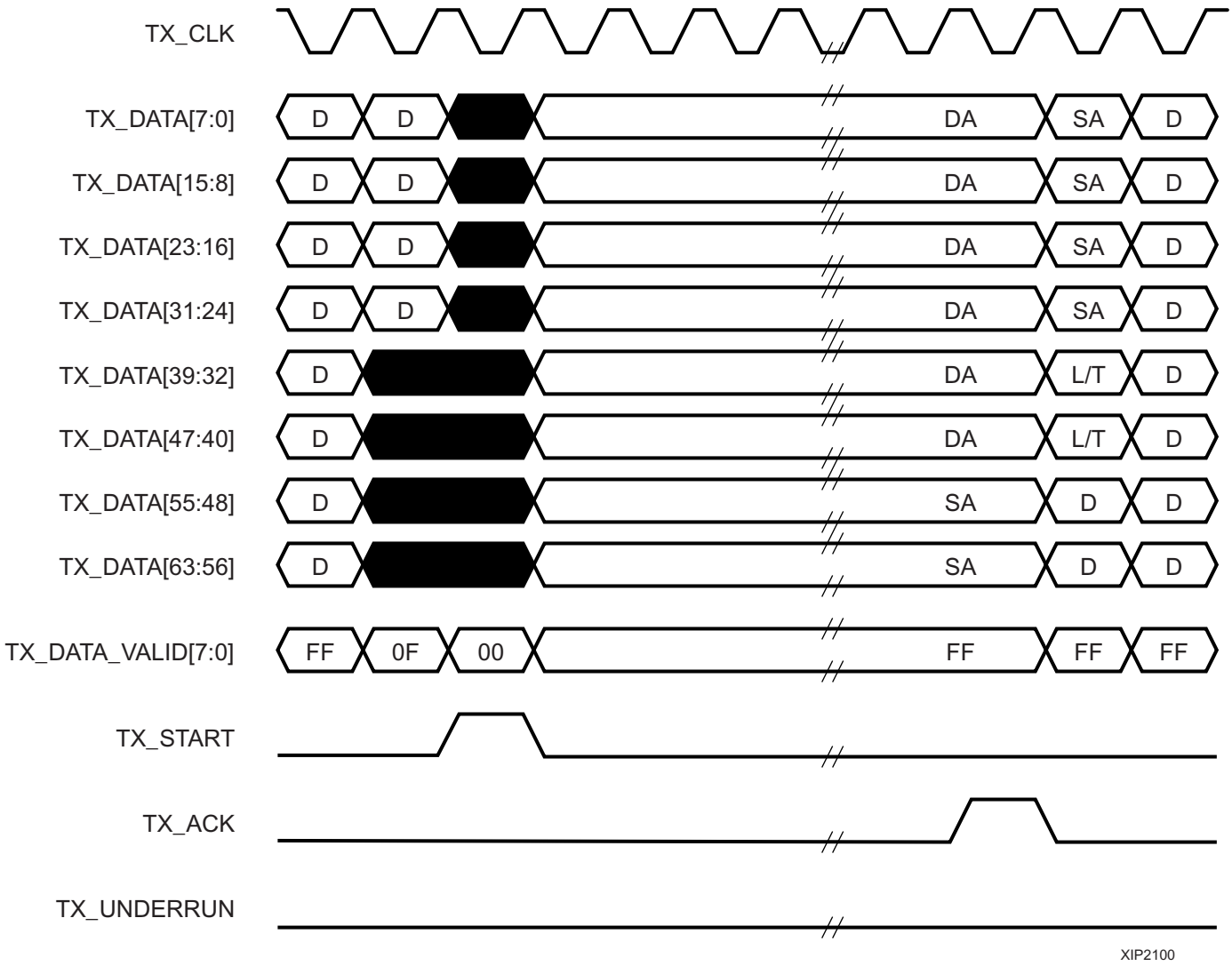


Figure 9: **Back-to-Back Frame Transmission with Back Pressure**

Interframe gap adjustment

The user can elect to vary the length of the interframe gap. If this function is selected (via a configuration bit, see "Configuration Registers" on page 22), the MAC will exert back pressure to delay the transmission of the next frame until the requested number of XGMII columns has elapsed. The number of XGMII columns is controlled by the value on the IFG_DELAY port. The minimum interframe gap of 3 XGMII columns is always maintained. Figure 10 shows the MAC operating in this mode.

If the core has a XAUI interface rather than a XAUI one, the interframe gap will vary as if an XGMII interface existed.

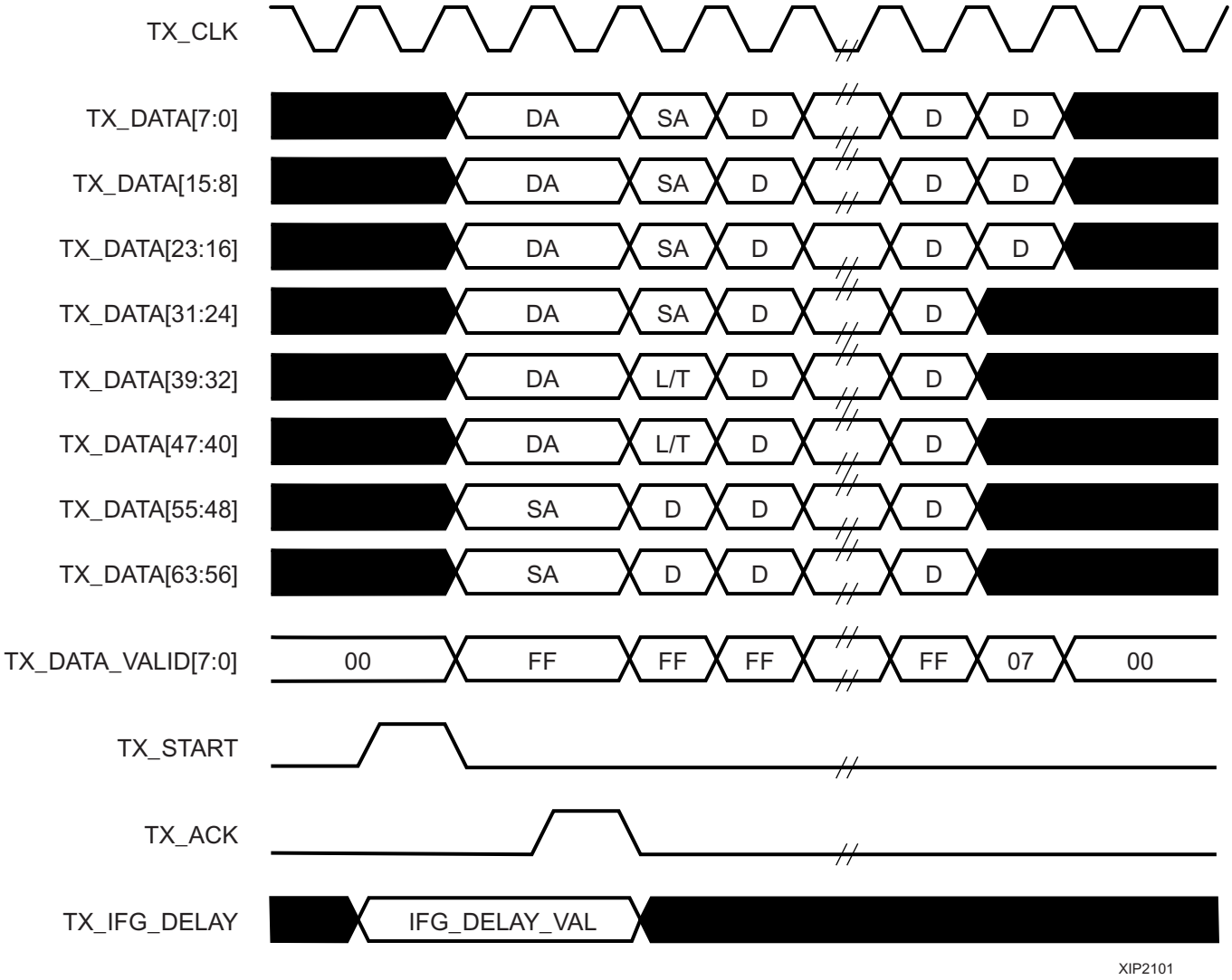


Figure 10: **Interframe Gap Adjustment**

VLAN Tagged Frames

Transmission of a VLAN tagged frame (if enabled) is shown in Figure 11. Note that the handshaking signals across the interface do not change; however, the VLAN type tag 81-00 must be supplied by the client to signify that the frame is VLAN tagged. The client also supplies the two bytes of Tag Control Information, V1 and V2, at the appropriate times in the data stream. More information on the contents of these two bytes can be found in IEEE 802.3-2000.

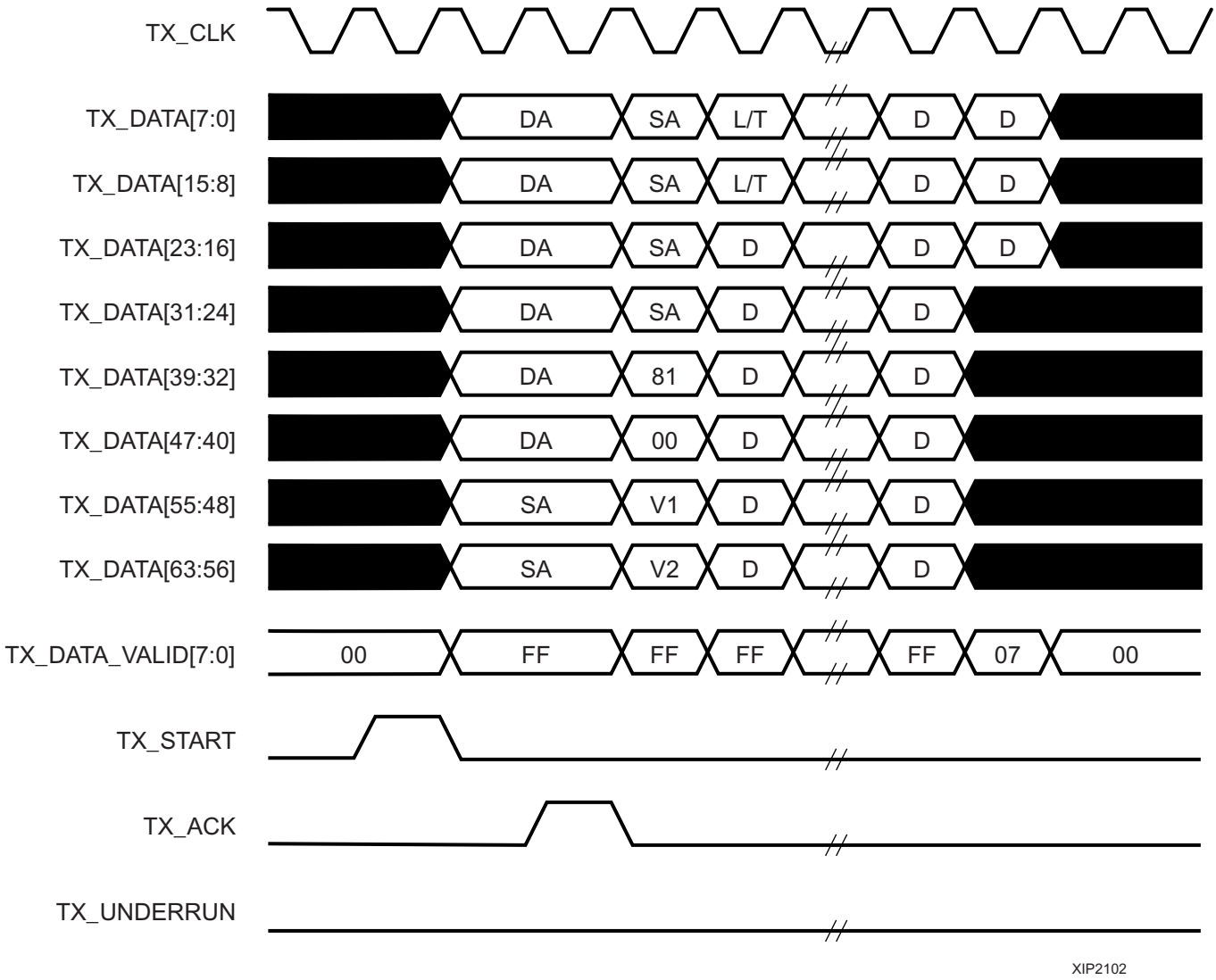


Figure 11: **Transmission of a VLAN Tagged Frame.**

Transmitter Statistics Vector

The statistics for the frame transmitted are contained within the TX_STATISTICS_VECTOR. The vector is synchronous to the transmitter clock, TX_CLK and is driven following frame transmission. The bit field definition for the Vector is defined in Table 10.

All bit fields, with the exception of BYTE_VALID, are valid only when the TX_STATISTICS_VALID is asserted. This is illustrated in Figure 12. BYTE_VALID is significant on every TX_CLK cycle.

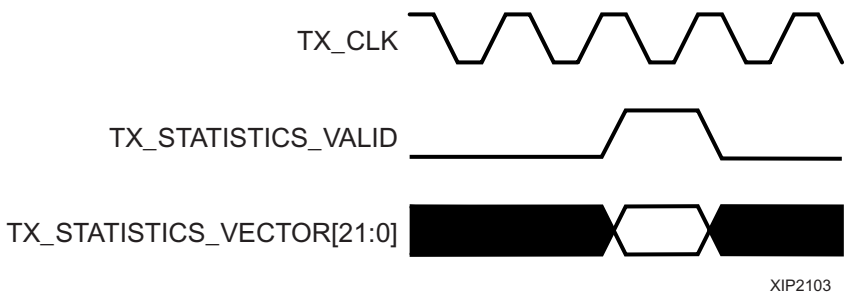


Figure 12: **Transmitter statistics output timing.**

Table 10: **TX_STATISTICS_VECTOR Description**

TX Stats Vector Bit	Name	Description
21	Pause Frame Transmitted	The previous frame was a pause frame that was initiated by the MAC in response to a pause request from the client.
20 to 17	Number of Bytes	The number of bytes transmitted on the last clock cycle. This can be between 0 and 8. This is valid on every clock cycle, it is not validated by TX_STATISTICS_VALID.
16	VLAN Frame	High along with the valid signal when the previous frame was a VLAN frame.
15 to 5	Length Count	The length of the previously transmitted frame. This does not take into account the preamble or start bytes. The count will stick at 2047 for any Jumbo frames larger than this value.
4	Control Frame	Indicates that the previous frame had the special control frame character in the length/type field.
3	Underrun Frame	High if the previous frame contained an underrun error.
2	Multicast Frame	High if the destination address in the previous frame contained a multicast address.
1	Broadcast Frame	High if the destination address in the previous frame contained a broadcast address.
0	Successful Frame	High if the previous frame was transmitted successfully.

Receiver

Normal Frame Reception

The timing of a normal inbound frame transfer is represented in Figure 13. The client must be prepared to accept data at any time; there is no buffering within the MAC to allow for latency in the receive client. Once frame reception begins, data is transferred on consecutive clock cycles to the receive client until the frame is complete. The MAC asserts the RX_GOOD_FRAME signal to signal successful frame reception to the client.

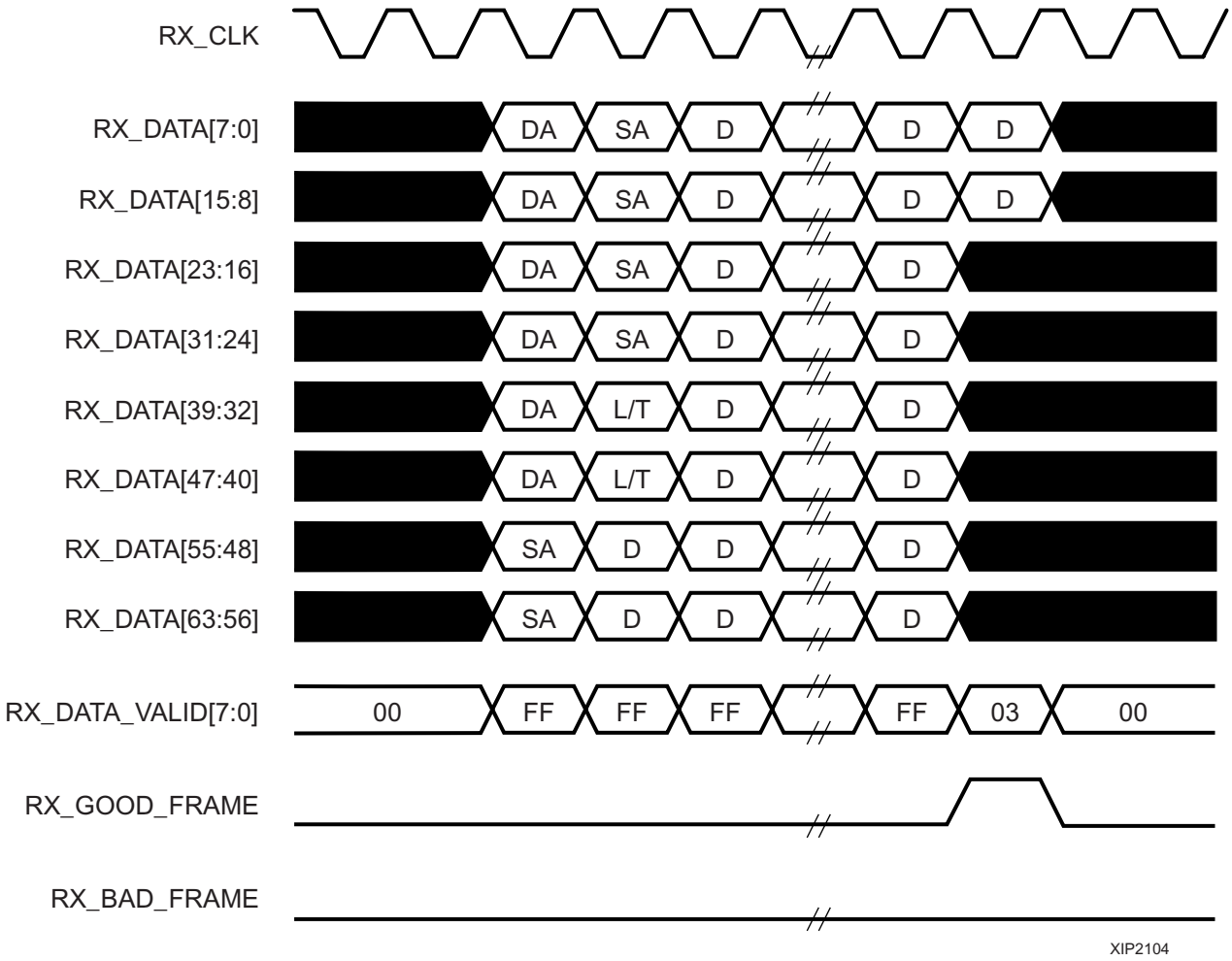


Figure 13: **Normal Frame Reception**

Frame parameters (destination address, source address, length/type and, optionally, FCS) are supplied on the data bus as shown on the timing diagram. The abbreviations are described in Table 9.

If the Length/Type field in the frame has the Length interpretation, and this indicates that the inbound frame has been padded to meet the Ethernet minimum frame size specification, this pad will not be passed to the client in the data payload. An exception to this occurs when FCS passing is enabled. See "Client-Supplied FCS Passing" on page 19.

There is always at least one clock cycle with RX_DATA_VALID = 0x00 between frames; *i.e.,* there's no valid data for this clock edge.

RX_GOOD_FRAME, RX_BAD_FRAME timing

Although the timing diagram in Figure 13 shows the RX_GOOD_FRAME signal asserted at the same time as the last valid data on RX_DATA, this is not always the case. The RX_GOOD_FRAME and RX_BAD_FRAME signals can in fact be asserted up to 7 clock cycles after the last valid data is presented; for example, this may result from padding at the end of the Ethernet frame. This is represented in Figure 14. Note that although RX_GOOD_FRAME is illustrated, the same timing applies to RX_BAD_FRAME.

Either the RX_GOOD_FRAME or RX_BAD_FRAME signal will, however, always be asserted before the next frame's data begins to appear on RX_DATA.

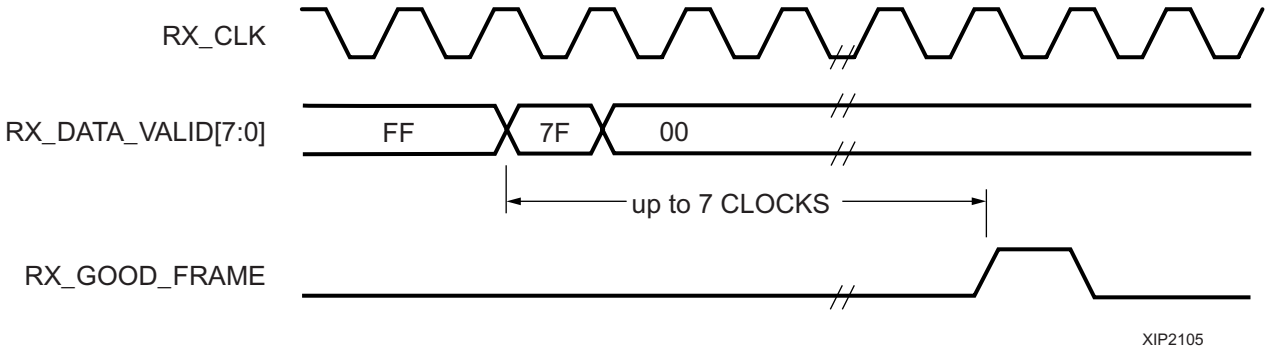


Figure 14: **Late Arrival of RX_GOOD_FRAME**

Frame Reception with Errors

The case of an unsuccessful frame reception (for example, a runt frame or a frame with an incorrect FCS) can be seen in Figure 15. In this case, the RX_BAD_FRAME signal is asserted to the client at the end of the frame. It is then the responsibility of the client to drop the data already transferred for this frame.

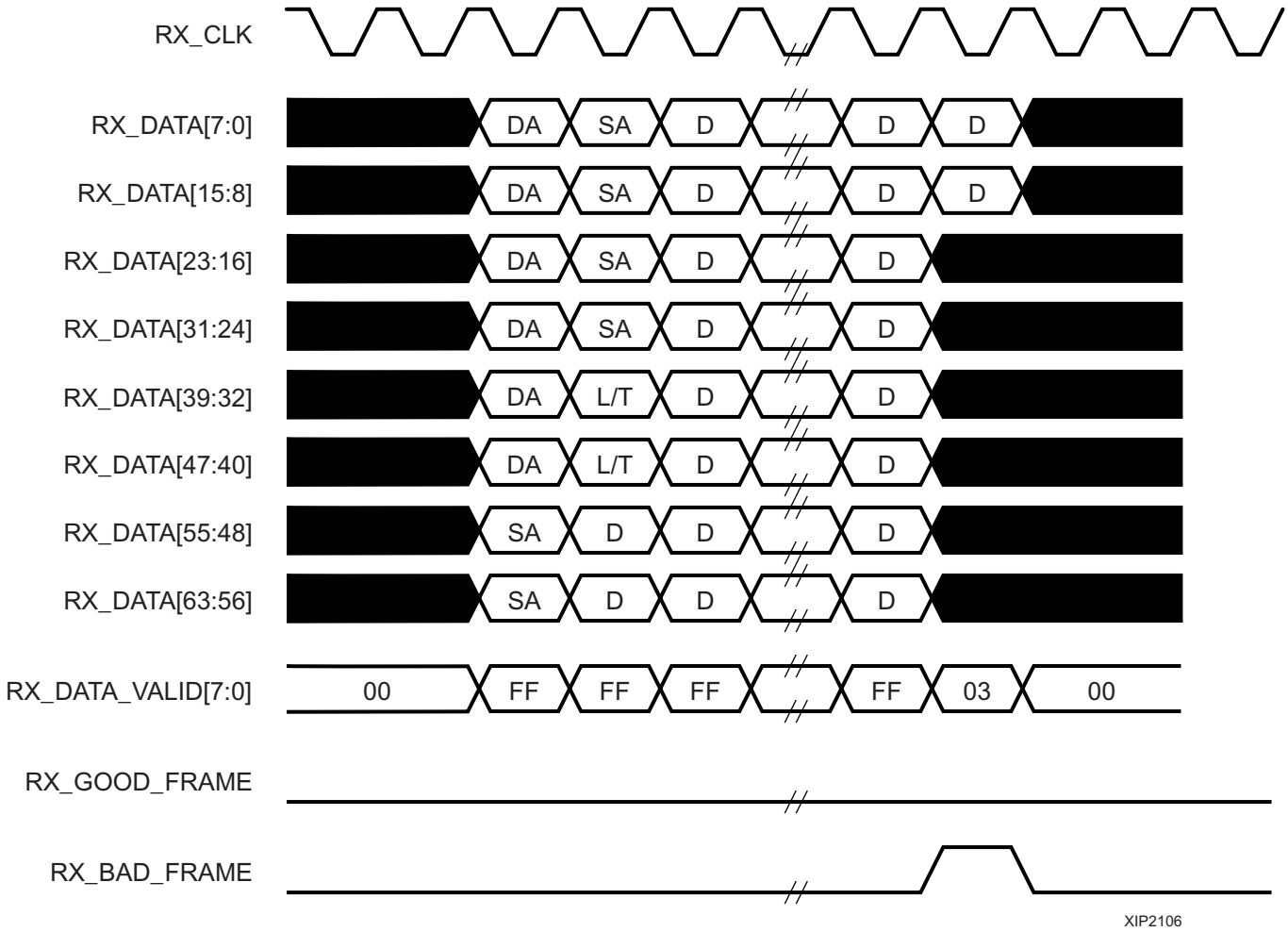


Figure 15: **Frame Reception with Error**

Client-Supplied FCS Passing

If the MAC core is configured to pass the FCS field to the client (see "Configuration Registers" on page 22), this is handled as shown in Figure 16.

In this case, any padding inserted into the frame to meet Ethernet minimum frame length specifications will be left intact and passed to the client.

Note that even though the FCS is passed up to the client, it is also verified by the MAC core, and RX_BAD_FRAME is asserted if the FCS check fails.

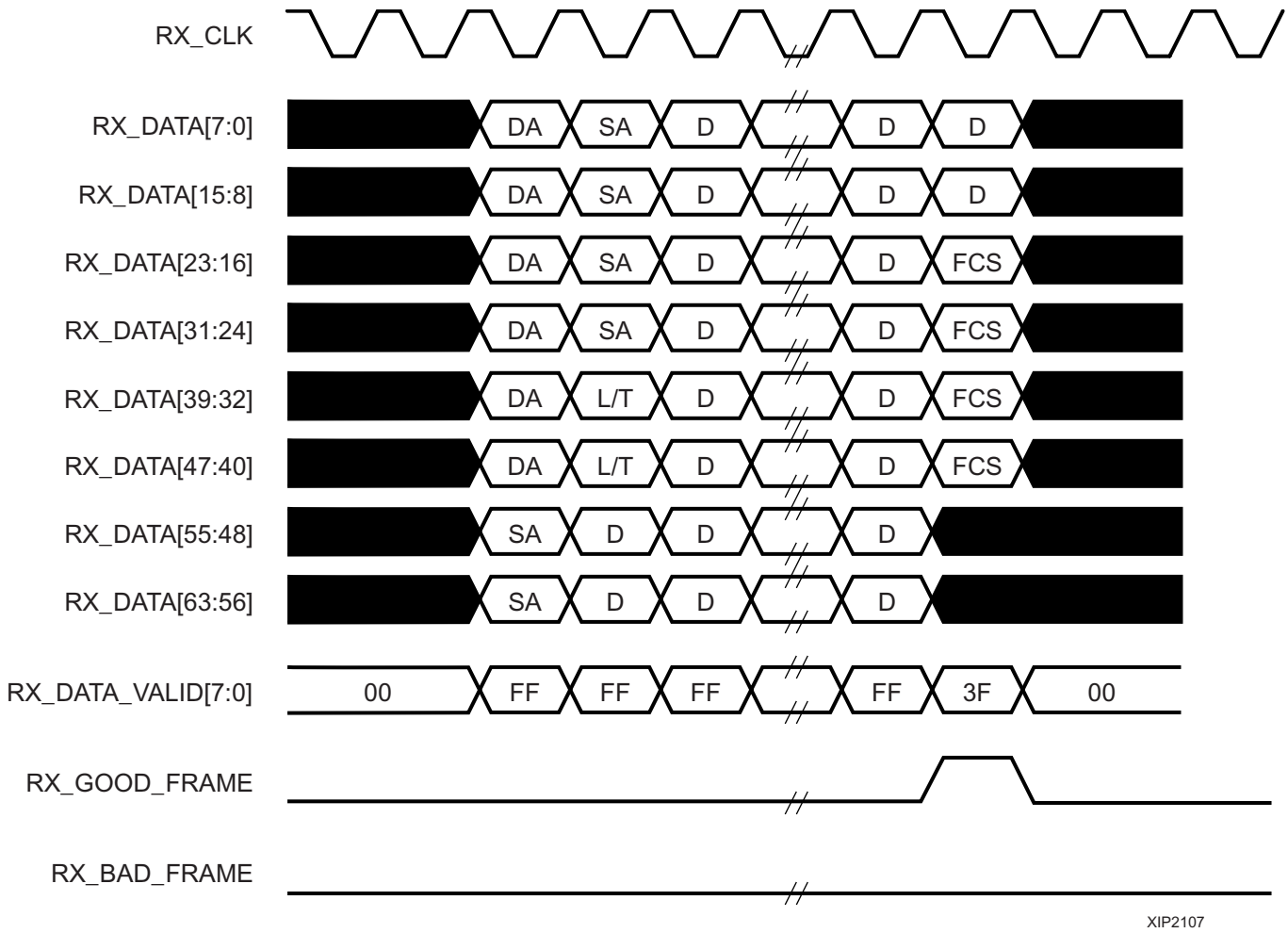


Figure 16: **Frame Reception with In-Band FCS Field**

VLAN Tagged Frames

The reception of a VLAN tagged frame (if enabled) is represented in Figure 17. The VLAN frame is passed to the client so that the frame can be identified as VLAN tagged; this is followed by the Tag Control Information bytes, V1 and V2. More information on the interpretation of these bytes can be found in IEEE 802.3ac-1998.

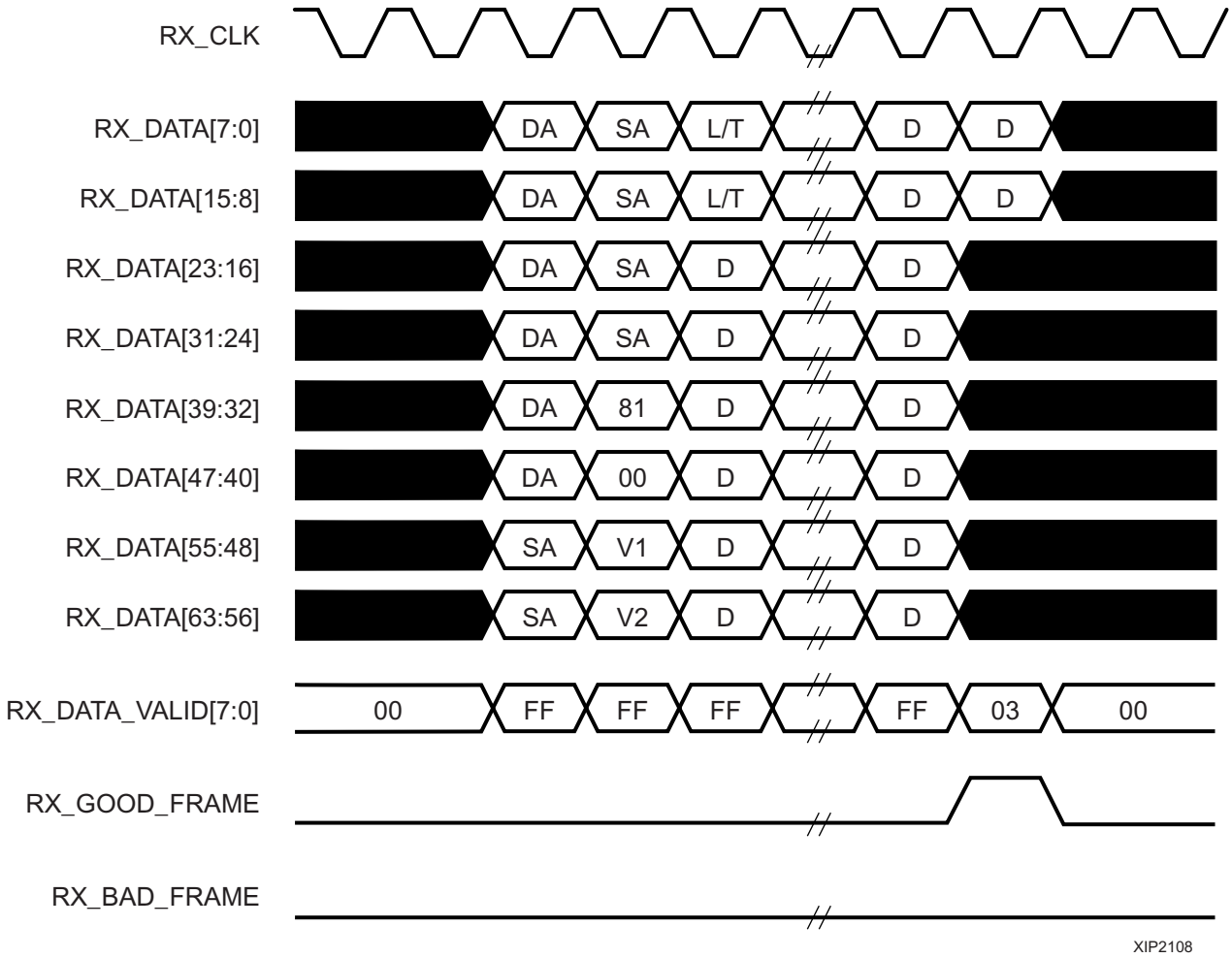


Figure 17: **Reception of a VLAN Tagged Frame**

Receive Statistics Vector

The statistics for the frame received are contained within the RX_STATISTICS_VECTOR. The vector is driven synchronously by the receiver clock, RX_CLK, following frame reception. The bit field definition for the Vector is defined in Table 11.

All bit fields, with the exception of BYTE_VALID, are valid only when RX_STATISTICS_VALID is asserted. This is illustrated in Figure 18. BYTE_VALID is significant on every RX_CLK cycle.

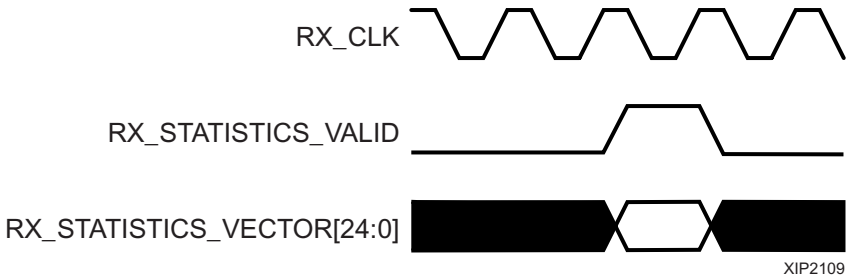


Figure 18: **Receiver Statistics Output Timing**

Table 11: **RX_STATISTICS_VECTOR Description**

RX Stats Vector Bit	Name	Description
24	Bad Opcode	The previous frame received was a flow control frame but contained an opcode that is not supported by the MAC.
23	Flow Control Frame	The previous frame was a flow control frame with a supported opcode.
22 to 19	Number of Bytes	A binary representation of the number of bytes received on the last clock cycle. This can range from 0 to 8. This is valid on every clock cycle, it is not validated by RX_STATISTICS_VALID.
18	VLAN Frame	The last received frame contained a VLAN tag in the length/type field.
17	Out of Bounds	The previous frame exceeded the maximum length of a frame. This is only valid when jumbo frames are disabled.
16	Control Frame	The last received frame contained the control frame identifier in the length/type field.
15 to 5	Frame Length Count	The length in bytes of the previous received frame. The count will stick at 2047 for any Jumbo frames larger than this value.
4	Multicast Frame	High if the destination address in the previous frame contained a multicast address.
3	Broadcast Frame	High if the destination address in the previous frame contained a broadcast address.
2	FCS Error	This is high if the last frame that was received had an incorrect FCS value.
1	Bad Frame	This is high when the last frame contained errors.
0	Good Frame	This is high if the last frame was error free.

Flow Control

The flow control block is designed to Clause 31 of the IEEE P802.3 Ethernet standard. The MAC can be configured to send pause frames and to act on their reception. These two behaviors can be configured asymmetrically; see "Configuration Registers" on page 22.

Transmitting a PAUSE Control Frame

The client sends a flow control frame by asserting PAUSE_REQ while the pause value is on the PAUSE_VAL bus. These signals are synchronous with respect to TX_CLK. The timing of this can be seen in Figure 19.

Figure 19: **Pause Request Timing**

If the MAC core is configured to support transmit flow control, this action causes the MAC core to transmit a PAUSE control frame on the link, with the PAUSE parameter set to the value on PAUSE_VAL in the cycle when PAUSE_REQ was asserted. This will not disrupt any frame transmission in progress but will take priority over any pending frame transmission.

Receiving a Pause Control Frame

When a pause frame is received by the MAC core and the MAC core is configured to act upon received pause frames, the following checks are made:

- The frame is checked to see whether it is well formed (is a valid Ethernet frame). If not, the frame is dropped
- If the Destination Address does not match the MAC Control Multicast address or the configured Source Address for the MAC (see "Configuration Registers" on page 22), the frame is passed to the client
- If the Length/Type field does not match the MAC Control Type code, the frame is passed up to the client
- If the opcode field contents do not match the PAUSE opcode, the frame is passed up to the client

If the frame passes all of these checks, the pause value parameter in the frame is then used to inhibit transmitter operation for the time defined in the Ethernet specification. This inhibit is implemented using the same back pressure scheme shown in Figure 9. Since the received pause frame has been acted upon, it is not passed up to the client by marking it as a bad frame.

Management Interface

The management interface is a processor-independent interface with standard address, data, and control signals. It can be used as-is, or a wrapper (not supplied) can be applied to interface to common bus architectures.

This interface is used for:

- configuring the MAC core
- accessing statistics information for use by high layers, *e.g.,* SNMP
- accessing an internal MIIM interface through the optional XAUI configuration and status registers
- accessing the MIIM interface through the management registers located in the PHY attached to the MAC core

The management interface is accessed differently, depending on the type of transaction; Table 12 is a truth table showing which access method is required for each transaction type. These access methods are described in the following sections.

Table 12: **Management Interface Transaction Types**

Transaction	HOST_MIIM_SEL	HOST_ADDR[9]
Configuration	0	1
Statistics	0	0
MIIM Access	1	X

HOST_CLK Frequency

The management interface clock, HOST_CLK, is used to derive the MIIM clock, MDC, and is therefore subject to some frequency restrictions. This HOST_CLK must be:

- ≥ 10 MHz
- ≤ 133 MHz

Configuring the MAC core to derive the MDC signal from this clock is detailed in MII Management Interface.

Configuration Registers

After power up or reset, the client can reconfigure some of the core parameters from their defaults, such as flow control support and WAN/LAN connections.

Configuration of the MAC core is performed through a register bank accessed through the management interface. The configuration registers available in the core are detailed in Table 13. As can be seen, the address has some implicit don't-care bits; the configuration words appear at all locations in the ranges described.

Table 13: **Configuration Registers**

Address	Description
0x200	Receiver Configuration (Word 0).
0x240	Receiver Configuration (Word 1).
0x280	Transmitter Configuration.
0x2C0	Flow Control Configuration.
0x300	Reconciliation Sublayer Configuration.
0x340	Management Configuration.

The register contents for the two receiver configuration words is shown in Table 14 and Table 15.

Table 14: **Receiver Configuration Word 0**

Bit	Default Value	Description
31-0	All “0s”	Pause frame MAC Address[31:0]. This address is used by the MAC to match against the Destination Address of any incoming flow control frames. It is also used by the flow control block as the Source Address (SA) for any outbound flow control frames. The address is ordered so the first byte transmitted/received is the lowest positioned byte in the register; for example, a MAC address of AA-BB-CC-DD-EE-FF would be stored in Address[47:0] as 0xFFEEDDCCBBAA.

Table 15: **Receiver Configuration Word 1**

Bit	Default Value	Description
15-0	All “0s”	Pause frame MAC Address[47:32]. See description in Table 14.
26-16	N/A	Reserved
27	0	VLAN Enable. When this bit is set to “1,” VLAN tagged frames will be accepted by the receiver. The maximum payload length will increase by 4 bytes.
28	1	Receiver Enable. If set to “1,” the receiver block will be operational. If set to “0,” the block will ignore activity on the XGMII RX port.
29	0	In-band CRC Enable. When this bit is “1,” the MAC receiver will pass the CRC up to the client as described in "Client-Supplied FCS Passing" on page 19. When it is “0,” the client will not be passed the FCS. In both cases, the FCS will be verified on the frame.
30	0	Jumbo Frame Enable. When this bit is set to “1,” the MAC receiver will accept frames of any length. When this bit is “0,” the MAC will only accept frames up to the Ethernet legal maximum.
31	0	Reset. When this bit is set to “1,” the receiver will be reset. The bit will then automatically revert to “0.” Note that this reset will also set all of the receiver configuration registers to their default values.

The register contents for the Transmitter Configuration Word are described in Table 16.

Table 16: **Transmitter Configuration Word**

Bit	Default Value	Description
24-0	N/A	Reserved
25	0	Interframe gap stretch mode. If this bit is set to “1,” the core will maintain an interframe gap of N cycles. N is set by the value appearing on the IFG_DELAY port. This value should be set along with the START signal and kept on the port until the DATA_ACK is received from the MAC. This bit has no effect when bit 26 (LAN/WAN mode) is set to “1.”
26	0	LAN/WAN Mode. When this bit is set to “1,” the transmitter will automatically insert extra idles into the inter frame gap (IFG) to reduce the average data rate to that of the OC-192 SONET payload rate (WAN mode). When this bit is set to 0, the transmitter will use normal Ethernet inter-frame gaps (LAN mode).
27	0	VLAN Enable. When this bit is set to “1,” the transmitter will allow the transmission of VLAN tagged frames.

Table 16: **Transmitter Configuration Word *(Continued)***

Bit	Default Value	Description
28	1	Transmit Enable. When this bit is “1,” the transmitter is operational. When it is “0,” the transmitter is disabled.
29	0	In-band CRC Enable. When this bit is “1,” the MAC transmitter will expect the CRC to be passed in by the client as described in "Client-supplied FCS passing" on page 9. When this bit is “0,” the MAC transmitter will append padding as required, compute the CRC and append it to the frame.
30	0	Jumbo Frame Enable. When this bit is set to “1,” the MAC transmitter will send frames of any length. When this bit is “0,” the MAC will only send frames up to the Ethernet legal maximum.
31	0	Reset. When this bit is set to “1,” the transmitter will be reset. The bit will then automatically revert to “0.” Note that this reset will also set all of the transmitter configuration registers to their default values.

The register contents for the Flow Control Configuration Word are described in Table 17.

Table 17: **Flow Control Configuration Word**

Bit	Default Value	Description
28-0	N/A	Reserved
29	1	Flow Control Enable (TX). When this bit is “1,” asserting the PAUSE_REQ signal will send a flow control frame out from the transmitter. When this bit is “0,” asserting the PAUSE_REQ signal has no effect.
30	1	Flow Control Enable (RX). When this bit is “1,” received flow control frames will inhibit the transmitter operation as described in "Receiving a Pause Control Frame" on page 21. When this bit is “0,” received flow control frames will be passed up to the client.
31	0	Reset. When this bit is set to “1,” the flow control block will be reset. The bit will then automatically revert to “0.” Note that this reset will also set all of the flow control configuration registers to their default values.

The register contents for the Reconciliation Sublayer Status Word are described in Table 18.

Table 18: **Reconciliation Sublayer Status Word**

Bits	Default Value	Description
27-0	N/A	Reserved
28	N/A	Local Fault. If this bit is “1,” the RS layer is receiving local fault sequence ordered sets. Read-only.
29	N/A	Remote Fault. If this bit is “1,” the RS layer is receiving remote fault sequence ordered sets. Read-only.
30	N/A	TXLOCK. If this bit is “1,” the Digital Clock Management (DCM) block for the transmit-side clocks (GTX_CLK, XGMII_TX_CLK, TX_CLK) is locked. If this bit is “0,” the DCM is not locked.
31	N/A	RXLOCK. If this bit is “1,” the Digital Clock Management (DCM) block for the receive-side clocks (XGMII_RX_CLK, RX_CLK) is locked. If this bit is “0,” the DCM is not locked.

The register contents for the Management Configuration Word are described in Table 19.

Table 19: **Management Configuration Word**

Bits	Default Value	Description
4-0	All “0s”	Clock Divide[4:0]. See "MII Management Interface" on page 28
5	0	MIIM Enable. When this bit is “1,” the MIIM interface can be used to access attached PHY devices. When this bit is “0,” the MIIM interface is disabled and the MDIO signal remains in a high impedance state.
31-6	N/A	Reserved.

Writing to the configuration registers through the management interface is depicted in Figure 20. When accessing the configuration registers (*i.e.,* when HOST_ADDR[9] = “1” and HOST_MIIM_SEL = “0”), the upper bit of HOST_OPCODE functions as an Active Low write-enable signal. The lower HOST_OPCODE bit is a “don’t care.”

Reading from the configuration register words is similar, except that the upper HOST_OPCODE bit should be “1,” as shown in Figure 21. In this case, the contents of the register appear on HOST_RD_DATA and the HOST_CLK edge after the register address is asserted onto HOST_ADDR.

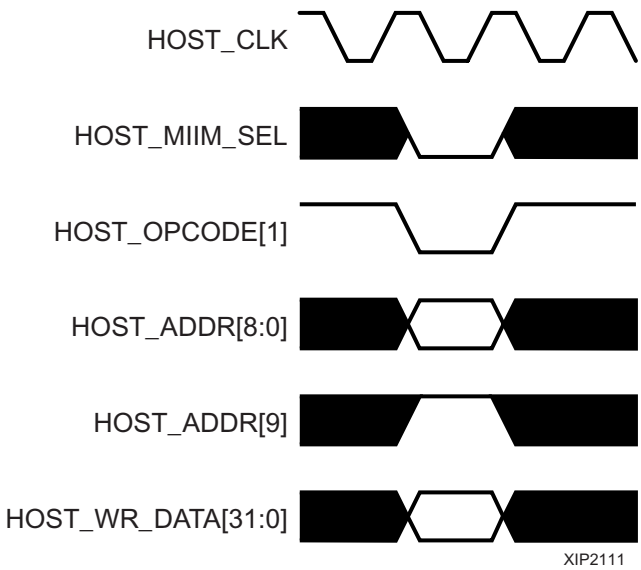


Figure 20: **Configuration Register Write Timing**

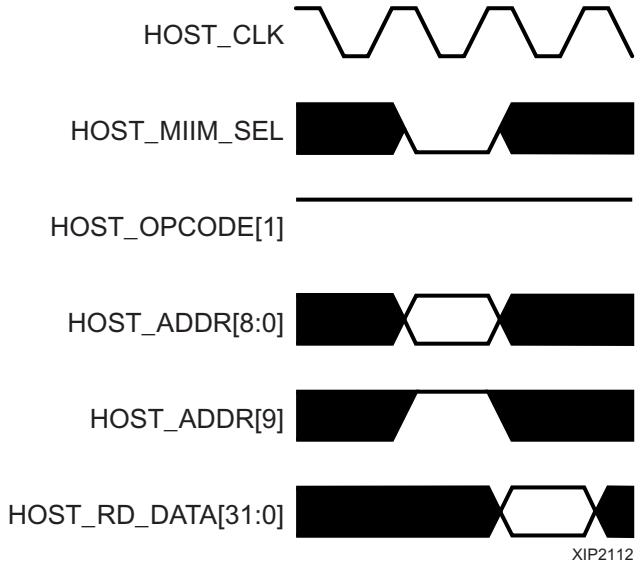


Figure 21: **Configuration Register Read Timing**

Operational Statistics

During operation, the MAC core collects statistics on the success and failure of various operations, for processing by station management entities (STA) further up the protocol stack. These statistics are accessed by the host through the management interface.

A complete list of statistics supported is described in Table 20. Each of these statistic registers is 64 bits wide and therefore must be read in a two-cycle transfer. The timing of this process is shown in Figure 22. Six clocks after the read transaction is initiated, the least significant word (LSW) of the statistics counter appears on the HOST_RD_DATA bus, and a clock cycle later the most significant word (MSW) appears. For accurate statistic values, 64 GTX_CLK ticks must elapse after the last frame is sent or received through the MAC core.

Table 20: **Statistics Registers**

Address	Description
0x000	Frames Received OK
0x001	Frame Check Sequence Errors
0x002	Broadcast Frames Received OK
0x003	Multicast Frames Received OK
0x004	64 byte Frames Received OK
0x005	65-127 byte Frames Received OK
0x006	128-255 byte Frames Received OK
0x007	256-511 byte Frames Received OK
0x008	512-1023 byte Frames Received OK
0x009	1024-1518 byte Frames Received OK
0x00A	Control Frames Received OK (*i.e.,* frames with Length/Type field matching the MAC Control Type code and having the Destination Address match either the Source Address in the configuration register or the MAC Control Multicast Address).
0x00B	Length/Type Out of Range
0x00C	VLAN Tagged Frames Received OK

Table 20: **Statistics Registers *(Continued)***

Address	Description
0x00D	Pause Frames Received OK (*i.e.,* Control Frames with an Opcode corresponding to a pause request)
0x00E	Control Frames Received with Unsupported Opcode
0x00F	Oversize Frames Received OK
0x010	Undersized Frames Received (less than minimum frame size with valid FCS field)
0x011	Fragment Frames Received (less than minimum frame size with invalid FCS field)
0x012	Number of Bytes Received (bytes counted from DA to FCS field inclusive)
0x013	Number of Bytes Transmitted (bytes counted from DA to FCS field inclusive)
0x020	Frames Transmitted
0x021	Broadcast Frames Transmitted
0x022	Multicast Frames Transmitted
0x023	Underrun Errors. Note: this will not count underrun frames of length < 64 bytes.
0x024	Control Frames Transmitted OK
0x025	64 byte Frames Transmitted OK
0x026	65-127 byte Frames Transmitted OK
0x027	128-255 byte Frames Transmitted OK
0x028	256-511 byte Frames Transmitted OK
0x029	512-1023 byte Frames Transmitted OK
0x02A	1024-1518 byte Frames Transmitted OK
0x02B	VLAN Tagged Frames Transmitted OK
0x02C	Pause Frames Transmitted OK
0x02D	Oversize Frames Transmitted OK

In general, frames that are declared “received OK” are well formed Ethernet frames with valid CRCs. Frames that are declared “transmitted OK” were sent out from the MAC with no errors introduced by the MAC.

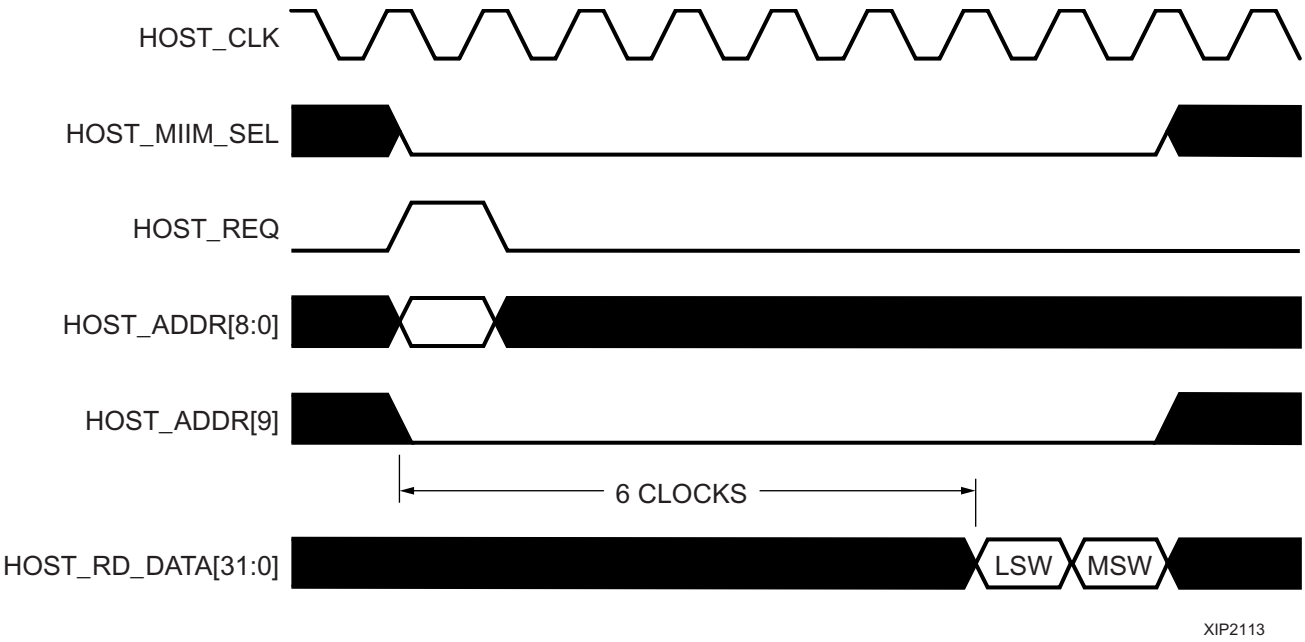


Figure 22: **Statistic Register Read Timing**

MII Management Interface

The management interface is also used to access the MII Management interface of the MAC core; this interface is used to access the Managed Information Block (MIB) of the PHY components attached to the MAC core.

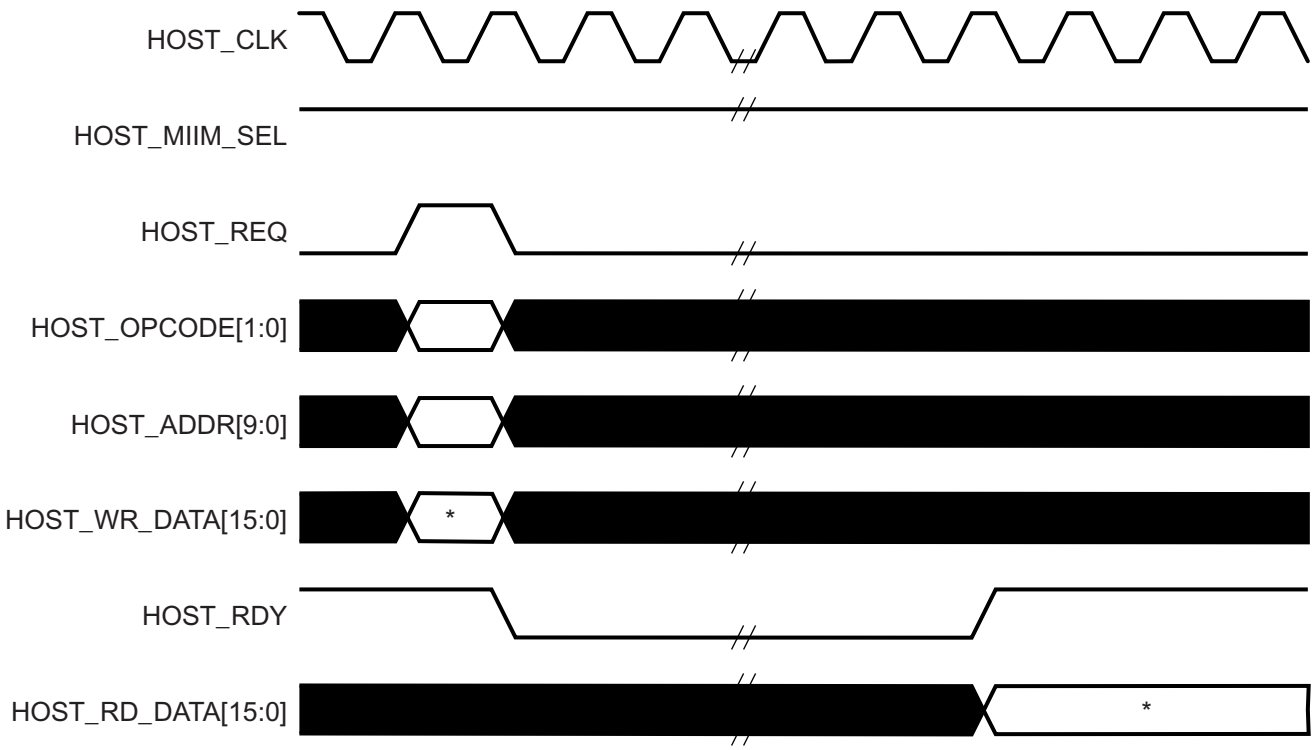
The MII Management interface supplies a clock to the external devices, MDC. This clock is derived from the HOST_CLK signal, using the value in the Clock Divide[4:0] configuration register. The frequency of the MII Management clock is given by the following equation:

$$f_{MDC} = \frac{f_{HOST\_CLK}}{\text{Clock Divide}[4:0] \times 2}$$

The frequency of MDC given by this equation should not exceed 2.5 MHz in order to comply with the IEEE specification for this interface. To prevent MDC from being out of specification, the Clock Divide[4:0] value powers up at 00000, and while this value is in the register, it is impossible to enable the MII Management interface.

For details of the register map of PHY layer devices and a fuller description of the operation of the MII Management interface itself, see IEEE draft specification P802.3ae D4.1.

Access to the MII Management interface through the management interface is depicted in the timing diagram in Figure 23.



* If a read transaction is initiated, the HOST_RD_DATA bus is valid at the point indicated. If a write transaction is initiated, the HOST_WR_DATA bus must be valid at the indicated point. Simultaneous read and write is not permitted.

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Figure 23: **MIIM Access Through Management Interface**

For MII Management transactions, the following points apply:

- HOST_OPCODE maps to the OP (opcode) field of the MII Management frame
- HOST_ADDR maps to the two address fields of the MII Management frame; PHY_ADDR is HOST_ADD[9:5], and REG_ADDR is HOST_ADD[4:0]
- HOST_WR_DATA[15:0] maps into the data field of the MII Management frame when performing a write operation
- The data field of the MII Management frame maps into HOST_RD_DATA[15:0]

The MAC core signals to the host that it is ready for an MII Management transaction by asserting HOST_MIIM_RDY. A read or write transaction on the MII Management is initiated by a pulse on the HOST_REQ signal. This pulse is ignored if the MII Management interface already has a transaction in progress.

The MAC core then disasserts the HOST_MIIM_RDY signal while the transaction across the MII Management interface is in progress. When the transaction across the MII Management interface has been completed, the HOST_MIIM_RDY signal will be asserted by the MAC core; if the transaction is a read, the data will also be available on the HOST_RD_DATA[15:0] bus at this time.

XGMII Interface

The optional XGMII interface is a 312Mbps DDR interface, as defined in clause 46 of IEEE P802.3ae D4.1. It is implemented using the Virtex-II DDR I/O buffer primitives and uses DCM to adjust clock/data alignment.

Clock Management

Figure 24 shows how the clocks are used and derived within the core when an XGMII interface is used.

Note that the GTX_CLK signal must have an input buffer IBUFG either instanced or inferred for correct operation of the core as shown. A DCM is then used to source this clock onto the global clock routing matrix.

Also note that the HOST_CLK signal does not have a BUFG instanced within the core; this clock buffer must be instanced or inferred by the core user.

The XGMII_RX_CLK is received through an IBUFG. This clock is then routed onto a global clock network by connecting it through a DCM to a BUFG: this global clock is used by all MAC receiver logic. The MAC Client can obtain this clock by connecting to the RX_CLK signal output from the core.

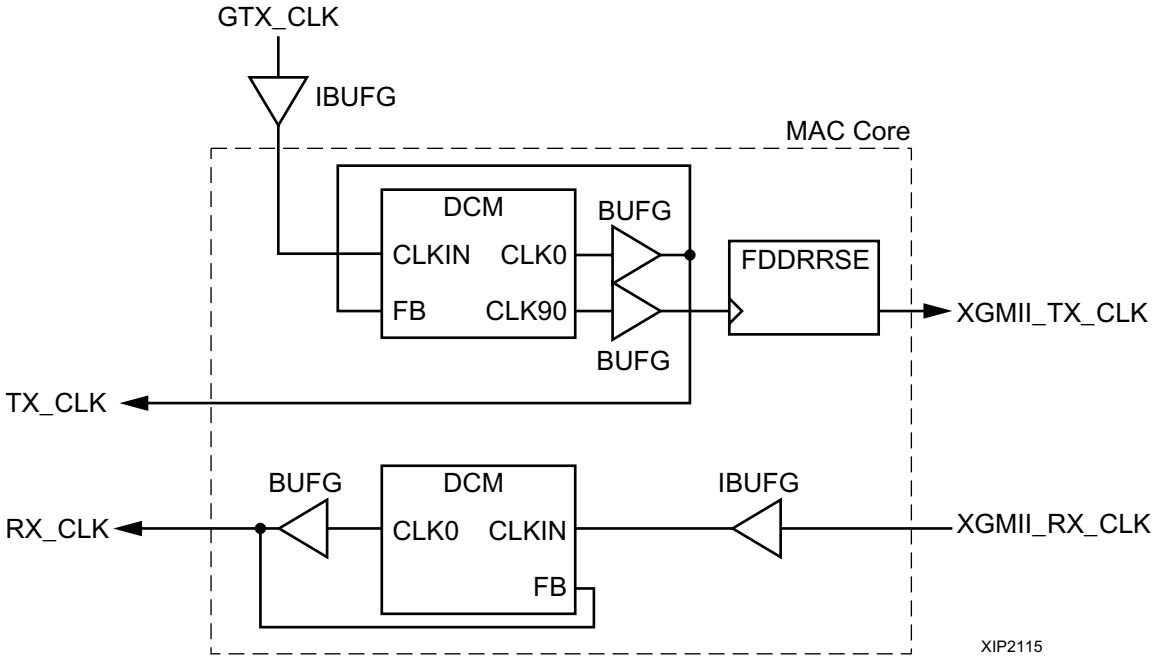

Figure 24: **Clock Management in core with XGMII interface**

Pin Location Considerations

The MAC core allows for a flexible pinout of the XGMII and the exact pin locations are left to the designer. In doing so, codes of practice and device restrictions must be followed.

Every Virtex-II and Virtex-II Pro device has 8 separate IO Banks. Each IO Bank has Output Drive Source Voltage Pads (Vcco) that must be connected to the same external voltage reference. For XGMII, this must be 1.5 volts. This will force all IO pads within the bank to operate at this voltage level.

IO standards, including HSTL, which use input differential amplifiers, require voltage reference inputs (Vref). These are automatically configured by the place and route tool onto predefined pins (see the *Virtex-II User Guide* or *Virtex-II Pro User Guide* for all devices and packages). Approximately one of every 12 IO pins within an IO bank will be configured as a Vref pin. For XGMII which uses HSTL_I, all Vref pins must be connected externally to 0.75 volts.

IOs should be grouped in their own separate clock domains. XGMII contains two of these: XGMII_RXD[31:0] and XGMII_RXC[3:0], which are centered with respect to XGMII_RX_CLK; XGMII_TXD[31:0] and XGMII_TXC[3:0], which are centered with respect to XGMII_TX_CLK. It is recommended that these be separated into separate IO Banks. Unused IOs in these banks, if tied to ground, will help to reduce jitter by providing a low impedance path for ground currents.

XAUI Interface

The optional XAUI interface is a 4-lane, 3.125Gbps-per-lane current mode logic interface, as defined in clauses 47 and 48 of IEEE P802.3ae D4.1.

A diagram of the XAUI block is shown in Figure 25. The main components of the XAUI block are:

- the transmitter component
- the receiver component
- the management register component
- the RocketIO Multi Gigabit Transceivers (MGTs)

The management registers of the XAUI block have an MIIM interface which is accessed through the core host interface as if it were an externally connected PHY.

The RocketIO MGTs provide some of the XAUI functionality, such as 8B10B encoding/decoding and the PMA serdes. The synchronization and idle pattern generation logic are generated as CLB logic.

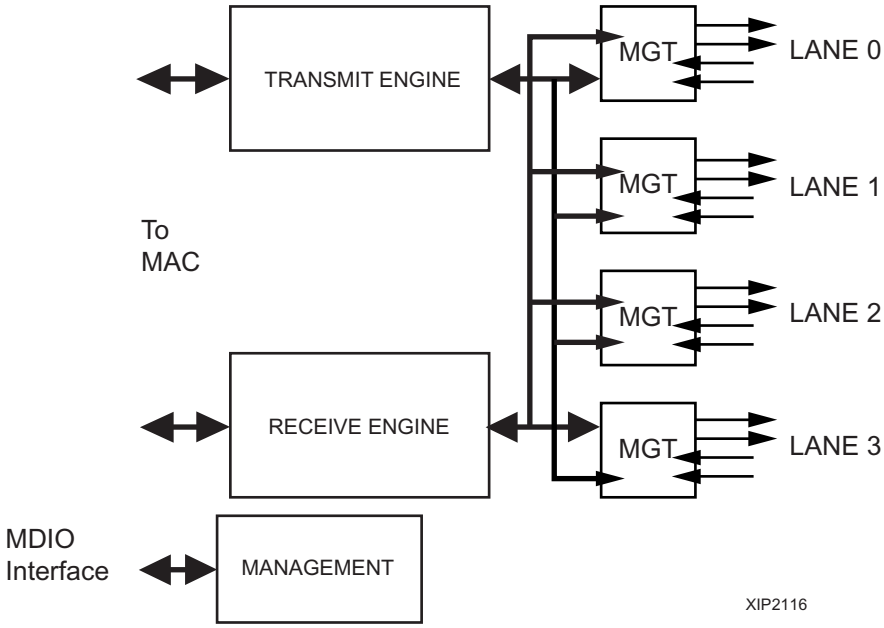

Figure 25: **Functional diagram of the XAUI block**

Clock Management

Figure 26 shows how the clocks are used and derived within the core when an XAUI interface is used.

Note that the REF_CLK signal must have an input buffer either instanced or inferred for correct operation of the core. This REFCLK signal must be a High purity clock as specified for RocketIO reference clocks in the *Virtex-II Pro User Guide.*

Also note that the HOST_CLK signal does not have a BUFG instanced within the core; this clock buffer must be instanced or inferred by the core user.

In this configuration, the TX_CLK and RX_CLK signals are actually the same net; the elastic buffer in the MGT is used to cross into a common clock domain. If only the XAUI configuration is to be used in the final application, some optimizations to client logic can be made.

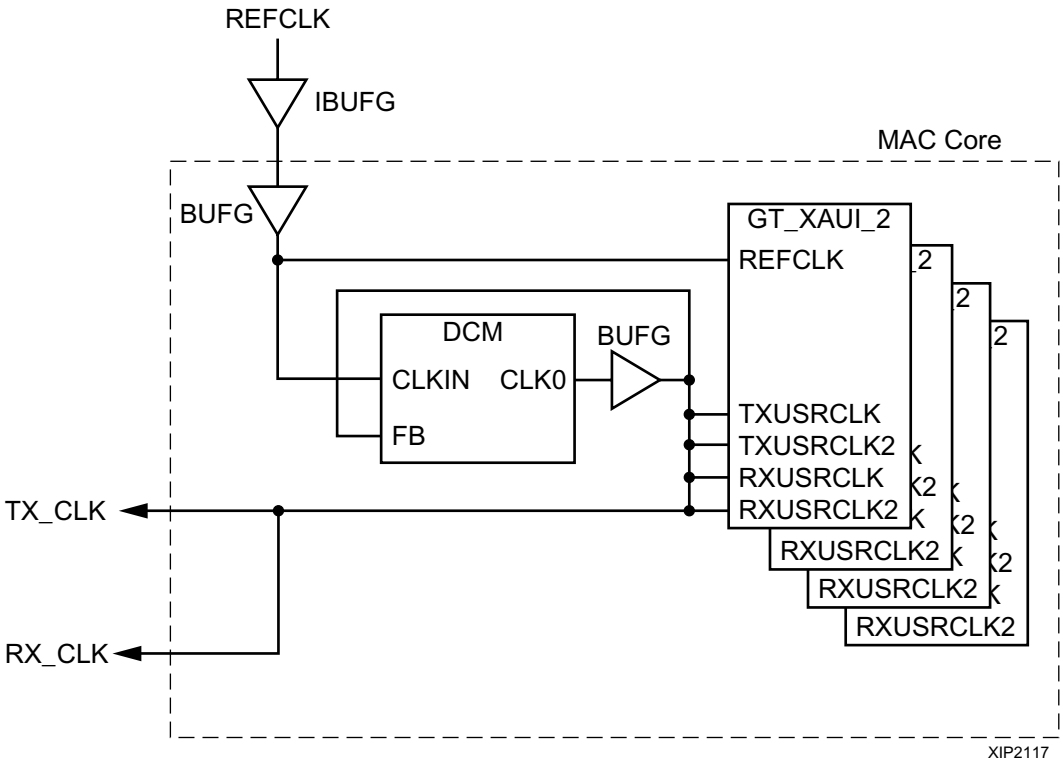

Figure 26: **Clock Management in core using XAUI interface**

Pin Location Considerations

The four MGTs of the XAUI block are channel bonded as described in the *Virtex-II Pro User's Guide*. The Lane 0 MGT is the channel bond master, Lanes 1 and 2 are 1-hop slaves, and Lane 3 is a 2-hop slave.

It is therefore recommended that if the XAUI interface is to be split across the top and bottom of the FPGA, lanes 0 and 1 are placed on one edge and lanes 2 and 3 on the opposite edge, with lane 0 and lane 2 aligned vertically with each other. This will allow the optimum routing for the time-critical channel bonding signals.

XAUI Register Block

The XAUI core contains registers as defined in Clause 45 of the IEEE P802.3ae D4.1 draft. If the XAUI_TYPE_SEL pin is "1," the register set is that of a DTE XGXS entity. If the XAUI_TYPE_SEL pin is "0," the register set is that of a 10GBASE-X PCS/PMA entity. Note that this pin is registered into the core at power-up and hard reset, and cannot be changed after that time; it is intended to be a static flag. These registers are accessed through the MIIM interface of the MAC. The XAUI_PRTAD port designates the address of the XAUI/PCS on the MIIM interface.

DTE XGXS Registers

The management registers for the DTE XGXS implementation of the XAUI block are shown in Table 21; the DTE XGXS occupies device address 5.

Table 21: **DTE XGXS Registers**

Register Address	Register Name
5.0	DTE XS Control 1
5.1	DTE XS Status 1
5.2,3	Device Identifier
5.4	DTE XS Speed Ability
5.5,6	Devices in Package
5.7	Reserved
5.8	DTE XS Status 2
5.9 to 5.13	Reserved
5.14,15	Package Identifier
5.16 to 5.23	Reserved
5.24	10G DTE XGXS Lane Status
5.25	10G DTE XGXS Test Control
5.26 to 5.65 535	Reserved

The DTE XS Control Register is described in Table 22.

Table 22: **DTE XS Control Register 1 (Register 5.0)**

Bit(s)	Name	Description	Attributes	Default Value
5.0.15	Reset	1 = block reset 0 = normal operation The XAUI block is reset when this bit is set to “1.” It returns to “0” when the reset is complete.	R/W Self-clearing	0
5.0.14	Loopback	1 = enable loopback mode 0 = disable loopback mode The XAUI block will loop the signal in the MGTs back into the receiver.	R/W	0
5.0.13	Speed selection	The block always returns “1” for this bit and ignores writes.	R/O	1
5.0.12	Reserved	The block always returns “0” for this bit and ignores writes.	R/O	0
5.0.11	Power down	1 = Power down mode 0 = Normal operation When set to “1,” the MGTs are placed in a low power state. This bit requires a reset (see bit 5.0.15) to clear.	R/W	0
5.0.10:7	Reserved	The block always returns “0s” for these bits and ignores writes.	R/O	0
5.0.6	Speed selection	The block always return “1” for this bit and ignores writes.	R/O	1
5.0.5:2	Speed Selection	The block always returns “0s” for these bits and ignores writes.	R/O	All “0s”
5.0.1:0	Reserved	The block always returns “0s” for these bits and ignores writes.	R/O	All “0s”

The DTE XS Status Register is described in Table 23.

Table 23: **DTE XS Status Register 1 (Register 5.1)**

Bit(s)	Name	Description	Attributes	Default Value
5.1.15:8	Reserved	The block always returns “0s” for these bits and ignores writes.	R/O	All “0s”
5.1.7	Local Fault	1 = Local fault detected 0 = no local fault detected This bit is set to “1” whenever either of the bits 5.8.11, 5.8.10 are set to “1.”	R/O	-
5.1.6:3	Reserved	The block always returns “0s” for these bits and ignores writes.	R/O	All “0s”

Table 23: **DTE XS Status Register 1 (Register 5.1) *(Continued)***

Bit(s)	Name	Description	Attributes	Default Value
5.1.2	DTE XS Receive Link Status	1 = the DTE XS receive link is up 0 = the DTE XS receive link is down This is a latching low version of bit 5.24.12.	R/O Self-setting	-
5.1.1	Power down ability	The block always returns “1” for this bit.	R/O	1
5.1.0	Reserved	The block always returns “0” for this bit and ignores writes.	R/O	0

The DTE XS Identifier Register is described in Table 24.

Table 24: **DTE XS Identifier (Registers 5.2 and 5.3)**

Bit(s)	Name	Description	Attributes	Default Value
5.2.15:0	DTE XS Identifier	The block always returns “0” for these bits and ignores writes	R/O	All “0s”
5.3.15:0	DTE XS Identifier	The block always returns “0” for these bits and ignores writes	R/O	All “0s”

The DTE XS Speed Ability Register is described in Table 25.

Table 25: **DTE XS Speed Ability Register (Register 5.4)**

Bit(s)	Name	Description	Attribute	Default Value
5.4.15:1	Reserved	The block always returns “0” for these bits and ignores writes	R/O	All “0s”
5.4.0	10G Capable	The block always returns “1” for this bit and ignores writes.	R/O	1

The Devices in Package Register is described in Table 26.

Table 26: **Devices in Package (Register 5.5 and 5.6)**

Bit(s)	Name	Description	Attributes	Default Value
5.6.15	Vendor-specific device present	The block always returns “0” for this bit.	R/O	0
5.6.14:0	Reserved	The block always returns “0” for these bits.	R/O	All “0s”
5.6.15:6	Reserved	The block always returns “0” for these bits.	R/O	All “0s”
5.5.5	DTE XS Present	The block always returns “1” for this bit.	R/O	All “0s”
5.5.4	PHY XS Present	The block always returns “0” for this bit.	R/O	0
5.5.3	PCS Present	The block always returns “0” for this bit.	R/O	0
5.5.2	WIS Present	The block always returns “0” for this bit.	R/O	0
5.5.1	PMA/PMD Present	The block always returns “0” for this bit.	R/O	0
5.5.0	Clause 22 device present	The block always returns “0” for this bit.	R/O	0

The DTE XS Status Register 2 is described in Table 27.

Table 27: **DTE XS Status Register 2 (Register 5.8)**

Bit(s)	Name	Description	Attributes	Default Value
5.8.15:14	Device present	The block shall always return “10.”	R/O	“10”
5.8.13:12	Reserved	The block always returns “0” for these bits.	R/O	All “0s”
5.8.11	Transmit Local Fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	R/O Latching high	-
5.8.10	Receive local fault	1 = Fault condition on receive path 0 = No fault condition on receive path	R/O Latching high	-
5.8.9:0	Reserved	The block always returns “0” for these bits.	R/O	All “0s”

The Package Identifier Register is described in Table 28

Table 28: **Package Identifier (Registers 5.14 and 5.15)**

Bit(s)	Name	Description	Attributes	Default Value
5.14.15:0	Package Identifier	The block always returns “0” for these bits.	R/O	All “0s”
5.15.15:0	Package Identifier	The block always returns “0” for these bits.	R/O	All “0s”

The DTE Lane Status Register is described in Table 29

Table 29: **DTE XS Lane Status Register (Register 5.24)**

Bit(s)	Name	Description	Attributes	Default Value
5.24.15:13	Reserved	The block always returns “0” for these bits.	R/O	All “0s”
5.24.12	DTE XGXS Lane Alignment Status	1 = DTE XGXS receive lanes aligned; 0 = DTE XGXS receive lanes not aligned.	RO	-
5.24.11	Pattern testing ability	The block always returns “1” for this bit.	R/O	1
5.24.10:4	Reserved	The block always returns “0” for these bits.	R/O	All “0s”
5.24.3	Lane 3 Sync	1 = Lane 3 is synchronized; 0 = Lane 3 is not synchronized.	R/O	-
5.24.2	Lane 2 Sync	1 = Lane 2 is synchronized; 0 = Lane 2 is not synchronized.	R/O	-
5.24.1	Lane 1 Sync	1 = Lane 1 is synchronized; 0 = Lane 1 is not synchronized.	R/O	-
5.24.0	Lane 0 Sync	1 = Lane 0 is synchronized; 0 = Lane 0 is not synchronized.	R/O	-

The DTE XS Test Control Register is shown in Table 30.

Table 30: **10G DTE XS Test Control register (Register 5.25)**

Bit(s)	Name	Description	Attributes	Default Value
5.25.15:3	Reserved	The block always returns “0” for these bits.	R/O	All “0s”
5.25.2	Transmit test pattern enable	1 = Transmit test pattern enable 0 = Transmit test pattern disabled	R/W	0
5.25.1:0	Test pattern select	11 = reserved 10 = mixed frequency test pattern 01 = low frequency test pattern 00 = high frequency test pattern	R/W	“00”

10GBASE-X PCS/PMA Registers

The management registers for the 10GBASE-X PCS/PMA implementation of the XAUI block are shown in Table 31. The 10GBASE-X PCS/PMA occupies device addresses 1 and 3.

Table 31: **10GBASE-X PCS/PMA Registers**

Register Address	Register Name
1.0	PMA/PMD Control 1
1.1	PMA/PMD Status 1
1.2,3	Device Identifier
1.4	PMA/PMD Speed Ability
1.5,6	Devices in Package
1.7	10G PMA/PMD Control 2
1.8	10G PMA/PMD Status 2
1.9	Reserved
1.10	10G PMD Receive Signal OK
1.11 to 1.13	Reserved
1.14,15	Package Identifier
1.16 to 1.65 535	Reserved
3.0	PCS Control 1
3.1	PCS Status 1
3.2,3	Device Identifier
3.4	PCS Speed Ability
3.5,6	Devices in Package
3.7	10G PCS Control 2
3.8	10G PCS Status 2
3.9 to 3.13	Reserved
3.14,15	Package Identifier
3.16 to 3.23	Reserved
3.24	10GBASE-X PCS Status
3.25	10GBASE-X PCS Test Control
3.26 to 3.65 535	Reserved

The PMA/PMD Control Register 1 is described in Table 32.

Table 32: **PMA/PMD Control Register 1 (Register 1.0)**

Bit(s)	Name	Description	Attributes	Default Value
1.0.15	Reset	1 = block reset 0 = normal operation The XAUI block is reset when this bit is set to “1.” It returns to “0” when the reset is complete.	R/W Self-clearing	0
1.0.14	Reserved	The block always returns “0” for this bit and ignores writes.	R/O	0
1.0.13	Speed Selection	The block always returns “1” for this bit and ignores writes.	R/O	1
1.0.12	Reserved	The block always returns “0” for this bit and ignores writes.	R/O	0
1.0.11	Power down	1 = Power down mode 0 = Normal operation When set to “1,” the MGTs are placed in a low power state. This bit requires a reset (see bit 1.0.15) to clear.	R/W	0
1.0.10:7	Reserved	The block always returns “0” for these bits and ignores writes.	R/O	All “0s”
1.0.6	Speed selection	The block always return “1” for this bit and ignores writes.	R/O	1
1.0.5:2	Speed Selection	The block always returns “0s” for these bits and ignores writes.	R/O	All “0s”
1.0.1	Reserved	The block always returns “0” for this bit and ignores writes	R/O	All “0s”
1.0.0	Loopback	1 = enable loopback mode 0 = disable loopback mode The XAUI block will loop the signal in the MGTs back into the receiver.	R/W	0

The PMA/PMD Status Register 1 is described in Table 33.

Table 33: **PMA/PMD Status Register 1 (Register 1.1)**

Bit(s)	Name	Description	Attributes	Default Value
1.1.15:8	Reserved	The block always returns “0” for this bit.	R/O	0
1.1.7	Local Fault	1 = Local fault detected 0 = no local fault detected This bit is set to “1” whenever either of the bits 1.8.11, 1.8.10 are set to “1.”	R/O	-
1.1.6:3	Reserved	The block always returns “0” for this bit.	R/O	0
1.1.2	Receive link Status	The block always returns “1” for this bit.	R/O	1
1.1.1	Power down ability	The block always returns “1” for this bit.	R/O	1
1.1.0	Reserved	The block always returns “0” for this bit.	R/O	0

The Device Identifier Register is described in Table 34.

Table 34: **Device Identifier (Registers 1.2 and 1.3)**

Bit(s)	Name	Description	Attributes	Default Value
1.2.15:0	DTE XS Identifier	The block always returns “0” for these bits and ignores writes.	R/O	All “0s”
1.3.15:0	DTE XS Identifier	The block always returns “0” for these bits and ignores writes.	R/O	All “0s”

The PMA/PMS Speed Ability Register is shown in Table 35.

Table 35: **PMA/PMD Speed Ability Register (Register 14)**

Bit(s)	Name	Description	Attribute	Default Value
1.4.15:1	Reserved	The block always returns “0” for these bits and ignores writes.	R/O	All “0s”
1.4.0	10G Capable	The block always returns “1” for this bit and ignores writes.	R/O	1

The Devices in Package Register is described in Table 36

Table 36: **Devices in Package (Register 1.5 and 1.6)**

Bit(s)	Name	Description	Attributes	Default Value
1.6.15	Vendor-specific device present	The block always returns “0” for this bit.	R/O	0
1.6.14:0	Reserved	The block always returns “0” for these bits.	R/O	All “0s”
1.6.15:6	Reserved	The block always returns “0” for these bits.	R/O	All “0s”
1.5.5	DTE XS Present	The block always returns “0” for this bit.	R/O	0
1.5.4	PHY XS Present	The block always returns “0” for this bit.	R/O	0
1.5.3	PCS Present	The block always returns “1” for this bit.	R/O	1
1.5.2	WIS Present	The block always returns “0” for this bit.	R/O	0
1.5.1	PMA/PMD Present	The block always returns “1” for this bit.	R/O	1
1.5.0	Clause 22 device present	The block always returns “0” for this bit.	R/O	0

The 10G PMA/PMD Control Register 2 is described in Table 37.

Table 37: **10G PMA/PMD Control Register 2 (Register 1.7)**

Bit(s)	Name	Description	Attributes	Default Value
1.7.15:3	Reserved	The block always returns “0” for these bits and ignores writes	R/O	All “0s”
1.7.2:0	PMA/PMD Type Selection	The block always returns “100” for these bits and ignores writes. This corresponds to the 10GBASE-X PMA/PMD.	R/O	“100”

The 10G PMA/PMD Status Register 2 is described in Table 38

Table 38: **10G PMA/PMD Status Register 2 (Register 1.8)**

Bit(s)	Name	Description	Attributes	Default Value
1.8.15:14	Device Present	The block always returns “10” for these bits.	R/O	“10”
1.8.13	Transmit Local Fault Ability	The block always returns “0” for this bit.	R/O	0
1.8.12	Receive Local Fault Ability	The block always returns “0” for this bit.	R/O	0
1.8.9	Reserved	The Block always returns “0” for this bit.	R/O	0
1.8.8	PMD Transmit Disable Ability	The block always returns “0” for this bit.	R/O	0
1.8.7	10GBASE-SR Ability	The block always returns “0” for this bit.	R/O	0
1.8.6	10GBASE-LR Ability	The block always returns “0” for this bit.	R/O	0
1.8.5	10GBASE-ER Ability	The block always returns “0” for this bit.	R/O	0
1.8.4	10GBASE-LX4 Ability	The block always returns “1” for this bit.	R/O	1
1.8.3	10GBASE-SW Ability	The block always returns “0” for this bit.	R/O	0
1.8.2	10GBASE-LW Ability	The block always returns “0” for this bit.	R/O	0
1.8.1	10GBASE-EW Ability	The block always returns “0” for this bit.	R/O	0
1.8.0	PMA Loopback Ability	The block always returns “1” for this bit.	R/O	1

The 10G PMD Signal Receive OK Register is described in Table 39.

Table 39: **10G PMD Signal Receive OK Register (Register 1.10)**

Bit(s)	Name	Description	Attributes	Default Value
1.10.15:5	Reserved	The block always returns “0s” for these bits.	R/O	All “0s”
1.10.4	PMD receive signal OK 3	1 = Signal OK on receive lane 3 0 = Signal not OK on receive lane 3 This is the value of the SIGNAL_DETECT[3] port.	R/O	-
1.10.3	PMD receive signal OK 2	1 = Signal OK on receive lane 2 0 = Signal not OK on receive lane 2 This is the value of the SIGNAL_DETECT[2] port.	R/O	-
1.10.2	PMD receive signal OK 1	1 = Signal OK on receive lane 1 0 = Signal not OK on receive lane 1 This is the value of the SIGNAL_DETECT[1] port.	R/O	-
1.10.1	PMD receive signal OK 0	1 = Signal OK on receive lane 0 0 = Signal not OK on receive lane 0 This is the value of the SIGNAL_DETECT[0] port.	R/O	-
1.10.0	Global PMD Receive Signal OK	1 = Signal OK on all receive lanes 0 = signal not OK on all receive lanes	R/O	-

The Package Identifier Register is described in Table 40.

Table 40: **Package Identifier (Registers 1.14 and 1.15)**

Bit(s)	Name	Description	Attributes	Default Value
1.14.15:0	Package Identifier	The block always returns “0” for these bits.	R/O	All “0s”
1.15.15:0	Package Identifier	The block always returns “0” for these bits.	R/O	All “0s”

The PCS Control Register 1 is described in Table 41.

Table 41: **PCS Control Register 1 (Register 3.0)**

Bit(s)	Name	Description	Attributes	Default Value
3.0.15	Reset	1 = block reset 0 = normal operation The XAUI block is reset when this bit is set to “1.” It returns to “0” when the reset is complete.	R/W Self-clearing	0
3.0.14	10GBASE-R Loopback	The block always returns “0” for this bit and ignores writes.	R/O	0
3.0.13	Speed Selection	The block always returns “1” for this bit and ignores writes.	R/O	1
3.0.12	Reserved	The block always returns “0” for this bit and ignores writes.	R/O	0

Table 41: **PCS Control Register 1 (Register 3.0) *(Continued)***

Bit(s)	Name	Description	Attributes	Default Value
3.0.11	Power down	1 = Power down mode 0 = Normal operation When set to “1,” the MGTs are placed in a low power state. This bit requires a reset (see bit 3.0.15) to clear.	R/W	0
3.0.10:7	Reserved	The block always returns “0” for these bits and ignores writes.	R/O	All “0s”
3.0.6	Speed selection	The block always return “1” for this bit and ignores writes.	R/O	1
3.0.5:2	Speed Selection	The block always returns “0s” for these bits and ignores writes.	R/O	All “0s”
3.0.1:0	Reserved	The block always returns “0” for this bit and ignores writes	R/O	All “0s”

The PCS Status Register 1 is described in Table 42.

Table 42: **PCS Status Register 1 (Register 3.1)**

Bit(s)	Name	Description	Attributes	Default Value
3.1.15:8	Reserved	The block always returns “0”s for these bits and ignores writes	R/O	All “0s”
3.1.7	Local Fault	1 = Local fault detected 0 = no local fault detected This bit is set to “1” whenever either of the bits 3.8.11, 3.8.10 are set to “1.”	R/O	-
3.1.6:3	Reserved	The block always returns “0s” for these bits and ignores writes	R/O	All “0s”
3.1.2	PCS Receive Link Status	1 = the PCS receive link is up 0 = the PCS receive link is down This is a latching low version of bit 3.24.12	R/O Self-setting	-
3.1.1	Power down ability	The block always returns “1” for this bit.	R/O	1
3.1.0	Reserved	The block always returns “0” for this bit and ignores writes	R/O	0

The Device Identifier Register is described in Table 43.

Table 43: **Device Identifier (Registers 3.2 and 3.3)**

Bit(s)	Name	Description	Attributes	Default Value
3.2.15:0	PCS Identifier	The block always returns “0” for these bits and ignores writes	R/O	All “0s”
3.3.15:0	PCS Identifier	The block always returns “0” for these bits and ignores writes	R/O	All “0s”

The PCS Speed Ability Register is described in Table 44.

Table 44: **PCS Speed Ability Register (Register 3.4)**

Bit(s)	Name	Description	Attribute	Default Value
3.4.15:1	Reserved	The block always returns “0” for these bits and ignores writes.	R/O	All “0s”
3.4.0	10G Capable	The block always returns “1” for this bit and ignores writes.	R/O	1

The Devices in Package Register is described in Table 45.

Table 45: **Devices in Package (Register 3.5 and 3.6)**

Bit(s)	Name	Description	Attributes	Default Value
3.6.15	Vendor specific device present	The block always returns “0” for this bit.	R/O	0
3.6.14:0	Reserved	The block always returns “0” for these bits.	R/O	All “0s”
3.6.15:6	Reserved	The block always returns “0” for these bits.	R/O	All “0s”
3.5.5	DTE XS Present	The block always returns “0” for this bit.	R/O	0
3.5.4	PHY XS Present	The block always returns “0” for this bit.	R/O	0
3.5.3	PCS Present	The block always returns “1” for this bit.	R/O	1
3.5.2	WIS Present	The block always returns “0” for this bit.	R/O	0
3.5.1	PMA/PMD Present	The block always returns “1” for this bit.	R/O	1
3.5.0	Clause 22 device present	The block always returns “0” for this bit.	R/O	0

The 10G PCS Control Register 2 is described in Table 46.

Table 46: **10G PCS Control Register 2 (Register 3.7)**

Bit(s)	Name	Description	Attributes	Default Value
3.7.15:2	Reserved	The block always returns “0” for these bits and ignores writes.	R/O	All “0s”
3.7.1:0	PCS Type Selection	The block always returns “01” for these bits and ignores writes.	R/O	“01”

The 10G PCS Status Register 2 is described in Table 47.

Table 47: **10G PCS Status Register 2 (Register 3.8)**

Bit(s)	Name	Description	Attributes	Default Value
3.8.15:14	Device present	The block always returns “10.”	R/O	“10”
3.8.13:12	Reserved	The block always returns “0” for these bits.	R/O	All “0s”
3.8.11	Transmit Local Fault	1 = Fault condition on transmit path 0 = No fault condition on transmit path	R/O Latching high	-

Table 47: **10G PCS Status Register 2 (Register 3.8) *(Continued)***

Bit(s)	Name	Description	Attributes	Default Value
3.8.10	Receive local fault	1 = Fault condition on receive path 0 = No fault condition on receive path	R/O Latching high	-
3.8.9:3	Reserved	The block always returns “0” for these bits.	R/O	All “0s”
3.8.2	10GBASE-W Capable	The block always returns “0” for this bit.	R/O	0
3.8.1	10GBASE-X Capable	The block always returns “1” for this bit.	R/O	1
3.8.0	10GBASE-R Capable	The block always returns “0” for this bit.	R/O	0

The Package Identifier register is described in Table 48.

Table 48: **Package Identifier (Registers 3.14 and 3.15)**

Bit(s)	Name	Description	Attributes	Default Value
3.14.15:0	Package Identifier	The block always returns “0” for these bits.	R/O	All “0s”
3.15.15:0	Package Identifier	The block always returns “0” for these bits.	R/O	All “0s”

The 10GBASE-X Status Register is described in Table 49.

Table 49: **10GBASE-X Status Register (Register 3.24)**

Bit(s)	Name	Description	Attributes	Default Value
3.24.15:13	Reserved	The block always returns “0” for these bits.	R/O	All “0s”
3.24.12	10GBASE-X Lane Alignment Status	1 = 10GBASE-X receive lanes aligned; 0 = 10GBASE-X receive lanes not aligned.	RO	-
3.24.11	Pattern testing ability	The block always returns “1” for this bit.	R/O	1
3.24.10:4	Reserved	The block always returns “0” for these bits.	R/O	All “0s”
3.24.3	Lane 3 Sync	1 = Lane 3 is synchronized; 0 = Lane 3 is not synchronized.	R/O	-
3.24.2	Lane 2 Sync	1 = Lane 2 is synchronized; 0 = Lane 2 is not synchronized	R/O	-
3.24.1	Lane 1 Sync	1 = Lane 1 is synchronized; 0 = Lane 1 is not synchronized.	R/O	-
3.24.0	Lane 0 Sync	1 = Lane 0 is synchronized; 0 = Lane 0 is not synchronized.	R/O	-

The 10GBASE-X Test Control Register is described in Table 50.

Table 50: **10GBASE-X Test Control register (Register 5.25)**

Bit(s)	Name	Description	Attributes	Default Value
3.25.15:3	Reserved	The block always returns “0” for these bits.	R/O	All “0s”
3.25.2	Transmit test pattern enable	1 = Transmit test pattern enable 0 = Transmit test pattern disabled	R/W	0
3.25.1:0	Test pattern select	11 = reserved 10 = mixed frequency test pattern 01 = low frequency test pattern 00 = high frequency test pattern	R/W	“00”

MDIO Interface

The MDIO interface pins (MDC, MDIO_IN, MDIO_OUT, MDIO_TRI) are brought out of the core separately for maximum flexibility. They can be:

- connected to an IOBUF to drive an external tristate bus
- connected through individual IBUFs and OBUFs to a level shifter to create a fully compliant Clause 45 MDIO interface
- connected to an internal SoC management interface

References

- IEEE P802.3ae D4.1 draft specification
- IEEE 802.3-2000
- *Virtex-II User Guide*
- *Virtex-II Pro User Guide*

Optional Blocks

Xilinx can deliver instances of the core with the optional functional blocks left out. This can significantly reduce logic consumption in lightweight applications.

The optional blocks are:

- Statistical Counters included or excluded from the netlist
- XGMII or XAUI interface to the PHY

Table 51 provides some indication of the resource savings that can be made. Note that these numbers are approximate and will depend to some extent on the customer design.

Table 51: **Optional blocks - approximate resource usage**

Optional block	XGMII	XAUI
Statistics Included	3750 slices	4400 slices
Statistics Excluded	3000 slices	3700 slices

Please contact Xilinx for more information on these configurations.

Related Information

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