T-46-13-29

Microchip

27C512

512K (64K x 8) CMOS UV Erasable PROM

FEATURES

- High speed performance
  - —120ns access time available
- CMOS Technology for low power consumption
  - —40mA Active current
  - —100μA Standby current
- OTP (one-time-programming) available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Two programming algorithms allow improved programming times
  - —Fast programming
  - —Rapid-pulse programming
- Organized 64K x 8: JEDEC standard pinouts
  - —28-pin Dual-in-line package
  - —32-pin Chip carrier (leadless or plastic)
- Available for extended temperature ranges:
  - —Commercial: 0° C to 70° C
  - —Industrial: -40° C to 85° C
  - —Military** (B): -55° C to 125° C

DESCRIPTION

The Microchip Technology Inc 27C512 is a CMOS 512K bit (ultraviolet light) Erasable (electrically) Programmable Read Only Memory. The device is organized into 64K words by 8 bits (64K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 120ns. This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are requirements.

A complete family of packages is offered to provide the most flexability in applications. One-time-programming (OTP) is available for low cost (plastic) applications.

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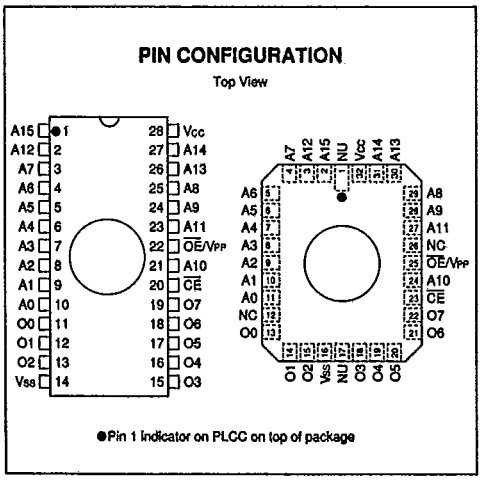

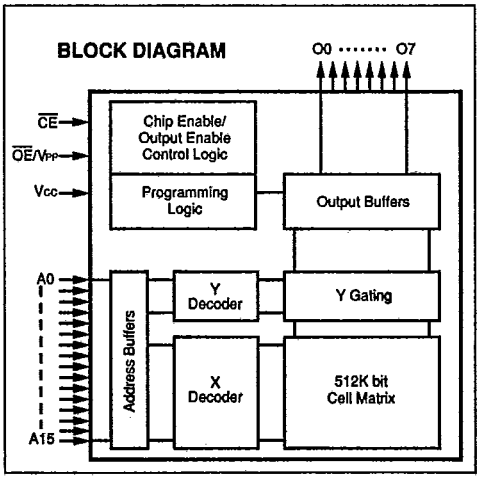

**See 27C512 Military Data Sheet DS60014

PIN FUNCTION TABLE	
Name	**Function**
A0 - A15	Address Inputs
CE	Chip Enable
OE/VPP	Output Enable/ Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection
NU	Not Used

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

VCC and input voltages w.r.t. VSS .....-0.6V to +7.25V
VPP voltage w.r.t. VSS during programming .....-0.6V to +14.0V
Voltage on A9 w.r.t. VSS .....-0.6V to +13.5V
Output voltage w.r.t. VSS .....-0.6V to VCC + 1.0V
Storage temperature .....-65° C to 150° C
Ambient temp. with power applied .....-65° C to 125° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial: Tamb= 0° C to 70° C
Industrial: Tamb= -40° C to 85° C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN = 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400µA IOL = 2.1mA
Output Leakage	all		ILO	-10	10	µA	VOUT = 0V to VCC
Input Capacitance	all		CIN		6	pF	VIN = 0V; Tamb = 25° C; f = 1MHz
Output Capacitance	all		COUT		12	pF	VOUT = 0V; Tamb= 25° C; f = 1MHz
Power Suppy Current, Active	S X	TTL input TTL input	ICC ICC		40 50	mA mA	VCC = 5.5V f = 1MHz; $\overline{OE}$/VPP= $\overline{CE}$ = VIL; Iout = 0mA; VIL = -0.1 to 0.8 V; VIH = 2.0 to VCC;
Power Supply Current, Standby	S X S	TTL input TTL input CMOS input	ICC(S)TTL ICC(S)TTL ICC(S)CMOS		2 3 100	mA mA µA	 $\overline{CE}$ = VCC ±0.2V

* Parts: S = Standard Power; X = Industrial Temp Range;
Notes: (1) AC Power component above 1MHz: 2mA/MHz.

READ OPERATION AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0 V and V_{OL} = 0.8V
Output Load: 1 TTL Load + 100pF
Input Rise and Fall Times: 10nsec
Ambient Temperature: Commercial: Tamb = 0° C to 70° C
Industrial: Tamb = -40° C to 85° C

Parameter	Sym	27C512-12*		27C512-15		27C512-17		27C512-20		27C512-25		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}		120		150		170		200		250	ns	$\overline{CE}$ = $\overline{OE}/V_{PP}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}		120		150		170		200		250	ns	$\overline{OE}/V_{PP}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}		65		70		70		75		100	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ to Output High Impedance	t_{OFF}	0	50	0	50	0	50	0	55	0	60	ns	
Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$, whichever occured first	t_{OH}	0		0		0		0		0		ns	

*27C512-12 is only available in commercial temperature range

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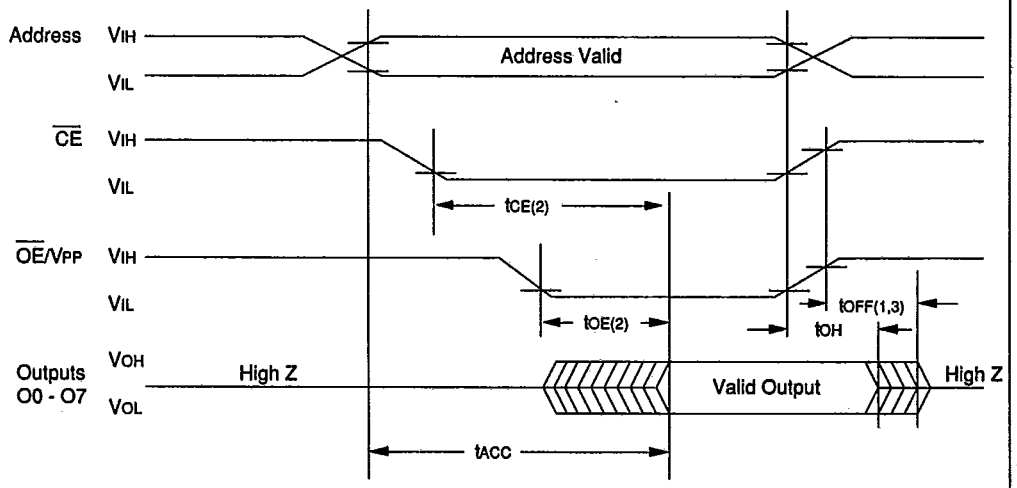
READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}/V_{PP}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

PROGRAMMING
DC Characteristics

Ambient Temperature: Tamb = 25° C±5° C
For $\overline{OE}$/VPP and VCC Voltages refer to Programming Algorithms

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage		ILI	-10	10	µA	VIN = VIL or VIH
Output Voltages	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400µA IOL = 2.1mA
VCC Current, program & verify		ICC2		40	mA	
$\overline{OE}$/VPP Current,program		IPP2		25	mA	$\overline{CE}$ = VIL
A9 Product Identification		VH	11.5	12.5	V	

Note: (1) VCC must be applied simultaneously or before the VPP voltage on $\overline{OE}$/VPP and removed simultaneously or after the VPP voltage on $\overline{OE}$/VPP.

PROGRAMMING
AC Characteristics
for Program, Program Verify and Program Inhibit Modes

AC Testing Waveform: VIH = 2.4V and VIL = 0.45V; VOH = 2.0V; VOL = 0.8V
Output Load: 1 TTL Load + 100pF
Ambient Temperature: 25° C ±5° C
For $\overline{OE}$/VPP and VCC Voltages, refer to Programming Algorithms

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	tAS	2		µs	
Data Set-Up Time	tDS	2		µs	
Data Hold Time	tDH	2		µs	
Address Hold Time	tAH	0		µs	
Float Delay (3)	tDF	0	130	ns	
VCC Set-Up Time	tVCS	2		µs	
Program Pulse Width (1)	tPW	95	105	µs	100µs typical
Program Pulse Width (1)	tPW	.95	1.05	ms	1ms typical
$\overline{CE}$ Set-Up Time	tCES	2		µs	
$\overline{OE}$ Set-Up Time	tOES	2		µs	
$\overline{OE}$ Hold Time	tOEH	2		µs	
$\overline{OE}$ Recovery Time	tOR	2		µs	
$\overline{CE}$ Overprogram Pulse Width (2)	tOPW	2.85	78.75	ms	
$\overline{OE}$/VPP Rise Time During Programming	tPRT	50		ns	

Notes: (1) For rapid-pulse programming algorithm, initial programming width tolerance is 100µsec ±5%. For fast programming algorithm, initial program pulse width tolerance is 1msec ± 5%.
(2) For fast programming algorithm, the length of the overprogram pulse may vary from 2.85 to 78.75msec as a function of the iteration counter value.
(3) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

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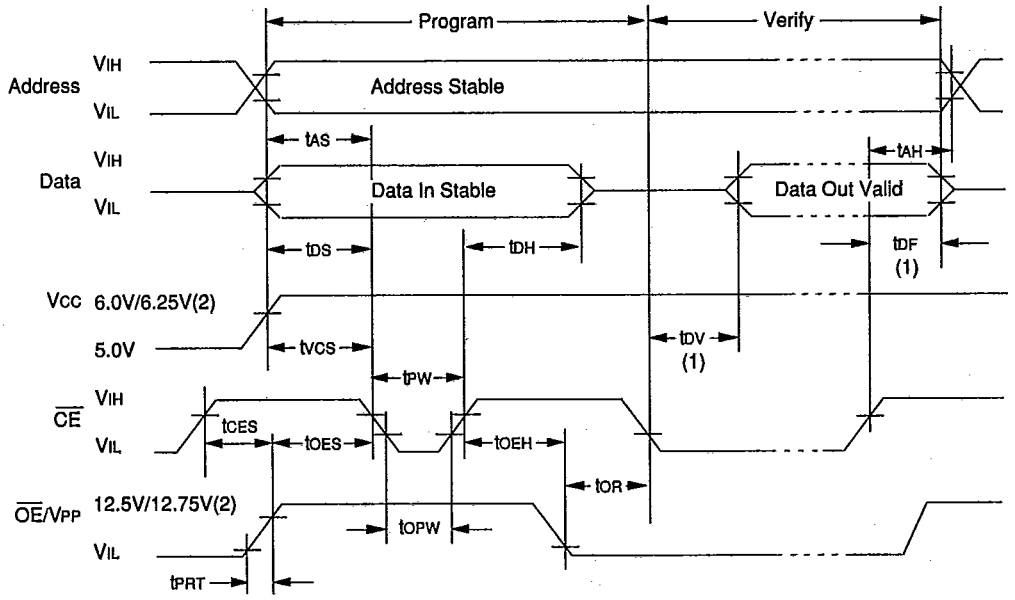
PROGRAMMING Waveforms



Notes: (1) t_{DF} and t_{OE} are characteristics of the device but must be accommodated by the programmer
(2) V_{CC} = 6.0V ±0.25 V, V_{PP} = V_H = 12.5V ±0.5 V for fast programming algorithm
V_{CC} = 6.25V ±0.25 V, V_{PP} = V_H = 12.75V ±0.25 V for rapid pulse programming algorithm

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MODES

Operation Mode	$\overline{CE}$	$\overline{OE}/V_{PP}$	A9	O0 - O7
Read	V_{IL}	V_{IL}	X	D_{OUT}
Program	V_{IL}	V_H	X	D_{IN}
Program Verify	V_{IL}	V_{IL}	X	D_{OUT}
Program Inhibit	V_{IH}	V_H	X	High Z
Standby	V_{IH}	X	X	High Z
Output Disable	V_{IL}	V_{IH}	X	High Z
Identity	V_{IL}	V_{IL}	V_H	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip

b) the $\overline{OE}/V_{PP}$ pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is transferred to the output after a delay (t_{OE}) from the falling edge of $\overline{OE}/V_{PP}$.

Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high and a program mode is not identified.

When this condition is met, the supply current will drop from 40mA to 100µA.

Output Enable $\overline{OE}$/VPP

This multifunction pin eliminates bus connection in multiple bus microprcessor systems and the outputs go to high impedance when:

• the $\overline{OE}$/VPP pin is high (VIH).

When a VH input is applied to this pin, it supplies the programming voltage (VPP) to the device.

Erase Mode

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1"s state as a result of being exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm² is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000µW/cm² for 20 minutes.

Programming Mode

Two programming algorithms are available. The fast programming algorithm is the industry-standard programming mode that requires both initial programming pulses and overprogramming pulses. The fast programming algorithm is recommended for windowed product only. A flowchart of the fast programming algorithm is shown in Figure 1.

The rapid-pulse programming algorithm has been developed to improve on the programming throughput times in a production environment. Up to 25 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the rapid-pulse programming algorithm is shown in Figure 2.

Rapid-pulse is the preferred programming algorithm.

Programming takes place when:

a) VCC is brought to the proper voltage,
b) $\overline{OE}$/VPP is brought to the proper VH level

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0 - A15 and the data to be programmed is presented to pins O0 - O7. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) VCC is at the proper level,
c) the $\overline{OE}$/VPP pin is low, and
d) the $\overline{CE}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ needs to be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed; all other devices with $\overline{CE}$ held high will not be programmed with the data (although address and data will be available on their input pins).

Identity Mode

In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc and the device type. This mode is entered when Pin A9 is taken to VH (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$/VPP lines must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	VIL	0	0	1	0	1	0	0	1	29
Device Type*	VIH	0	0	0	0	1	0	1	1	0D

* Code subject to change.

FIGURE 1 - PROGRAMMING FAST ALGORITHMS

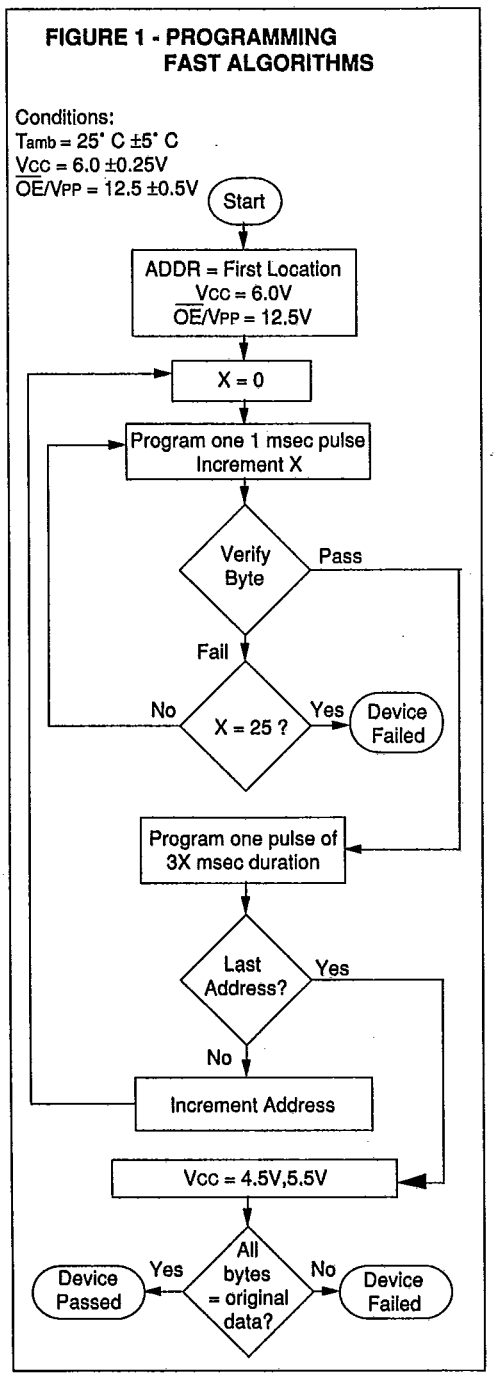
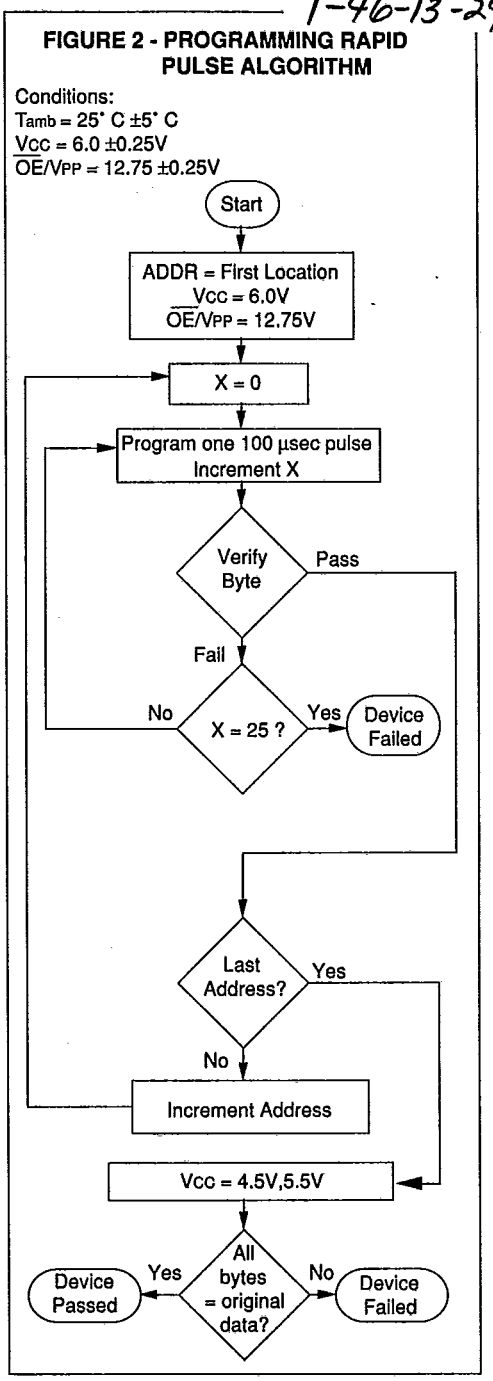


FIGURE 2 - PROGRAMMING RAPID PULSE ALGORITHM



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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27C512 - 25 I / P

Package:	J	Cerdip
	K	Ceramic Leadless Chip Carrier
	L	Plastic Leaded Chip Carrier (OTP Available)
	P	Plastic DIP (OTP Available)
	SO	SOIC 28 Pin
Temperature Range:	-	0° C to 70° C
	I	-40° C to 85° C
Access Time:	12	120 nsec
	15	150 nsec
	17	170 nsec
	20	200 nsec
	25	250 nsec
Device	27C512	512K (64K x 8) CMOS EPROM