512Kx32 3.3V SRAM MODULE *ADVANCED**

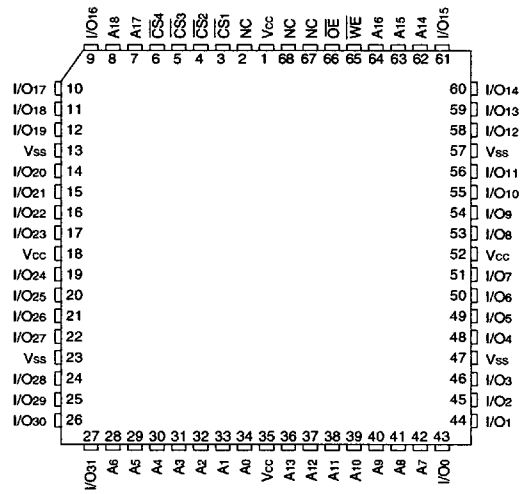
FEATURES

- Access Times of 15, 17, 20ns
- Low Voltage Operation:
  - 3.3V ±10% Power Supply
- Packaging
  - 68-lead, JLCC/PLCC, (Package 701)
- Organized as 512Kx32; User Configurable as 1Mx16 or 2Mx8
- BiCMOS:
  - Radiation Tolerant with Epitaxial Layer Die
- Commercial Temperature Range
- TTL Compatible Inputs and Outputs
- Fully Static Operation:
  - No Clock or Refresh Required
- Three State Output
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation

* *This data sheet describes a product under development and is subject to change or cancellation without notice.*

PIN CONFIGURATION FOR WS512K32BV-XCJCE

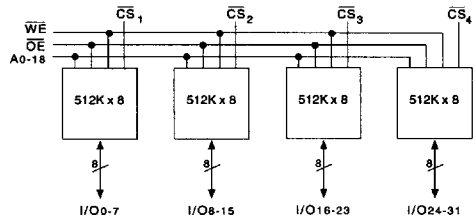
TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$1-4	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	0	+70	°C
Storage Temperature	T_{STG}	-45	+85	°C
Signal Voltage Relative to GND	V_G	-0.5	4.6	V
Supply Voltage	V_{CC}	-0.5	4.6	V

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V

CAPACITANCE

(@ T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
$\overline{OE}$ Capacitance	C_{OE}	V_{IN} = 0V, f = 1.0MHz	50	pF
Write Enable Capacitance	C_{WE}	V_{IN} = 0V, f = 1.0MHz	50	pF
$\overline{CS}_{1-4}$ Capacitance	C_{CS}	V_{IN} = 0V, f = 1.0MHz	20	pF
Data I/O Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1.0MHz	20	pF
Address Input Capacitance	C_{AD}	V_{IN} = 0V, f = 1.0MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 3.3V ±0.3V, V_{SS} = 0V, T_A = 0°C to +70°C)

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current (x 32 Mode)	I_{CC} x 32	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 3.6V		480	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 3.6V		60	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

AC CHARACTERISTICS
(V_{CC} = 3.3V, T_A = 0°C to +70°C)

Parameter	Symbol	-15		-17		-20		Units
Read Cycle		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		17		20		ns
Address Access Time	t_{AA}		15		17		20	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns
Chip Select Access Time	t_{ACS}		15		17		20	ns
Output Enable to Output Valid	t_{OE}		7		8		10	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	2		2		2		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		7		8		10	ns
Output Disable to Output in High Z	t_{OHZ}[1]		7		8		10	ns

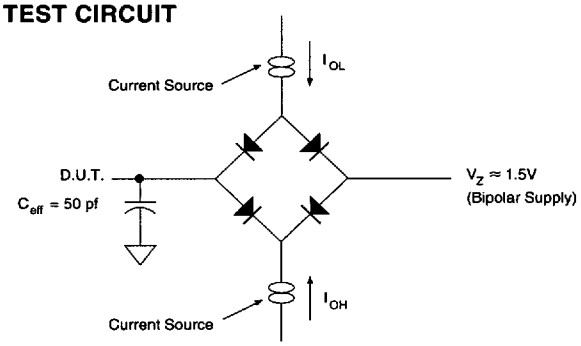
1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS
(V_{CC} = 3.3V, T_A = 0°C to +70°C)

Parameter	Symbol	-15		-17		-20		Units
Write Cycle		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		17		20		ns
Chip Select to End of Write	t_{CW}	10		12		14		ns
Address Valid to End of Write	t_{AW}	10		12		14		ns
Data Valid to End of Write	t_{DW}	8		9		10		ns
Write Pulse Width	t_{WP}	12		14		14		ns
Address Setup Time	t_{AS}	0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		ns
Output Active from End of Write	t_{OW}[1]	2		3		3		ns
Write Enable to Output in High Z	t_{WHZ}[1]		8		8		9	ns
Data Hold Time	t_{DH}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT

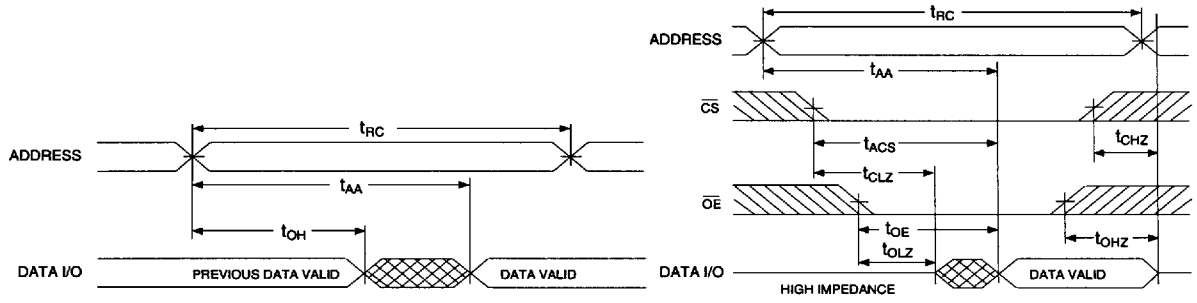


AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_O = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

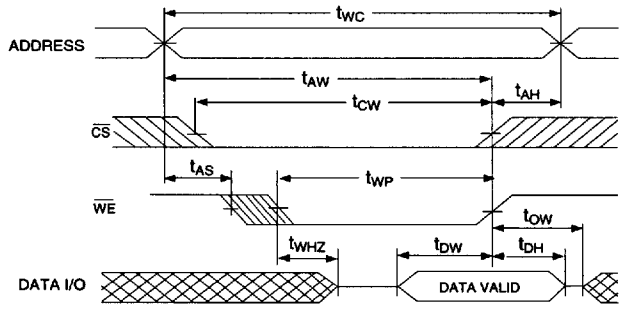
TIMING WAVEFORM - READ CYCLE



READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})

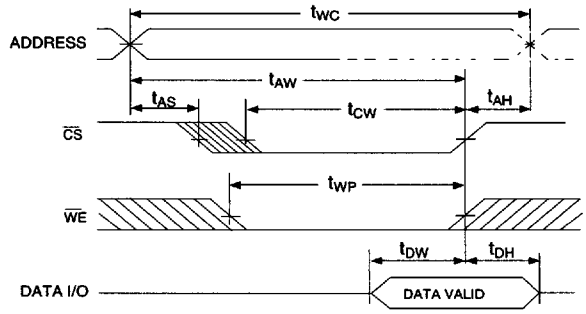
READ CYCLE 2 ($\overline{WE}$ = V_{IH})

WRITE CYCLE - $\overline{WE}$ CONTROLLED



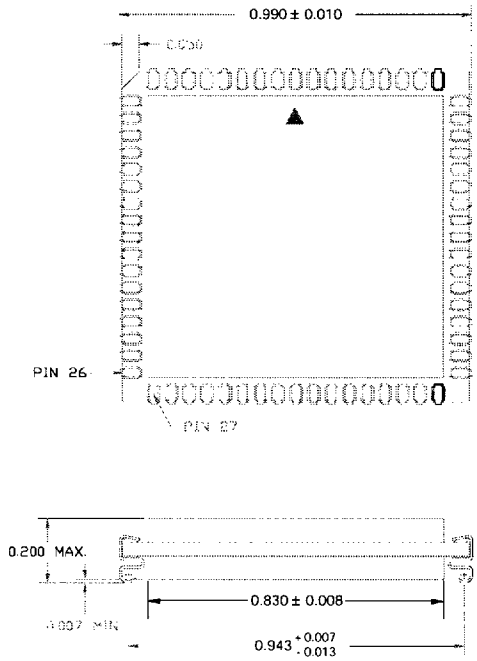
WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

WRITE CYCLE - $\overline{CS}$ CONTROLLED



WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

PACKAGE 701: 68 LEAD JLCC



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION