

H3S -

TOSHIBA
4Mbit Static RAM
TC55V4000ST
Data Sheet

**TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS
524,288-WORD BY 8-BIT STATIC RAM**

DESCRIPTION

The TC55V4000ST is a 4,194,304-bit static random access memory (SRAM) organized as 524,288 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 2.3 to 3.6 V power supply. Advanced circuit technology provides both high speed and low power at an operating current of 3 mA/MHz and a minimum cycle time of 70 ns. It is automatically placed in low-power mode at 0.5 μ A standby current ($V_{DD}=3V$, $T_a=25^\circ C$) when chip enable (\overline{CE}) is asserted high. There are two control inputs. \overline{CE} and $\overline{CE2}$ are used to select the device and for data retention control, and output enable (\overline{OE}) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. The TC55V4000ST is available in a normal pinout plastic 32-pin thin-small-outline package (TSOP).

FEATURES

- Low-power dissipation
Operating: 10.8 mW/MHz (typical)
- Single power supply voltage of 2.3 to 3.6 V
- Power down features using \overline{CE}
- Data retention supply voltage of 1.5 to 3.6 V
- Direct TTL compatibility for all inputs and outputs
- Standby current (maximum)

3.6V	7 μ A
3.0V	5 μ A

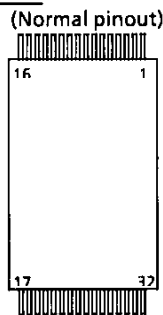
- Access Times (maximum):

	TC55V4000ST	
	-70	-85
Access Time	70ns	85ns
$\overline{CE1}$ Access Time	70ns	85ns
\overline{OE} Access Time	35ns	45ns

- Packages:
TSOP I 32-P-0.50 (Weight: g typ)

PIN ASSIGNMENT (TOP VIEW)

o 32 PIN TSOP



PIN NAMES

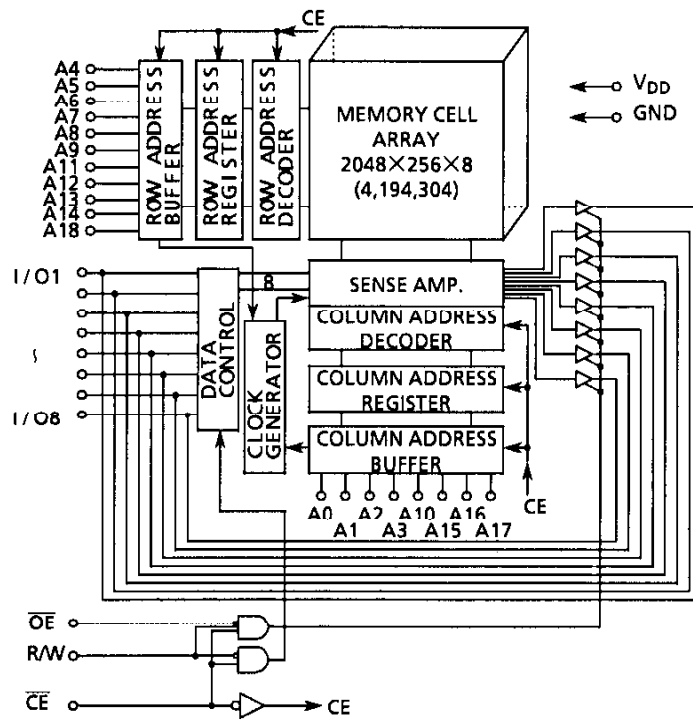
A0 to A18	Address Inputs
R/W	Read / Write Control Input
\overline{OE}	Output Enable Input
\overline{CE}	Chip Enable Input
I/O1 to I/O8	Data Input / Output
V_{DD}	Power
GND	Ground

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PIN NAME	A ₁₁	A ₉	A ₈	A ₁₃	R/W	A ₁₇	A ₁₅	V _{DD}	A ₁₈	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
PIN NO.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
PIN NAME	A ₃	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	\overline{CE}	A ₁₀	\overline{OE}

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BLOCK DIAGRAM



OPERATION MODE

MODE	\overline{CE}	\overline{OE}	R/W	I/O1 to I/O8	POWER
Read	L	L	H	D _{OUT}	I _{DDO}
Write	L	X	L	D _{IN}	I _{DDO}
Outputs Disabled	L	H	H	High-Z	I _{DDO}
Standby	H	X	X	High-Z	I _{DDs}
	X	X	X	High Z	I _{DDs}

Note: X = don't care. H = logic high. L = logic low.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V _{DD}	Power Supply Voltage	- 0.3 to 4.6	V
V _{IN}	Input Voltage	- 0.3 to 4.6	V
V _{IO}	Input/Output Voltage	- 0.5 to V _{DD} + 0.5	V
P _D	Power Dissipation	0.8	W
T _{solder}	Soldering Temperature (10 s)	260	°C
T _{strg.}	Storage Temperature	- 55 to 150	°C
T _{opr.}	Operating Temperature	- 40 to 85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta = -40° to 85°C)

SYMBOL	PARAMETER	2.3 to 3.6V			2.7 to 3.6V			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V _{DD}	Power Supply Voltage	2.3	3.0	3.6	2.7	3.0	3.6	V
V _{IH}	Input High Voltage	V _{DD} -0.2	-	V _{DD} +0.3	2.2	-	V _{DD} +0.3	V
V _{IL}	Input Low Voltage	-0.3	-	0.2	-0.3	-	0.6	V
V _{DH}	Data Retention Supply Voltage	1.5	-	3.6	1.5	-	3.6	V

DC CHARACTERISTICS (Ta = -40° to 85°C, V_{DD} = 2.7 to 3.6 V)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT			
I _{IL}	Input Leakage Current	V _{IN} = 0 V to V _{DD}	-	-	± 1.0	μA			
I _{OH}	Output High Current	V _{OH} = V _{DD} - 0.5 V	-0.5	-	-	mA			
I _{OL}	Output Low Current	V _{OL} = 0.4 V	2.1	-	-	mA			
I _{IO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or R/W = V _{IL} or $\overline{OE} = V_{IH}$, V _{OUT} = 0 V to V _{DD}	-	-	± 1.0	μA			
I _{DDO1}	Operating Current	$\overline{CE} = V_{IL}$ and R/W = V _{IH} , I _{OUT} = 0 mA Other Input = V _{IH} /V _{IL}	V _{DD} = 3.0V±10%	Tcycle	min	-	-	35	mA
I _{DDO2}		$\overline{CE} = 0.2$ V R/W = V _{DD} - 0.2 V, I _{OUT} = 0 mA Other Inputs = V _{DD} - 0.2 V/0.2 V			1μs	-	-	10	
				min	-	-	30		
				1μs	-	-	5		
I _{DD51}		$\overline{CE} = V_{IH}$ or CE2 = V _{IL}			-	-	2	mA	
I _{DD52} (NOTE)	Standby Current	$\overline{CE} = V_{DD} - 0.2$ V V _{DD} = 2.0 to 3.6 V	V _{DD} = 3.0V±10%	Ta = 25°C	-	-	0.6	μA	
				Ta = -40~85°C	-	-	6		
			V _{DD} = 3.3V±0.3V	Ta = 25°C	-	-	0.7		
				Ta = -40~85°C	-	-	7		
			V _{DD} = 3.0V	Ta = 25°C	-	0.05	0.5		
				Ta = -40~40°C	-	-	1		
				Ta = -40~85°C	-	-	5		

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = GND	10	

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS ($T_a = -40^\circ$ to 85°C , $V_{DD} = 2.7$ to 3.6 V)

READ CYCLE

SYMBOL	PARAMETER	TC55V4000ST				UNIT
		-70		-85		
		MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	70	—	85	—	ns
t_{ACC}	Address Access Time	—	70	—	85	
t_{CO1}	Chip Enable ($\overline{CE1}$) Access Time	—	70	—	85	
t_{OE}	Output Enable Access Time	—	35	—	45	
t_{COE}	Chip Enable Low to Output Active	5	—	5	—	
t_{OEE}	Output Enable Low to Output Active	0	—	0	—	
t_{ON}	Chip Enable High to Output High-Z	—	30	—	35	
t_{ODO}	Output Enable High to Output High-Z	—	30	—	35	
t_{OH}	Output Data Hold Time	10	—	10	—	

WRITE CYCLE

SYMBOL	PARAMETER	TC55V4000ST				UNIT
		-70		-85		
		MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	70	—	85	—	ns
t_{WP}	Write Pulse Width	50	—	55	—	
t_{CW}	Chip Enable to End of Write	60	—	70	—	
t_{AS}	Address Setup Time	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	
t_{ODW}	R/W Low to Output High-Z	—	25	—	35	
t_{OEW}	R/W High to Output Active	0	—	0	—	
t_{DS}	Data Setup Time	30	—	35	—	
t_{DH}	Data Hold Time	0	—	0	—	

AC TEST CONDITIONS

Output load: 30 pF
 Input pulse level: 0.4 V, 2.4 V
 Timing measurements: 1.5 V
 Reference level: $V_{DD} \times 0.5$
 t_R, t_F : 5 ns

AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = -40° to 85°C, VDD = 2.3 to 3.6 V)

READ CYCLE

SYMBOL	PARAMETER	TC55V4000ST				UNIT
		-70		-85		
		MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	85	—	100	—	ns
t _{ACC}	Address Access Time	—	85	—	100	
t _{CO1}	Chip Enable (CE1) Access Time	—	85	—	100	
t _{OE}	Output Enable Access Time	—	45	—	50	
t _{COE}	Chip Enable Low to Output Active	5	—	5	—	
t _{OEE}	Output Enable Low to Output Active	0	—	0	—	
t _{OD}	Chip Enable High to Output High-Z	—	35	—	40	
t _{ODO}	Output Enable High to Output High-Z	—	35	—	40	
t _{OH}	Output Data Hold Time	10	—	10	—	

WRITE CYCLE

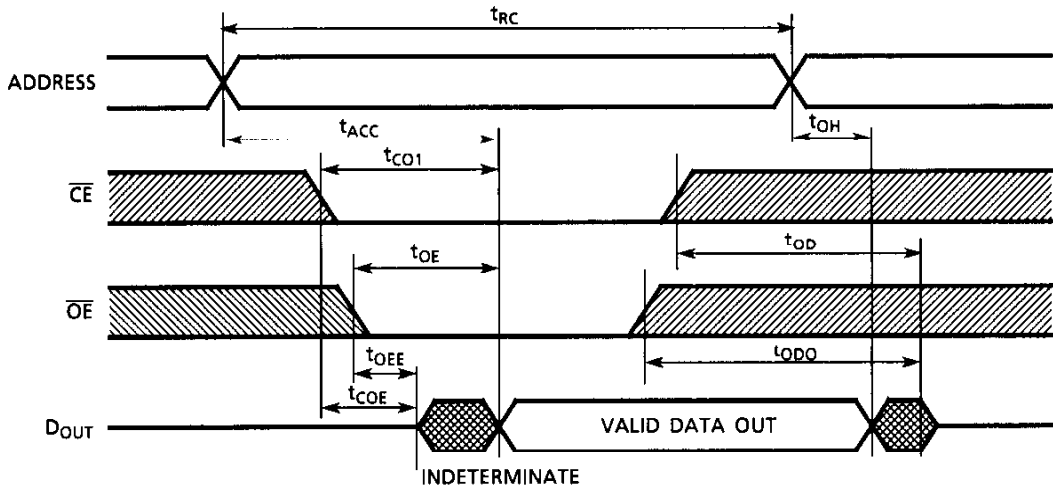
SYMBOL	PARAMETER	TC55V4000ST				UNIT
		-70		-85		
		MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time	85	—	100	—	ns
t _{WP}	Write Pulse Width	—	55	—	60	
t _{CW}	Chip Enable to End of Write	—	70	—	80	
t _{AS}	Address Setup Time	0	—	0	—	
t _{WR}	Write Recovery Time	0	—	0	—	
t _{ODW}	R/W Low to Output High-Z	—	35	—	40	
t _{OEW}	R/W High to Output Active	0	—	0	—	
t _{DS}	Data Setup Time	35	—	40	—	
t _{DH}	Data Hold Time	0	—	0	—	

AC TEST CONDITIONS

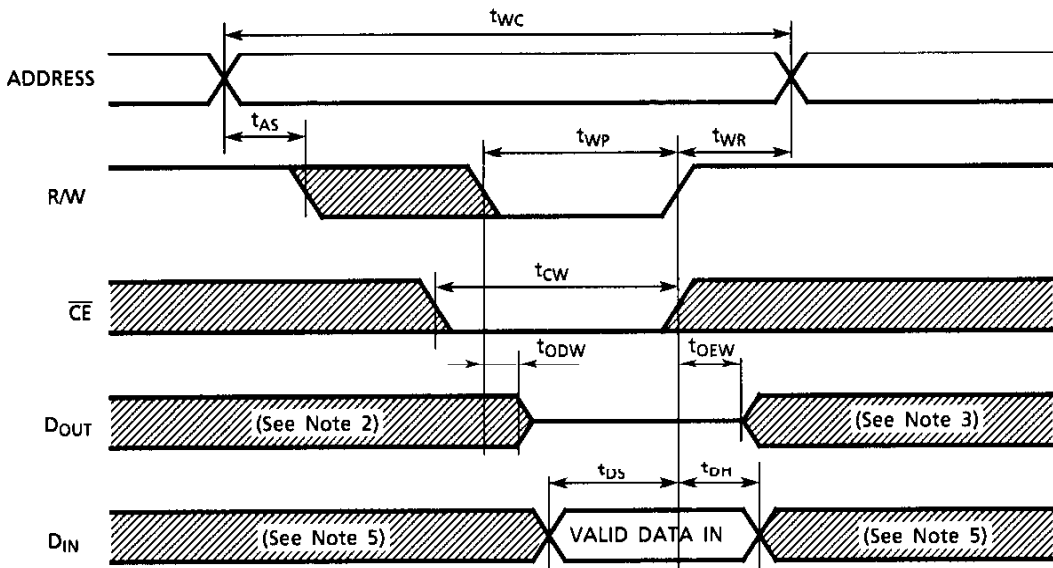
Output load: 30 pF
 Input pulse level: V_{DD} - 0.2V, 0.2V
 Timing measurements: V_{DD} × 0.5
 Reference level: V_{DD} × 0.5
 t_R, t_F: 5 ns

TIMING DIAGRAMS

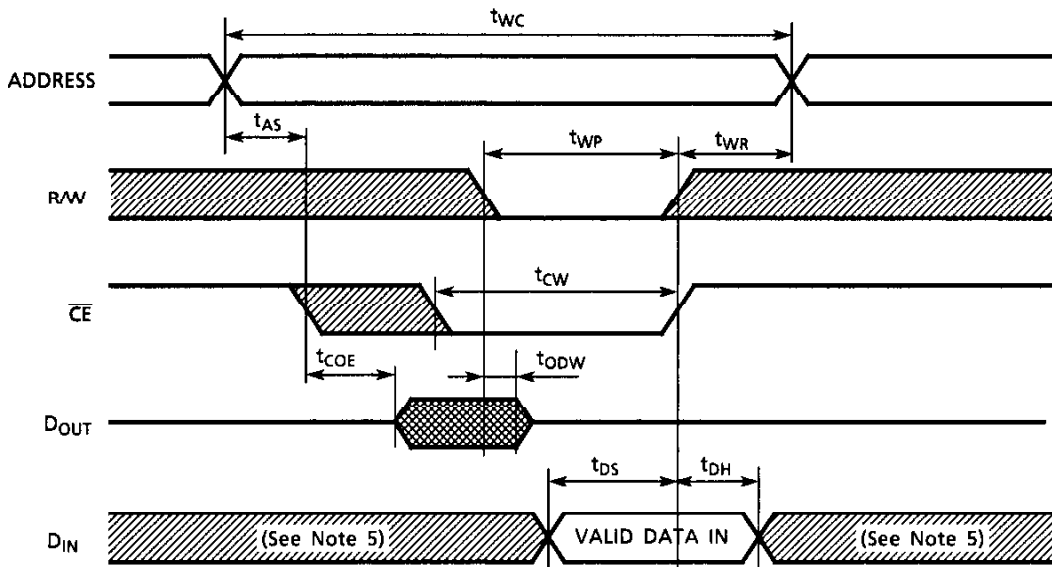
READ CYCLE (See Note 1)



WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



WRITE CYCLE 2 (\overline{CE} CONTROLLED) (See Note 4)



Note: (1) R/W remains HIGH for the read cycle.

(2) If \overline{CE} goes LOW coincident with or after R/W goes LOW, the outputs will remain at high impedance.

(3) If \overline{CE} goes HIGH coincident with or before R/W goes HIGH, the outputs will remain at high impedance.

(4) If \overline{OE} is HIGH during the write cycle, the outputs will remain at high impedance.

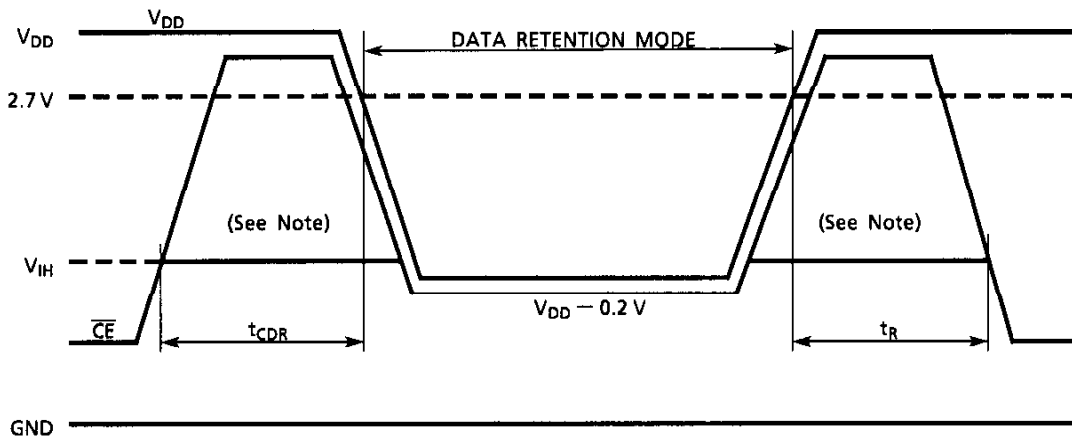
(5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = -40° to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	
V _{DH}	Data Retention Supply Voltage	1.5	—	3.6	V	
I _{DD52}	Standby Current	V _{DH} = 3.0V	Ta = -40 to 40°C	—	1	μA
			Ta = -40 to 85°C	—	5	
		V _{DH} = 3.6V	Ta = -40 to 85°C	—	7	
t _{CDR}	Chip Deselect to Data Retention Mode Time	0	—	—	nS	
t _R	Recovery Time	t _{RC} (1)	—	—	nS	

Note: (1) Read cycle time

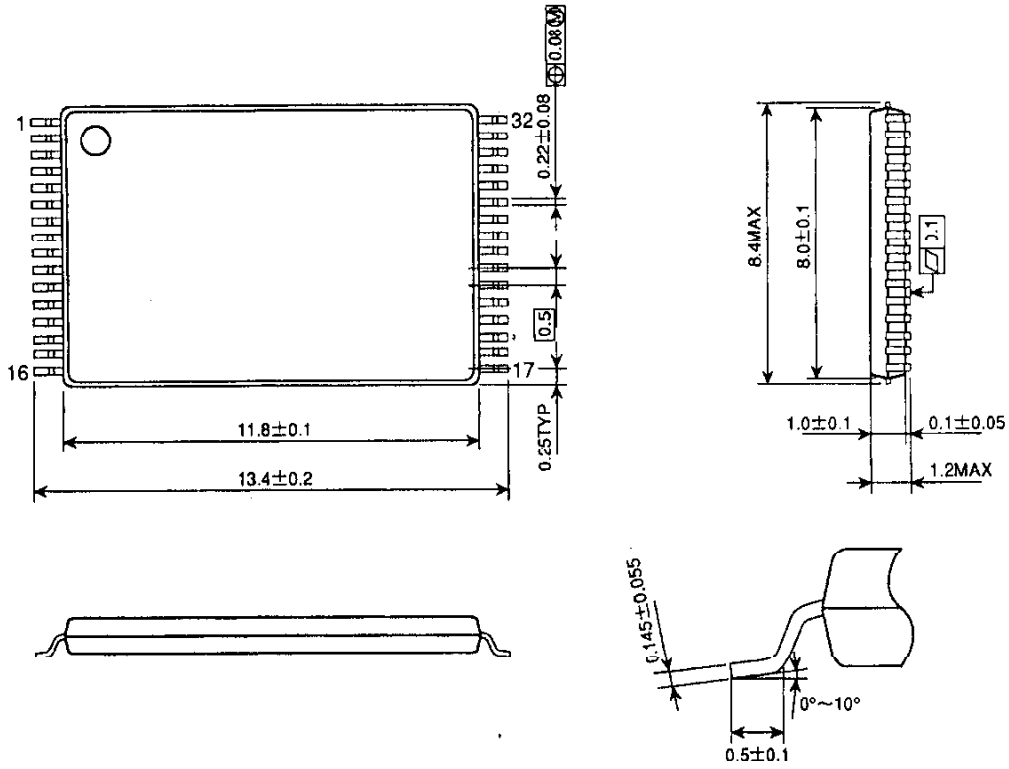
CE CONTROLLED DATA RETENTION MODE



Note: When \overline{CE} is operating at the V_{IH} level (2.2 V), the operating current is given by I_{DD51} during the transition of V_{DD} from 3.6 to 2.4 V.

PACKAGE DIMENSIONS (TSOP I 32-P-0.50)

Units in mm



Weight: g (typ)