DUAL FIBRE CHANNEL DEVICE S2102

FEATURES

- 1062 MHz (Fibre Channel) operating rate
  - Half rate operation
- Dual Transmitter with phase-locked loop (PLL) clock synthesis from low speed reference
- ANSI x3T11 Fibre Channel Compatible
- Dual Receiver PLL provides clock and data recovery
- Internally series terminated TTL outputs
- Low-jitter serial PECL interface
- Individual local loopback control
- JTAG 1149.1 Boundary scan on low speed I/O signals
- Interfaces with coax, twinax, or fiber optics
- Single +3.3V supply, 1.85 W power dissipation
- Compact 21mm x 21mm 156 TBGA package

APPLICATIONS

- Workstation
- Frame buffer
- Switched networks
- Data broadcast environments
- Proprietary extended backplanes

GENERAL DESCRIPTION

The S2102 facilitates high-speed serial transmission of data in a variety of applications including Fibre Channel, serial backplanes, and proprietary point to point links. The chip provides two separate transceivers which are operated individually for a data capacity of >2 Gbps.

Each bi-directional channel provides parallel to serial and serial to parallel conversion, clock generation/recovery, and framing. The on-chip transmit PLL synthesizes the high-speed clock from a low-speed reference. The on-chip dual receive PLL is used for clock recovery and data re-timing on the two independent data inputs. The transmitter and receiver each support differential PECL-compatible I/O for copper or fiber optic component interfaces with excellent signal integrity. Local loopback mode allows for system diagnostics. The chip requires a 3.3V power supply and dissipates 1.85 watts.

Figure 1 shows the S2102 and S2002 in a Fibre Channel application. Figure 2 summarizes the input/output signals of the device. Figures 3 and 4 show the transmit and receive block diagrams, respectively.

Figure 1. Typical Dual Fibre Channel Application

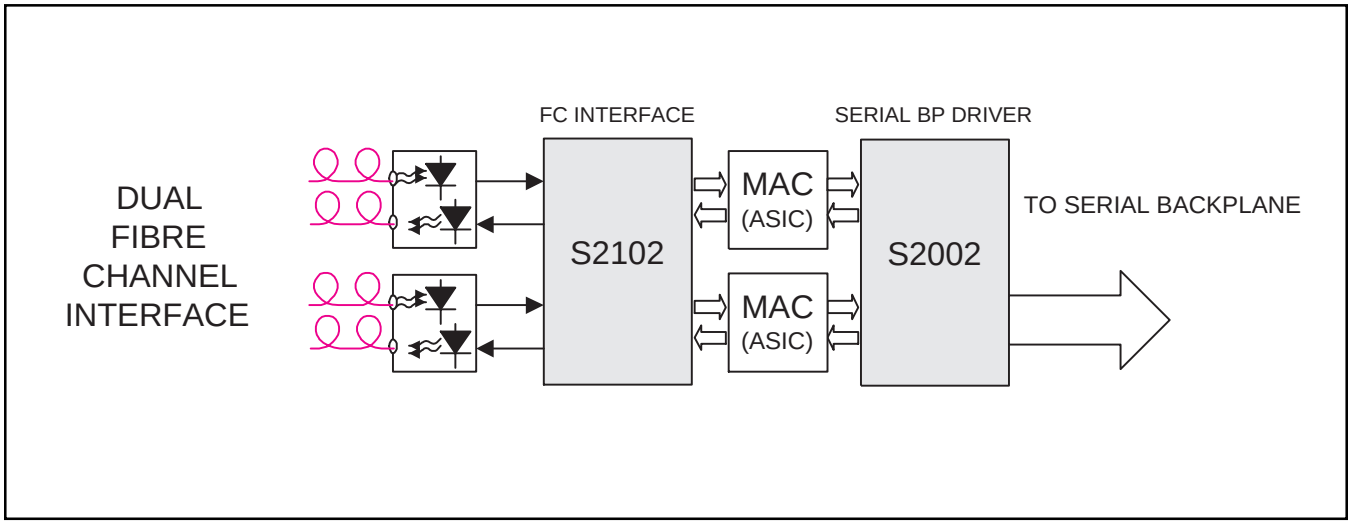


Figure 2. S2102 Input/Output Diagram

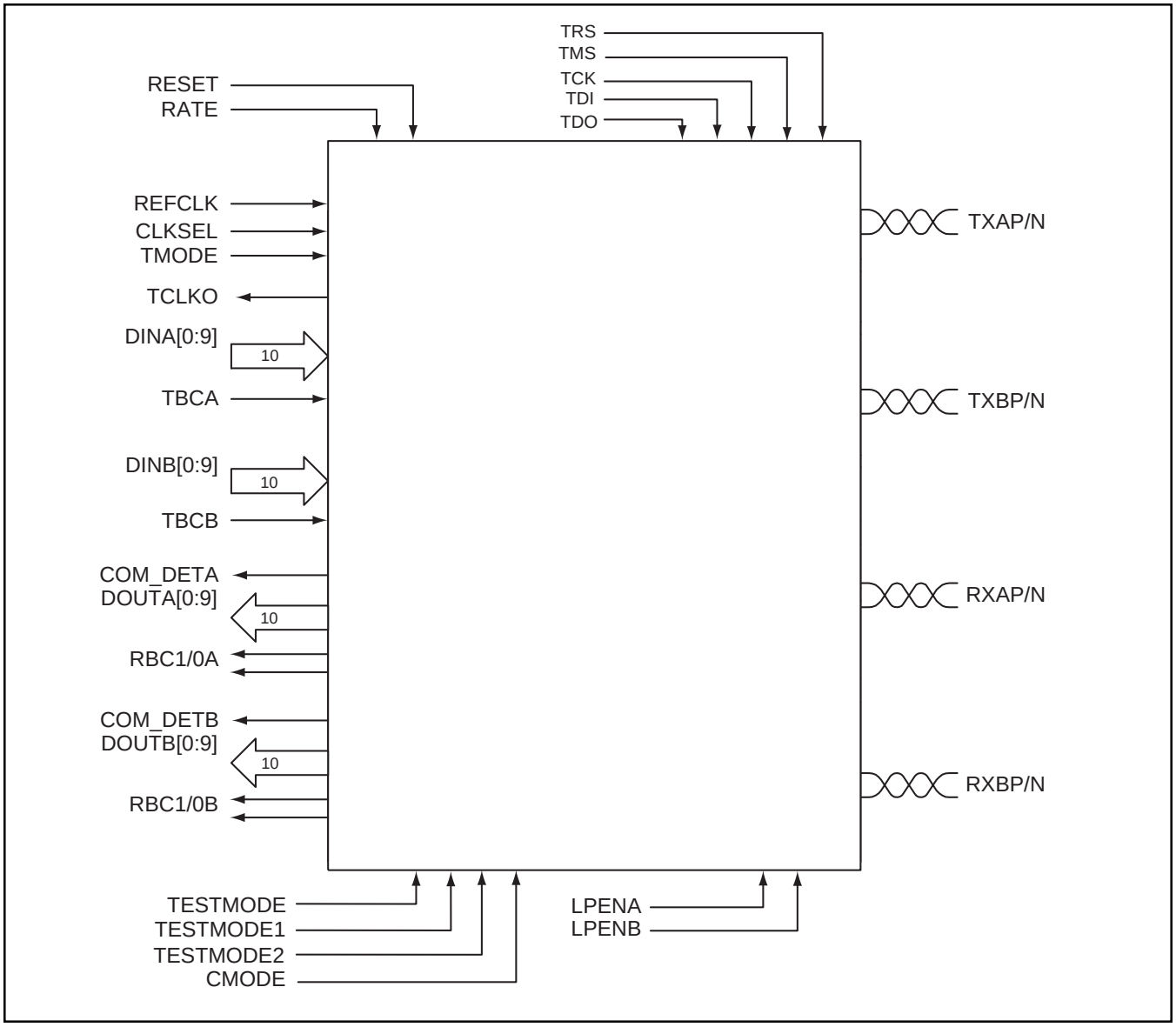


Figure 3. Transmitter Block Diagram

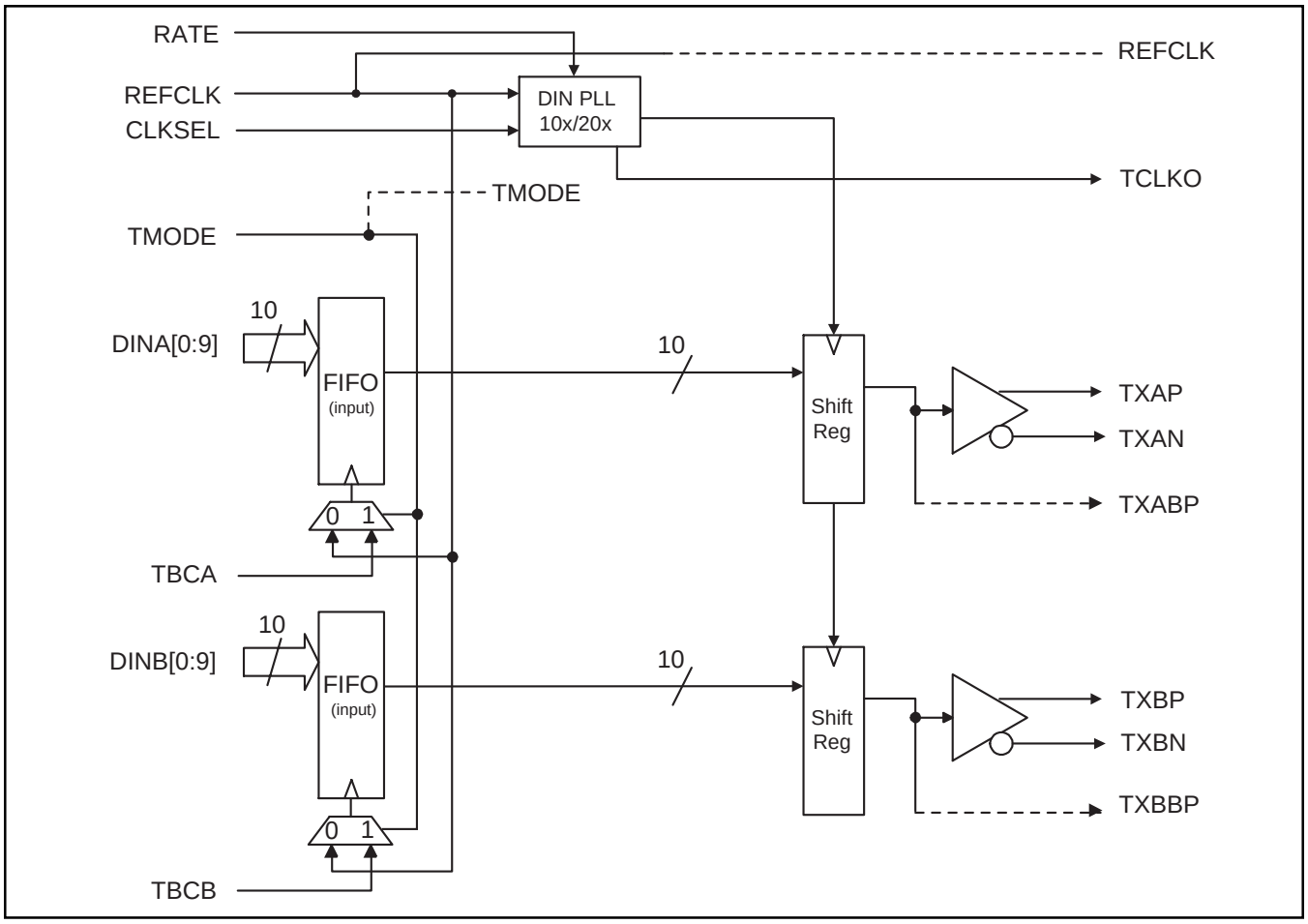
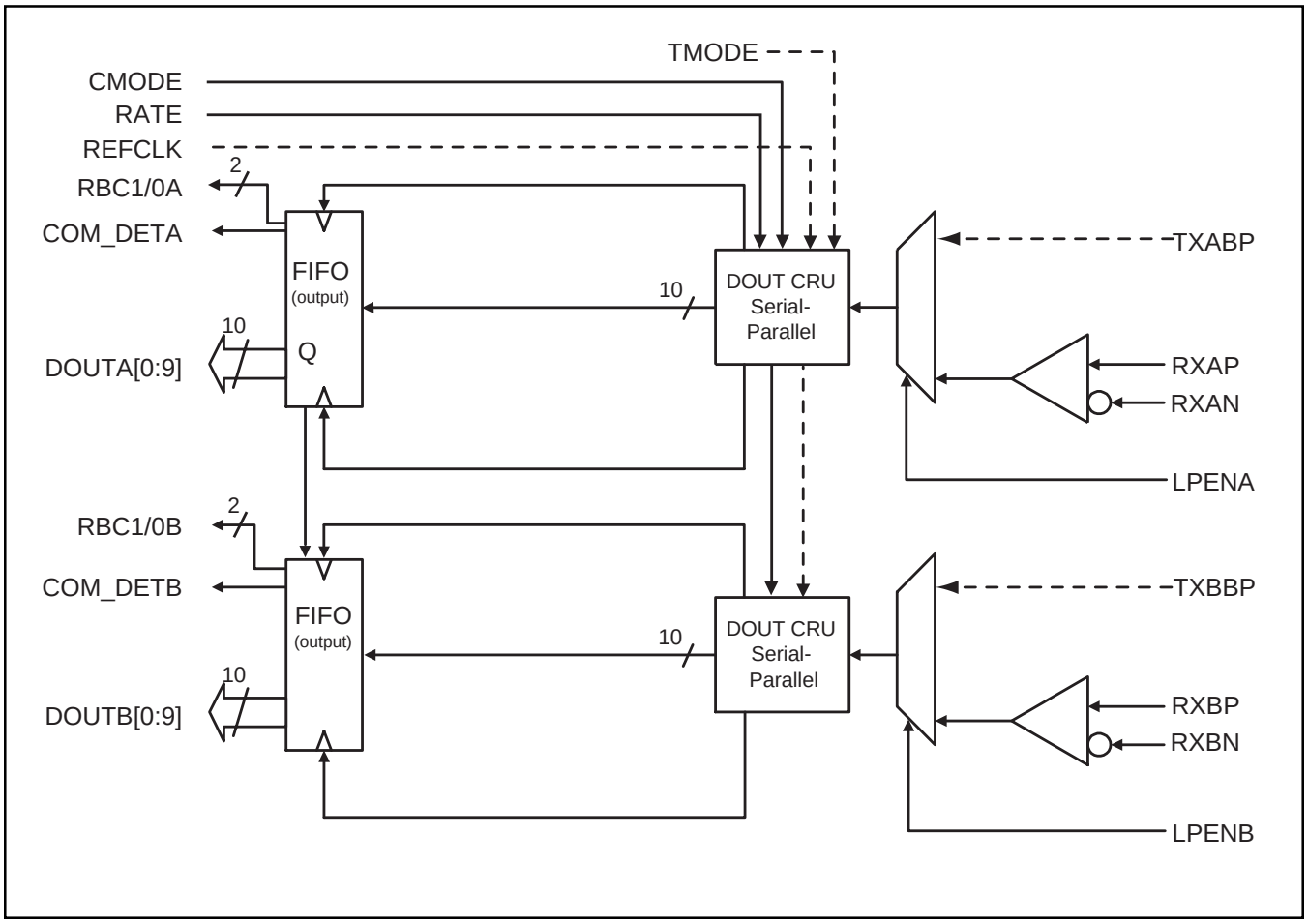


Figure 4. Receiver Block Diagram



TRANSMITTER DESCRIPTION

The transmitter section of the S2102 contains a single PLL which is used to generate the serial rate transmit clock for all transmitters. Two channels are provided with a variety of options regarding input clocking and loopback. The transmitters operate at 1.062 GHz, 10 or 20 times the reference clock frequency.

Data Input

The S2102 has been designed to simplify the parallel interface data transfer and provides the utmost in flexibility regarding clocking of parallel data. The S2102 incorporates a unique FIFO structure on both the parallel inputs and the parallel outputs which enables the user to provide a “clean” reference source for the PLL and to accept a separate external clock which is used exclusively to reliably clock data into the device. Data can also be clocked in using the REFCLK.

Data is input to each channel of the S2102 nominally as a 10 bit wide word. An input FIFO and a clock input, TBCx, are provided for each channel of the S2102. The device can operate in two different modes. The S2102 can be configured to use either the TCLKx (TCLK MODE) input or the REFCLK input (REFCLK MODE). In TCLK or REFCLK mode, 10 bits of data are clocked into its FIFO with the TBCx provided with each 10 bits. Table 1 provides a summary of the input modes of the S2102.

Operation in the TBC MODE makes it easier for users to meet the relatively narrow setup and hold time window required by the 106.25 Mbps 10-bit interface. The TBC signal is used to clock the data into an internal holding register and the S2102 synchronizes its internal data flow to ensure stable operation. However, regardless of the clock mode, REFCLK is always the VCO reference clock. This facilitates the provision of a clean reference clock resulting in minimum jitter on the serial output. The TBC must be frequency locked to REFCLK, but may have an arbitrary phase relationship. Adjustment of internal timing of the S2102 is performed during reset. Once synchronized, the user must ensure that the timing of the TBC signal does not change by more than ± 3 ns relative to the REFCLK.

Figure 5 demonstrates the flexibility afforded by the S2102. A low jitter reference is provided directly to the S2102 at either 1/10 or 1/20 the serial data rate. This ensures minimum jitter in the synthesized clock used for serial data transmission. A system clock output at the parallel word rate, TCLKO, is derived from the PLL and provided to the upstream circuit as a system clock. The frequency of this output is constant at the parallel word rate, 1/10 the serial data

Table 1. Input Modes

TMODE	Operation
0	REFCLK Mode. REFCLK used to clock data into FIFOs for all channels.
1	TBC Mode. TBCx used to clock data into FIFOs for all channels.

Note that internal synchronization of FIFOs is performed upon de-assertion of RESET.

Figure 5. DIN Data Clocking with TBC

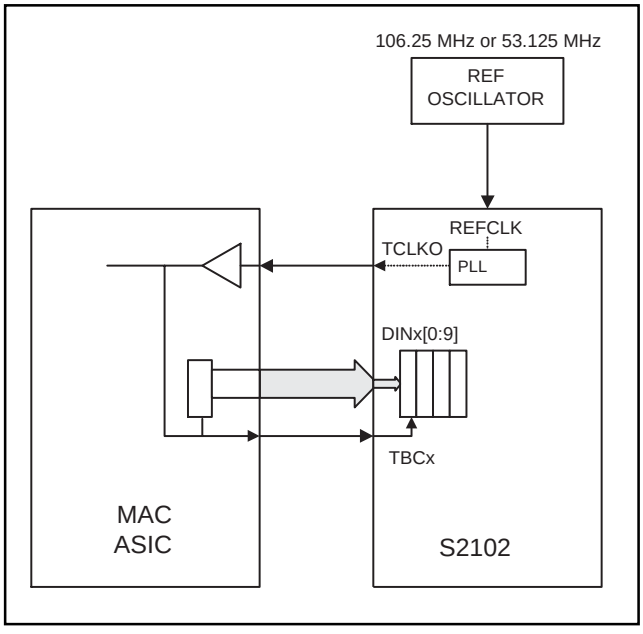


Figure 6. FC DIN Clocking with REFCLK

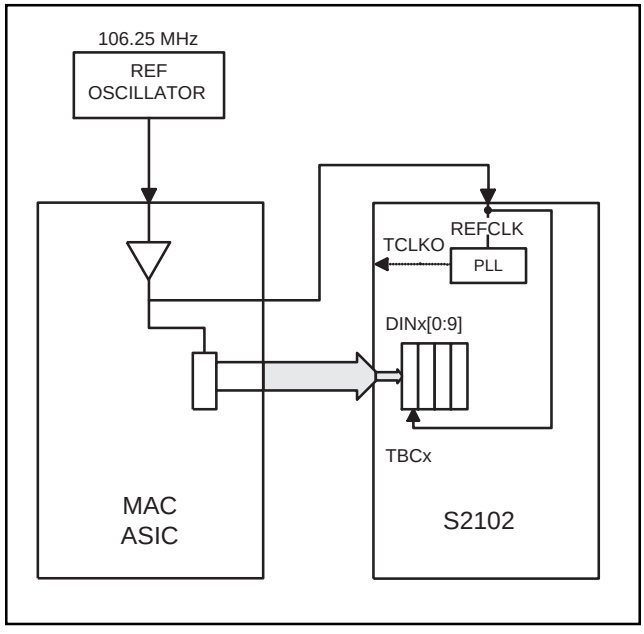


Table 2. Data to 8B/10B Alphabetic Representation

	Data Byte									
DIN[0:9] or DOUT[0:9]	0	1	2	3	4	5	6	7	8	9
8B/10B Alphanumeric Representation	a	b	c	d	e	i	f	g	h	j

Table 3. Operating Rates

RATE	CLKSEL	REFCLK Frequency	Serial Output Rate	TCLKO Frequency
0	0	106.25 MHz	1062.5 MHz	106.25 MHz
0	1	53.125 MHz	1062.5 MHz	106.25 MHz
1	0	53.125 MHz	531.25 MHz	53.125 MHz
1	1	26.563 MHz	531.25 MHz	53.125 MHz

rate, regardless of whether the reference is provided at 1/10 or 1/20 the serial data rate. This clock can be buffered as required without concern about added delay. There is no phase requirement between TCLKO and TBCx, which is provided back to the S2102, other than that they remain within ± 3ns of the phase relationship established at reset.

The S2102 also supports the traditional REFCLK clocking found in many Fibre Channel applications and is illustrated in Figure 6.

Half Rate Operation

The S2102 supports full and half rate operation for all modes of operation. When RATE is LOW, the S2102 serial data rate equals the VCO frequency. When RATE is HIGH, the VCO is divided by 2 before being provided to the chip. Thus the S2102 can support Fibre Channel and serial backplane functions at both full and half the VCO rate. See Table 3.

Parallel to Serial Conversion

The 10-bit parallel data handled by the S2102 device should be from a DC-balanced encoding scheme, such as the 8B/10B transmission code, in which information to be transmitted is encoded, 8 bits at a time, into a 10-bit transmission character and must be compliant with ANSI X3.230 FC-PH (Fibre Channel Physical and Signaling Interface).

The 8B/10B transmission code includes serial encoding and decoding rules, special characters, and error control. Information is encoded, 8 bits at a time, into a 10 bit transmission character. The characters defined by this code ensure that short run lengths and enough transitions are present in the serial bit stream to make clock recovery possible at the receiver. The encoding also greatly increases the likelihood of detecting any single or multiple errors that might occur during the transmission and reception of data[1].

Table 2 identifies the mapping of the 8B/10B characters to the data inputs of the S2102. The S2102 will serialize the parallel data for each channel and will transmit bit “a” or DIN[0] first.

Frequency Synthesizer (PLL)

The S2102 synthesizes a serial transmit clock from the reference signal. Upon startup, the S2102 will obtain phase and frequency lock within 2500 bit times after the start of receiving reference clock inputs. Reliable locking of the transmit PLL is assured, but a lock-detect output is NOT provided.

Reference Clock Input

The reference clock input must be supplied with a low-jitter clock source. All reference clocks in a system must be within 200 ppm of each other to ensure that the clock recovery units can lock to the serial data.

The frequency of the reference clock must be either 1/10 the serial data rate, CLKSEL = 0, or 1/20 the serial data rate, CLKSEL=1. In both cases the frequency of the parallel word rate output, TCLKO, is constant at 1/10 the serial data rate. See Table 3.

Serial Data Outputs

The S2102 provides LVPECL level serial outputs. The serial outputs do not require output pulldown resistors. Outputs are designed to perform optimally when AC-coupled.

Transmit FIFO Initialization

The transmit FIFO must be initialized after stable delivery of data and TBC to the parallel interface, and before entering the normal operational state of the circuit. FIFO initialization is performed upon the de-assertion of the RESET signal. TCLKO will operate normally regardless of the state of RESET.

1. A.X. Widner and P.A. Franaszek, "A Byte-Oriented DC Balanced (0,4) 8B/10B Transmission Code," IBM Research Report RC9391, May 1982.

RECEIVER DESCRIPTION

Each receiver channel is designed to implement a Serial Backplane receiver function through the physical layer. A block diagram showing the basic function is provided in Figure 4.

Whenever a signal is present, the receiver attempts to recover the serial clock from the received data stream. After acquiring bit synchronization, the S2102 searches the serial bit stream for the occurrence of a K28.5 character on which to perform word synchronization. Once synchronization on both bit and word boundaries is achieved, the receiver provides the word-aligned data on its parallel outputs.

Data Input

A differential input receiver is provided for each channel of the S2102. Each channel has a loopback mode in which the serial data from the transmitter replaces external serial data. The loopback function for each channel is enabled by its respective LPEN input.

The high speed serial inputs to the S2102 are internally biased to VDD-1.3V. All that is required externally are AC-coupling and line-to-line differential termination.

Clock Recovery Function

Clock recovery is performed on the input data stream for each channel of the S2102. The receiver PLL has been optimized for the anticipated needs of Serial Backplane systems. A simple state machine in the clock recovery macro decides whether to acquire lock from the serial data input or from the reference clock. The decision is based upon the frequency and run length of the serial data inputs. If at any time the frequency or run length checks are violated, the state machine forces the VCO to lock to the reference clock. This allows the VCO to maintain the correct frequency in the absence of data.

The “lock to reference” frequency criteria ensure that the S2102 will respond to variations in the serial data input frequency (compared to the reference frequency). The new lock state is dependent upon the current lock state, as shown in Table 4.

The run-length criteria ensure that the S2102 will respond appropriately and quickly to a loss of signal. The run-length checker flags a condition of consecutive ones or zeros across 12 parallel words. Thus 119 or less consecutive ones or zeros does not cause signal loss, 129 or more causes signal loss, and 120 - 128 may or may not, depending on how the data aligns across byte boundaries.

If both the off-frequency detect circuitry test and the run-length test are satisfied, the CRU will attempt to lock to the incoming data. It is possible for the run length test to be satisfied due to noise on the inputs, even if no signal is present. In this case the receiver VCO will maintain frequency accuracy to within 100 ppm of the target rate as determined by REFCLK.

In any transfer of PLL control from the serial data to the reference clock, the RBC1/0x outputs remain phase continuous and glitch free, assuring the integrity of downstream clocking.

Reference Clock Input

A single reference clock, which serves both transmitter and receiver, must be provided from a low jitter clock source. The frequency of the received data stream (divided-by-10 or -20) must be within 200 ppm of the reference clock to ensure reliable locking of the receiver PLL.

Table 4. Lock to Reference Frequency Criteria

Current Lock State	PLL Frequency (vs. REFCLK)	New Lock State
Locked	< 488 ppm	Locked
	488 to 732 ppm	Undetermined
	> 732 ppm	Unlocked
Unlocked	< 244 ppm	Locked
	244 to 366 ppm	Undetermined
	> 366 ppm	Unlocked

Serial to Parallel Conversion

Once bit synchronization has been attained by the S2102 CRU, the S2102 must synchronize to the 10 bit word boundary. Word synchronization in the S2102 is accomplished by detecting and aligning to the 8B/10B K28.5 codeword. The S2102 will detect and byte-align to either polarity of the K28.5. Each channel of the S2102 will detect and align to a K28.5 anywhere in the data stream. For TCLK ot REFCLK mode operation, the presence of a K28.5 is indicated for each channel by the assertion of the COM_DETx signal.

Data Output

Data is output on the DOUT[0:9] outputs. The COM_DETx signal is used to indicate the reception of a valid K28.5 character.

The S2102 TTL outputs are optimized to drive 65Ω line impedances. Internal source matching provides good performance on unterminated lines of reasonable length.

Parallel Output Clock Rate

Two output clock modes are supported, as shown in Table 5. When CMODE is High, a complementary TTL clock at the data rate is provided on the RBC1/0x outputs. Data should be clocked on the rising edge of RBC1x. When CMODE is Low, a complementary TTL clock at half the data rate is provided. Data should be latched on the rising edge of RBC1x and the rising edge of RBC0x.

In Fibre Channel applications, multiple consecutive K28.5 characters cannot be generated. However, for serial backplane applications this can occur. The S2102 must be able to operate properly when multiple K28.5 characters are received. After the first K28.5 is detected and aligned, the RBC1/0x clock will operate without glitches or loss of cycles.

Receiver Output Clocking

The S2102 parallel output clock source is determined by the TMODE selection. When REFCLK clocking is selected (TMODE = Low), the parallel output clocks (RCxP/N) are sourced from the TCLKA input. When TCLK clocking is selected (External Clocking Mode), the parallel output clocks are derived from the recovered clock from each channel. Table 5A describes the receiver output clocking options available.

When TCLKA is the output clock source, REFCLK and TCLKA must equal the parallel word rate (CLKSEL = Low). Additionally, the recovered clocks and the clock input on TCLKA must be frequency locked in order to avoid overflow/underflow of the internal FIFOs. The propagation delay between TCLKA and DOUTx, listed in Table 21, shows that the phase delay between TCLKA and the RCxP/N outputs may vary more than a bit time based on process variation.

The recommended clocking configuration for external clocking mode (REFCLK input clocking) is shown in Figure 7. TCLKA is sourced from TCLKO, which is frequency locked to the Reference clock input.

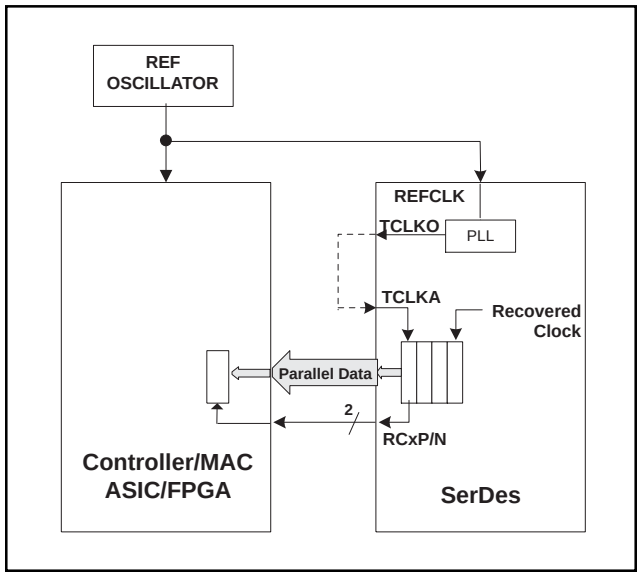
Table 5. Output Clock Mode

Mode	CMODE	RBC1/0x Freq
Half Clock Mode	0	53.125 MHz
Full Clock Mode	1	106.25 MHz

Table 5A. S2102 Data Clocking

TMODE	Input Clock Source	Output Clock Source
0	REFCLK	TBCA
1	TBCx	RBCx

Figure 7. External Receiver Clocking



OTHER OPERATING MODES

Operating Frequency Rate

The S2102 is designed to operate at the Fibre Channel rate of 1.062 GHz.

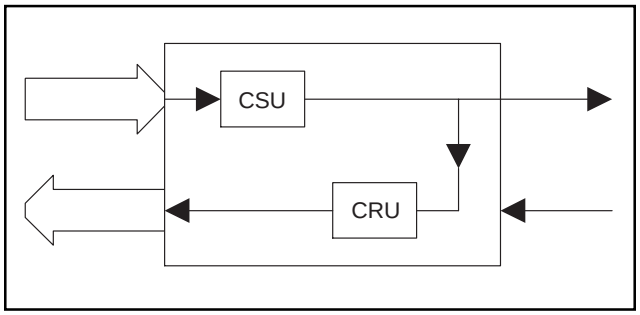
Loopback Mode

When loopback mode is enabled, the serial data from the transmitter is provided to the serial input of the receiver, as shown in Figure 8. This provides the ability to perform system diagnostics and off-line testing of the interface to verify the integrity of the serial channel. Loopback mode is enabled independently for each channel using its respective loopback-enable input, LPEN.

Test Modes

The RESET pin is used to initialize the Transmit FIFOs and must be asserted (LOW) prior to entering the normal operational state (see section Transmit FIFO Initialization).

Figure 8. S2102 Diagnostic Loopback Operation



Note: Serial output data remains active during loopback operation to enable other system tests to be performed.

JTAG TESTING

The JTAG implementation for the S2102 is compliant with the IEEE1149.1 requirements. JTAG is used to test the connectivity of the pins on the chip. The TAP, (Test Access Port), provides access to the test logic of the chip. When TRST is asserted the TAP is initialized. TAP is a state machine that is controlled by TMS. The test instruction and data are loaded through TDI on the rising edge of TCK. When TMS is high the test instruction is loaded into the instruction register. When TMS is low the test data is loaded into the data register. TDO changes on the falling edge of TCK. All input pins, including clocks, that have boundary scan are observe only. They can be sampled in either normal operational or test mode. All output pins that have boundary scan, are observe and control. They can be sampled as they are driven out of the chip in normal operational mode, and they can be driven out of the chip in test mode using the Extest instruction. Since JTAG testing operates only on digital signals there are some pins with analog signals that JTAG does not cover. The JTAG implementation has the three required instruction, Bypass, Extest, and Sample/Preload.

Instruction	Code
BYPASS	11
EXTEST	00
SAMPLE/PRELOAD	01
ID CODE	10

JTAG Instruction Description:

The BYPASS register contains a single shift-register stage and is used to provide a minimum-length serial path between the TDI and TDO pins of a component when no test operation of that component is required. This allows more rapid movement of test data to and from other components on a board that are required to perform test operations.

The EXTEST instruction allows testing of off-chip circuitry and board level interconnections. Data would typically be loaded onto the latched parallel outputs of boundary-scan shift-register stages using the SAMPLE/PRELOAD instruction prior to selection of the EXTEST instruction.

The SAMPLE/PRELOAD instruction allows a snapshot of the normal operation of the component to be taken and examined. It also allows data values to be loaded onto the latched parallel outputs of the boundary-scan shift register prior to selection of the other boundary-scan test instructions.

The following table provides a list of the pins that are JTAG tested. Each port has a boundary scan register (BSR), unless otherwise noted. The following features are described: the JTAG mode of each register (input, output2, or internal (refers to an internal package pin)), the direction of the port if it has a boundary scan register (in or out), and the position of this register on the scan chain.

Table 6. JTAG Pin Assignments

S2102 Pin Name	Core_Scan Port Name	JTAG Mode	Routing In	Routing Out
TESTMODE2	testmode_2	Input	0	-
CMODE	cmode	Input	1	-
TESTMODE	testmode_0	Input	2	-
		Internal	3	-
LPENB	lpenb	Input	4	-
		Internal	5	-
LPENA	lpena	Input	6	-
CLKSEL	clksel	Input	7	-
TMODE	tmode	Input	8	-
		Internal	9	-
RESET	reset	Input	10	-
REFCLK	refclk	Input	11	-
TCLKO	transmit_clk_ buf_out	Output2	-	12
		Internal	13-22	-
TESTMODE1	testmode_1	Input	23	-
DINB9	tdatain_b (9)	Input	24	-
DINB8	tdatain_b (8)	Input	25	-
DINB7	tdatain_b (7)	Input	26	-
DINB6	tdatain_b (6)	Input	27	-
DINB5	tdatain_b (5)	Input	28	-
DINB4	tdatain_b (4)	Input	29	-
DINB3	tdatain_b (3)	Input	30	-
DINB2	tdatain_b (2)	Input	31	-
DINB1	tdatain_b (1)	Input	32	-
DINB0	tdatain_b (0)	Input	33	-
TBCB	tclkb	Input	34	-
		Internal	35-45	-
DINA9	tdatain_a (9)	Input	46	-
DINA8	tdatain_a (8)	Input	47	-
DINA7	tdatain_a (7)	Input	48	-
DINA6	tdatain_a (6)	Input	49	-
DINA5	tdatain_a (5)	Input	50	-
DINA4	tdatain_a (4)	Input	51	-
DINA3	tdatain_a (3)	Input	52	-
DINA2	tdatain_a (2)	Input	53	-
DINA1	tdatain_a (1)	Input	54	-
DINA0	tdatain_a (0)	Input	55	-
TBCA	tclka	Input	56	-
		Internal	-	57-69
RBC1B	rcbp	Output2	-	70
RBC0B	rcbn	Output2	-	71
DOUTB7	rdataout_b (7)	Output2	-	72
DOUTB6	rdataout_b (6)	Output2	-	73
DOUTB5	rdataout_b (5)	Output2	-	74
DOUTB4	rdataout_b (4)	Output2	-	75
DOUTB3	rdataout_b (3)	Output2	-	76
DOUTB2	rdataout_b (2)	Output2	-	77
DOUTB1	rdataout_b (1)	Output2	-	78
DOUTB0	rdataout_b (0)	Output2	-	79
DOUTB9	rdataout_b (9)	Output2	-	80
COM_DETB	eofd_b	Output2	-	81
DOUTB8	rdataout_b (8)	Output2	-	82
		Internal	-	83-95
RBC1A	rcap	Output2	-	96
RBC0A	rcan	Output2	-	97
DOUTA9	rdataout_a (9)	Output2	-	98
DOUTA7	rdataout_a (7)	Output2	-	99
DOUTA6	rdataout_a (6)	Output2	-	100
DOUTA5	rdataout_a (5)	Output2	-	101
DOUTA4	rdataout_a (4)	Output2	-	102
DOUTA3	rdataout_a (3)	Output2	-	103
DOUTA2	rdataout_a (2)	Output2	-	104
DOUTA1	rdataout_a (1)	Output2	-	105
DOUTA0	rdataout_a (0)	Output2	-	106
COM_DETA	eofd_a	Output2	-	107
DOUTA8	rdataout_a (8)	Output2	-	108
		Internal	-	109
JTAG Control Pins (Ports that do not have a Boundary Scan Register)				
TCK	jtag_tck	-	-	-
TDI	jtag_tdi	-	-	-
TDO	jtag_tdo	-	-	-
TMS	jtag_tms	-	-	-
TRS	jtag_trs	-	-	-
Pins not JTAG Tested				
TXAP	-	-	-	-
TXAN	-	-	-	-
TXBP	-	-	-	-
TXBN	-	-	-	-
RATE	-	-	-	-
RXAP	-	-	-	-
RXAN	-	-	-	-
RXBP	-	-	-	-
RXBN	-	-	-	-

Table 7. Transmitter Input Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
DINA9 DINA8 DINA7 DINA6 DINA5 DINA4 DINA3 DINA2 DINA1 DINA0	TTL	I	T15 R13 P12 T14 R12 P11 T13 R11 T12 P10	Transmit Data for Channel A. Parallel data on this bus is clocked in on the rising edge of TBCA or REFCLK.
TBCA	TTL	I	R10	Transmit Byte Clock A. When TMODE is High, this signal is used to clock Data on DINA[0:9] into the S2102. When TMODE is Low, TBCA is ignored.
DINB9 DINB8 DINB7 DINB6 DINB5 DINB4 DINB3 DINB2 DINB1 DINB0	TTL	I	L14 M16 M15 M14 N16 N15 N14 P16 P15 R16	Transmit Data for Channel B. Parallel data on this bus is clocked in on the rising edge of TBCB or REFCLK.
TBCB	TTL	I	P14	Transmit Byte Clock B. When TMODE is High, this signal is used to clock Data on DINB[0:9] into the S2102. When TMODE is Low, TBCB is ignored.

Table 8. Transmitter Output Signals

Pin Name	Level	I/O	Pin #	Description
TXAP TXAN	Diff. LVPECL	O	D16 E16	High speed serial outputs for Channel A.
TXBP TXBN	Diff. LVPECL	O	G16 F16	High speed serial outputs for Channel B.
TCLKO	TTL	O	K15	TTL Output Clock at the Parallel data rate. This clock is provided for use by up-stream circuitry.

Table 9. Mode Control Signals

Pin Name	Level	I/O	Pin #	Description
TESTMODE	TTL	I	D3	Test Mode Control. Keep Low for normal operation.
TESTMODE1	TTL	I	L15	Test Mode Control. Keep Low for normal operation.
TESTMODE2	TTL	I	C4	Test Mode Control. Keep Low for normal operation.
TMODE	TTL	I	A13	Transfer Mode Control. Controls the source of the clock used to input and output data to and from the S2102. When TMODE is Low, REFCLK is used to clock data on DINx[0:9] into the S2102. TBCA is used to clock parallel data DOUTx[0:9] out of the device. When TMODE is High, the TBCx inputs are used to clock data into their respective channels. The output clocks are derived from the receivers' CRUs.
CLKSEL	TTL	I	B11	REFCLK Select Input. This signal configures the PLL for the appropriate REFCLK frequency. When CLKSEL = 0, the REFCLK frequency equals the parallel word rate. When CLKSEL = 1, the REFCLK frequency is half the parallel data rate.
REFCLK	TTL	I	J14	Reference Clock is used for the transmit VCO and frequency check for the clock recovered from the receiver serial data.
RESET	TTL	I	B15	When Low, the S2102 is held in reset. The receiver PLL is forced to lock to the REFCLK. The FIFOs are initialized on the rising edge of RESET. When High, the S2102 operates normally.
RATE	TTL	I	C11	When Low, the S2102 operates with the serial output rate equal to the VCO frequency. When High, the S2102 operates with the VCO internally divided by 2 for all functions.

Note: All TTL inputs except REFCLK have internal pull-up networks.

Table 10. Receiver Output Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
DOUTA9 DOUTA8 DOUTA7 DOUTA6 DOUTA5 DOUTA4 DOUTA3 DOUTA2 DOUTA1 DOUTA0	TTL	O	J2 G2 L2 L1 K2 K1 J3 J1 H3 H2	Channel A Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of RBC1A in full clock mode and valid on the rising edge of both RBC1A and RBC0A in half clock mode.
COM_DETA	TTL	O	G1	Channel A Comma Detect. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTA[0:9].
RBC1A RBC0A	TTL	O	M1 L3	Receive Byte Clocks. Parallel receive data, DOUTA[0:9] and COM_DETA are valid on the rising edge of RBC1A when in full clock mode and valid on the rising edge of both RBC1A and RBC0A in half clock mode.
DOUTB9 DOUTB8 DOUTB7 DOUTB6 DOUTB5 DOUTB4 DOUTB3 DOUTB2 DOUTB1 DOUTB0	TTL	O	P4 P2 P8 T5 R6 P6 R5 T3 P5 R3	Channel B Receiver Data Outputs. Parallel data on this bus is valid on the rising edge of RBC1B in full clock mode and valid on the rising edge of both RBC1B and RBC0B in half clock mode.
COM_DETB	TTL	O	P3	Channel B Comma Detect. A High on this output indicates that a valid K28.5 has been detected and is present on the parallel data outputs DOUTB[0:9].
RBC1B RBC0B	TTL	O	R7 P7	Receive Byte Clocks. Parallel receive data, DOUTB[0:9] and COM_DETB are valid on the rising edge of RBC1B when in full clock mode and valid on the rising edge of both RBC1B and RBC0B in half clock mode.

Table 11. Receiver Input Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
RXAP RXAN	Diff. LVPECL	I	A3 A4	Differential LVPECL compatible inputs for channel A. RXAP is the positive input, RXAN is the negative. Internally biased to VDD -1.3V for AC coupled applications.
RXBP RXBN	Diff. LVPECL	I	A8 A9	Differential LVPECL compatible inputs for channel B. RXBP is the positive input, RXBN is the negative. Internally biased to VDD -1.3V for AC coupled applications.

Table 12. Receiver Control Signals

Pin Name	Level	I/O	Pin #	Description
LPENA LPENB	TTL	I	C14 H14	Loopback Enable. When Low, input source is the high speed serial input for each channel. When High, the serial output for each channel is looped back to its input.
CMODE	TTL	I	C2	Clock Mode Control. When Low, the parallel output clocks (RBC1/0x) rate is equal to 1/2 the data rate. When High, the parallel output clocks (RBC1/0x) rate is equal to the data rate.

Table 13. Power and Ground Signals

Pin Name	Qty.	Pin #	Description
VDDA	4	A6, B4, B13, C8	Analog Power (VDD) low noise.
VSSA	3	A2, B8, C13	Analog Ground (VSS).
VDD	3	B12, C6, C9	Power for High Speed Circuitry (VDD).
VSS VSSSUB	8	A7, A11, A12, A14, B5, B7, C7, C12	Ground for High Speed Circuitry (VSS).

Table 13. Power and Ground Signals (Continued)

Pin Name	Qty.	Pin #	Description
PECLPWR	4	D15, F15, G14, H15	PECL Power (VDD)
PECLGND	2	C16 J16	PECL Ground (VSS)
DIGPWR	6	B2, C1, D2, J15, N1, P9	Core Circuitry Power (VDD)
DIGGND	8	C3, D1, E2, E3, K16, R1, T1, T11	Core Circuitry Ground (VSS)
TTLPWR	8	F1, G3, H1, M2, P1, R4, R8, T7	Power for TTL I/O (VDD)
TTLGND	10	E1, F2, F3, K3, M3, N3, R2, T2, T4, T8	Ground for TTL I/O (VSS)
PWR	2	A16 B1	Power
GND	5	K14, L16, P13, R14, T16	Ground
CAP1 CAP2	2	A15 B14	Pins for external loop filter capacitor
NC	18	A1, A5, B6, B9, B16, C5, C15, D14, E14, E15, F14, G15, N2, R9, R15, T6, T9, T10	Not Connected. Used as test pins. Do Not Connect.

Table 14. JTAG Test Signals

Pin Name	Level	I/O	Pin #	Description
TMS	TTL	I	A10	Test Mode Select. Enables JTAG testing of device.
TCK	TTL	I	B10	Test Clock. JTAG test clock.
TDI	TTL	I	C10	Test Data In. JTAG data input.
TDO	TTL	O TRISTATE	H16	Test Data Out. JTAG data output. Can be high impedance under JTAG controller command.
TRS	TTL	I	B3	Test Reset. Resets JTAG test state machine.

Figure 9. S2102 Pinout (Bottom View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T
1	NC	PWR	DIGPWR	DIGGND	TTLGND	TTLPWR	COM_ DETA	TTLPWR	DOUTA2	DOUTA4	DOUTA6	RBC1A	DIGPWR	TTLPWR	DIGGND	DIGGND
2	VSSA	DIGPWR	CMODE	DIGPWR	DIGGND	TTLGND	DOUTA8	DOUTA0	DOUTA9	DOUTA5	DOUTA7	TTLPWR	NC	DOUTB8	TTLGND	TTLGND
3	RXAP	TRS	DIGGND	TEST MODE	DIGGND	TTLGND	TTLPWR	DOUTA1	DOUTA3	TTLGND	RBC0A	TTLGND	TTLGND	COM_ DETB	DOUTB0	DOUTB2
4	RXAN	VDDA	TEST MODE2											DOUTB9	TTLPWR	TTLGND
5	NC	VSSSUB	NC											DOUTB1	DOUTB3	DOUTB6
6	VDDA	NC	VDD											DOUTB4	DOUTB5	NC
7	VSSSUB	VSS	VSS											RBC0B	RBC1B	TTLPWR
8	RXBP	VSSA	VDDA											DOUTB7	TTLPWR	TTLGND
9	RXBN	NC	VDD											DIGPWR	NC	NC
10	TMS	TCK	TDI											DINA0	TBCA	NC
11	VSS	CLKSEL	RATE											DINA4	DINA2	DIGGND
12	VSSSUB	VDD	VSSSUB											DINA7	DINA5	DINA1
13	TMODE	VDDA	VSSA											GND	DINA8	DINA3
14	VSS	CAP2	LPENA	NC	NC	NC	PECL PWR	LPENB	REFCLK	GND	DINB9	DINB6	DINB3	TBCB	GND	DINA6
15	CAP1	RESET	NC	PECL PWR	NC	PECL PWR	NC	PECL PWR	DIGPWR	TCLKO	TEST MODE1	DINB7	DINB4	DINB1	NC	DINA9
16	PWR	NC	PECLGND	TXAP	TXAN	TXBN	TXBP	TDO	PECLGND	DIGGND	GND	DINB8	DINB5	DINB2	DINB0	GND

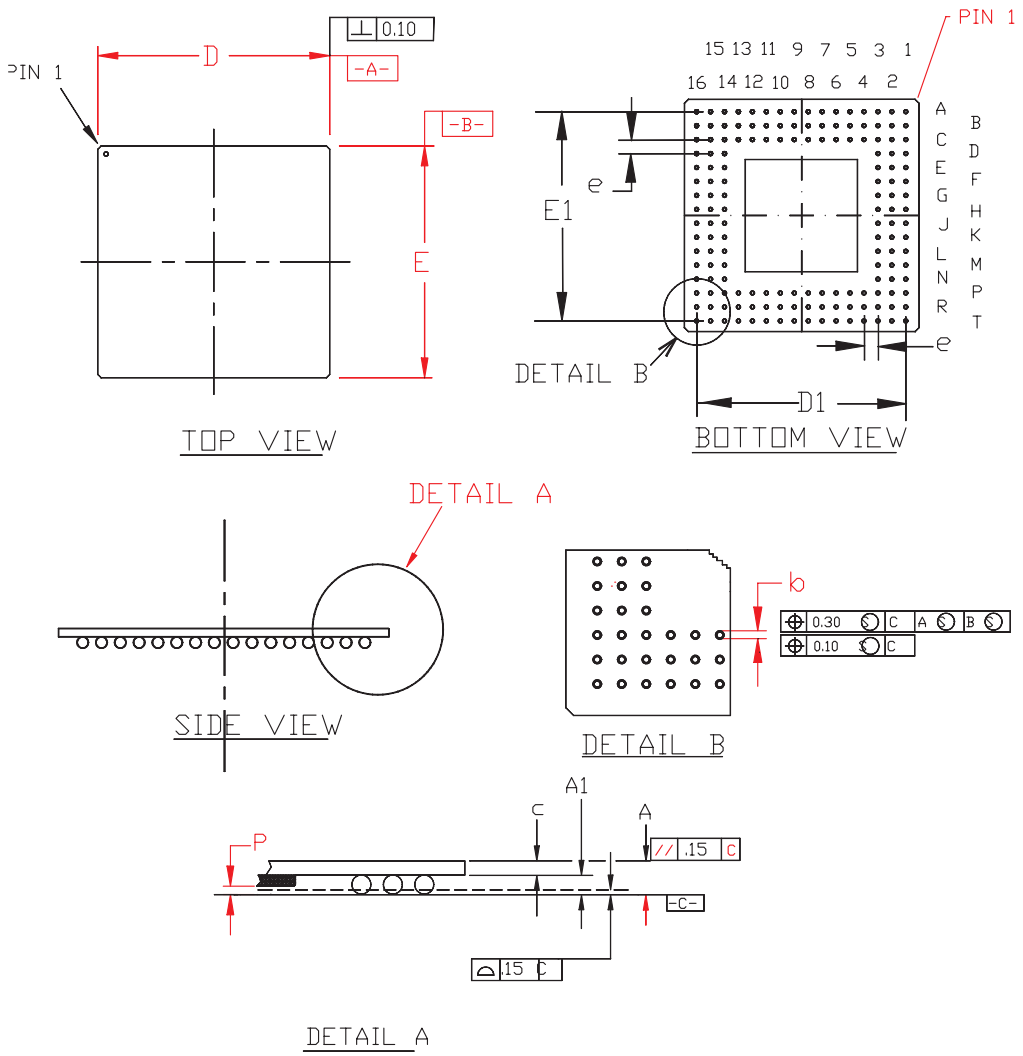
Note: NC used as Test Pins. Do Not Connect.

Figure 10. S2102 Pinout (Top View)

T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
DIGGND	DIGGND	TTLPWR	DIGPWR	RBC1A	DOUTA6	DOUTA4	DOUTA2	TTLPWR	COM_ DETA	TTLPWR	TTLGND	DIGGND	DIGPWR	PWR	NC	1
TTLGND	TTLGND	DOUTB8	NC	TTLPWR	DOUTA7	DOUTA5	DOUTA9	DOUTA0	DOUTA8	TTLGND	DIGGND	DIGPWR	CMODE	DIGPWR	VSSA	2
DOUTB2	DOUTB0	COM_ DETB	TTLGND	TTLGND	RBC0A	TTLGND	DOUTA3	DOUTA1	TTLPWR	TTLGND	DIGGND	TEST MODE	DIGGND	TRS	RXAP	3
TTLGND	TTLPWR	DOUTB9											TEST MODE2	VDDA	RXAN	4
DOUTB6	DOUTB3	DOUTB1											NC	VSSSUB	NC	5
NC	DOUTB5	DOUTB4											VDD	NC	VDDA	6
TTLPWR	RBC1B	RBC0B											VSS	VSS	VSSSUB	7
TTLGND	TTLPWR	DOUTB7											VDDA	VSSA	RXBP	8
NC	NC	DIGPWR											VDD	NC	RXBN	9
NC	TBCA	DINA0											TDI	TCK	TMS	10
DIGGND	DINA2	DINA4											RATE	CLKSEL	VSS	11
DINA1	DINA5	DINA7											VSSSUB	VDD	VSSSUB	12
DINA3	DINA8	GND											VSSA	VDDA	TMODE	13
DINA6	GND	TBCB	DINB3	DINB6	DINB9	GND	REFCLK	LPENB	PECL PWR	NC	NC	NC	LPENA	CAP2	VSS	14
DINA9	NC	DINB1	DINB4	DINB7	TEST MODE1	TCLKO	DIGPWR	PECL PWR	NC	PECL PWR	NC	PECL PWR	NC	RESET	CAP1	15
GND	DINB0	DINB2	DINB5	DINB8	GND	DIGGND	PECLGND	TDO	TXBP	TXBN	TXAN	TXAP	PECLGND	NC	PWR	16

Note: NC used as Test Pins. Do Not Connect.

Figure 11. Compact 21mm x 21mm 156 TBGA Package



DIMENSIONS (are in millimeters)

UNIT	A	A_1	D	D_1	E	E_1	P	b	c	e
MIN	1.45	0.60	20.80	19.05 BSC.	20.80	19.05 BSC.		0.65	0.85	1.27 BSC.
NOM	1.55	0.65	21.00		21.00			0.75	0.90	
MAX	1.65	0.70	21.20		21.20		0.25	0.85	0.95	

Thermal Management

Device	Θja	Θjc
S2102	19.8˚C/W	3.5˚C/W

Figure 12. Transmitter Timing (REFCLK Mode, TMODE = 0)

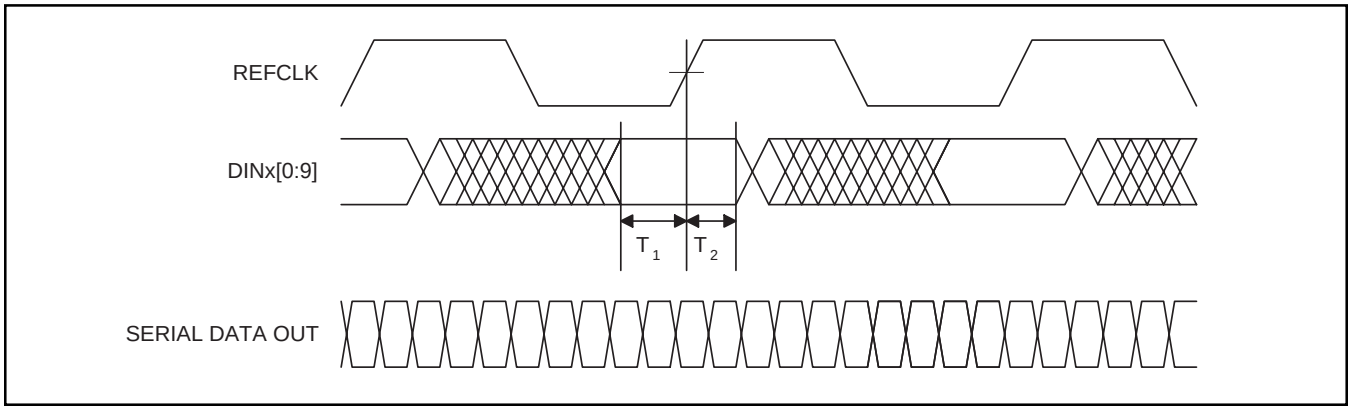


Table 15. S2102 Transmitter Timing (REFCLK Mode, TMODE = 0)

Parameters	Description	Min	Max	Units	Conditions
T_1	Data Setup w.r.t. ↑ REFCLK	0.5	-	ns	See Note 1.
T_2	Data Hold w.r.t. ↑ REFCLK	1.5	-	ns	—

1. All AC measurements are made from the reference voltage levels of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

Figure 13. Transmitter Timing (TBC Mode, TMODE = 1)

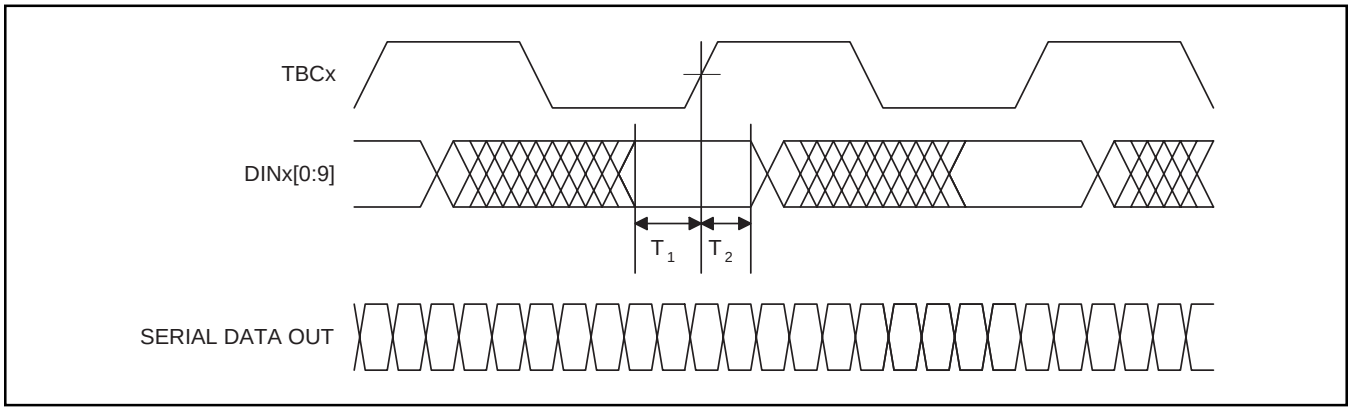


Table 16. S2102 Transmitter Timing (TBC Mode, TMODE = 1)

Parameters	Description	Min	Max	Units	Conditions
T_1	Data Setup w.r.t. ↑ TBC	1.0		ns	See Note 1.
T_2	Data Hold w.r.t. ↑ TBC	0.5		ns	
	Phase drift between TBCx and REFCLK	-3	+3	ns	

1. All AC measurements are made from the reference voltage levels of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

Table 17. S2102 Receiver Timing (Full and Half Clock Mode)

Parameters	Description	Min	Max	Units	Conditions
T_3	Data Setup w.r.t.↑RBC1/0x	3.0		ns	at 1.062 Gbps[1,2] TMODE = 1
T_4	Data Hold w.r.t.↑RBC1/0x	2.5		ns	TMODE = 1
T_5	Data Setup w.r.t.↑RBC1/0x	3.0		ns	at 1.062 Gbps[1,2] TMODE = 1
T_6	Data Hold w.r.t.↑RBC1/0x	2.5		ns	TMODE = 1
T_7	Time from RBC1x rise to RBC0x rise	8.9	9.9	ns	at 1.062 Gbps[1,2]
T_{R1}, T_{F1}	RBC1x Rise and Fall Times		2.4	ns	See note 2. See Figure 19.
T_{R0}, T_{F0}	RBC0x Rise and Fall Times		2.4	ns	See note 2. See Figure 19.
T_{DR}, T_{DF}	DOUTx Rise and Fall Times		2.4	ns	See note 2. See Figure 19.
Duty Cycle	RBC1/0x Duty Cycle	40	60	%	See note 1.

1. Measurements made from the reference voltage levels of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).
2. TTL/CMOS AC timing measurements are assumed to have an output load of 10pf.

Table 18. Receiver Timing (External Clock Mode)

Parameters	Description	Min	Max	Units	Conditions
T_8	TBCA to DOUTx Propagation Delay	3.0	8.0	ns	10 pf capacitance at the end of a 3 inch 50Ω transmission line.

1. Measurements made from the reference voltage levels of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

Figure 14. Receiver Timing (Full Clock Mode, CMODE = 1)

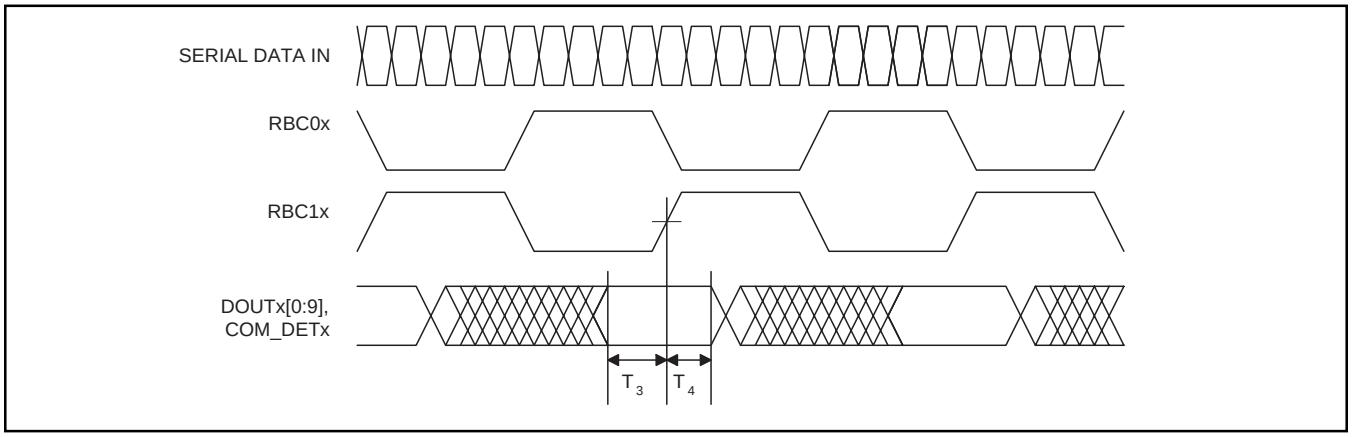


Figure 15. Receiver Timing (Half Clock Mode, CMODE = 0)

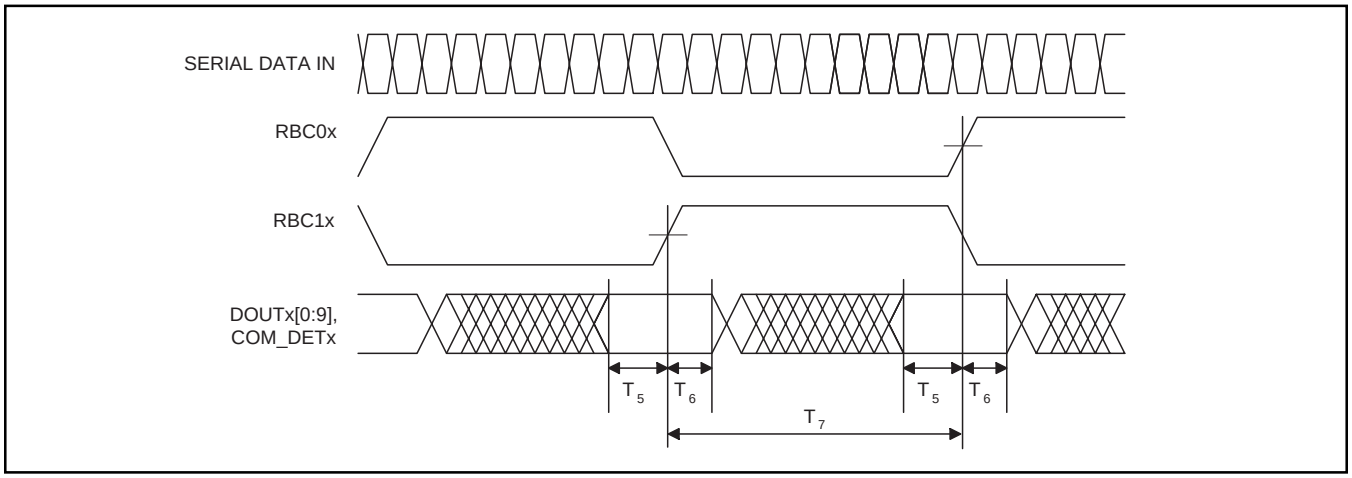


Figure 16. Receiver Timing (External Clock Mode) (TBCA to DATA Propagation Delay, TMODE = 0)

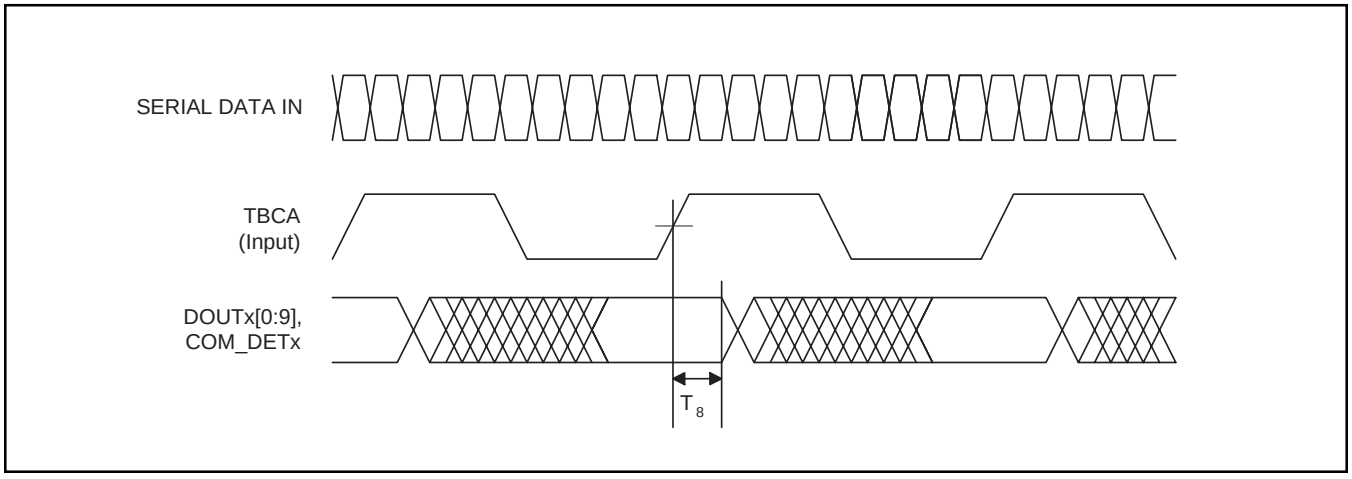


Figure 17. TCLKO Timing

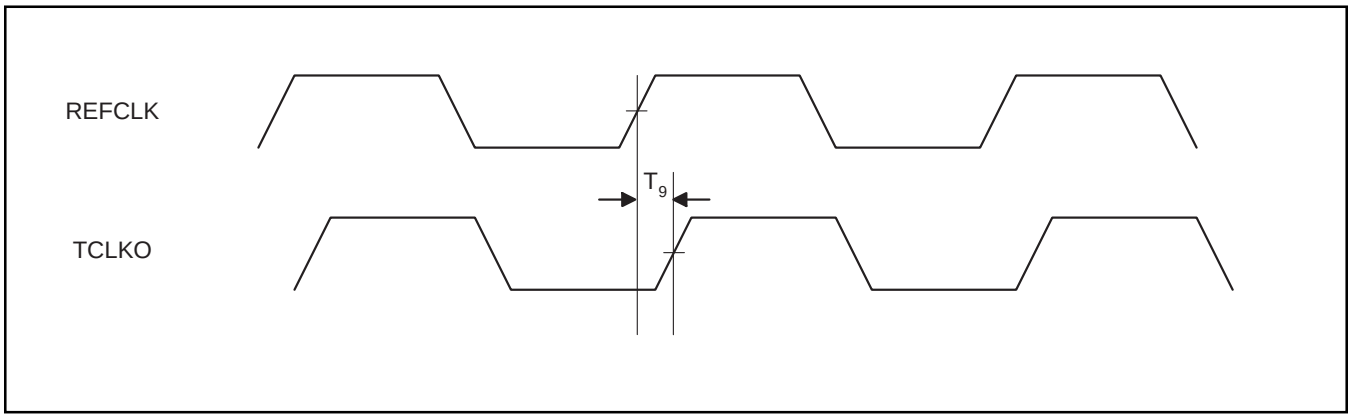


Table 19. S2102 Transmitter (TCLKO Timing)

Parameters	Description	Min	Max	Units	Conditions
T_9	↑ TCLKO w.r.t. ↑ REFCLK	1.0	6.5	ns	
TCLKO Duty Cycle		45%	55%	%	

Note: Measurements are made at 1.4V level of clocks.

Table 20. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature	-65		150	˚C
Voltage on VDD with Respect to GND	-0.5		+5.0	V
Voltage on any TTL Input Pin	-0.5		3.47	V
Voltage on any PECL Input Pin	0		VDD	V
TTL Output Sink Current			8	mA
TTL Output Source Current			8	mA
High Speed PECL Output Source Current			25	mA
ESD Sensitivity [1]	Over 500 V			

1. Human body model.

Table 21. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	0		70	˚C
Junction Temperature Under Bias			130	˚C
Voltage on any Power Pin with respect to GND/VSS	3.13	3.3	3.47	V
Voltage on any TTL Input Pin	0		3.47	V
Voltage on any PECL Input Pin	VDD -2V		VDD	V

Table 22. Reference Clock Requirements

Parameters	Description	Min	Max	Units	Conditions
FT	Frequency Tolerance	-100	+100	ppm	
TD_{1-2}	Symmetry	40	60	%	Duty Cycle at 50% pt.
T_{RCR}, T_{RCF}	REFCLK Rise and Fall Time		2	ns	20% - 80%.
—	Jitter		80	ps	Peak-to-Peak, to maintain ≥ 77% eye opening.

Table 23. Serial Data Timing, Transmit Outputs

Parameters	Description	Min	Typ	Max	Units	Comments
Total Jitter	Serial Data Output total jitter			0.23	UI	Peak-to-Peak.
T_{DJ}	Serial Data Output deterministic jitter			0.08	UI	Peak-to-Peak.
T_{SR}, T_{SF}	Serial Data Output rise and fall time			300	ps	20% - 80%. See Figure 18.

Table 24. Serial Data Timing, Receive Inputs

Parameters	Description	Min	Typ	Max	Units	Comments
T_{LOCK} (Frequency)	Frequency Acquisition Lock Time (Loss of Lock) (1.062 Gbps)			175	µs	8B/10B idle pattern sample basis, from device start up.
T_{FDJ}	Frequency Dependent Jitter Tolerance	0.10			UI	As specified in ANSI X3T11.
T_{DJ}	Deterministic Input Jitter Tolerance	0.38			UI	As specified in ANSI X3T11.
T_{RJ}	Random Input Jitter Tolerance	0.22			UI	As specified in ANSI X3T11.
Input Jitter Tolerance	Serial Data Input total jitter tolerance	0.7			UI	As specified in ANSI X3T11.
R_{SR}, R_{SF}	Serial Data Input rise and fall time			330	ps	20% - 80%. See Figure 18.

Table 25. DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage (TTL)	2.4	2.8	VDD	V	VDD = min I_{OH} = -4mA
V_{OL}	Output Low Voltage (TTL)	GND	.025	0.5	V	VDD = min I_{OL} = 4mA
V_{IH}	Input High Voltage (TTL)	2.0			V	
V_{IL}	Input Low Voltage (TTL)	GND		0.8	V	
I_{IH}	Input High Current (TTL)			40	µA	V_{IN} = 2.4 V, VDD = Max
I_{IL}	Input Low Current (TTL)			600	µA	V_{IN} = .8 V, VDD = Max
IDD	Supply Current		570	660	mA	1010 Pattern.
P_D	Power Dissipation		1.85	2.3	W	1010 Pattern.
V_{DIFF}	Min. differential input voltage swing for differential PECL inputs	100		2600	mV	See Figure 21.
ΔV_{OUT}	Differential Serial Output Voltage Swing	1400		2600	mV	See Figure 20.
C_{IN}	Input Capacitance			3	pf	

OUTPUT LOAD

The S2102 serial outputs do not require output pulldown resistors.

Figure 18. Serial Input/Output Rise and Fall Time

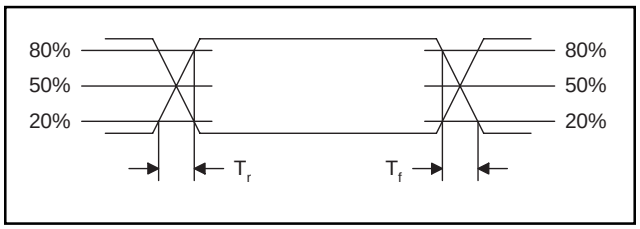


Figure 19. TTL Input/Output Rise and Fall Time

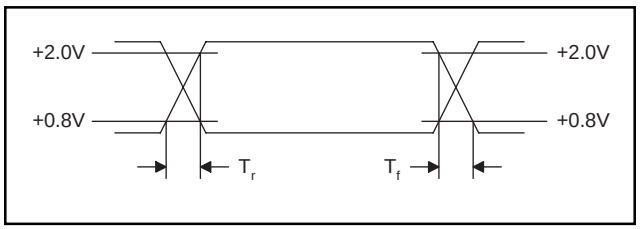


Figure 20. Serial Output Load

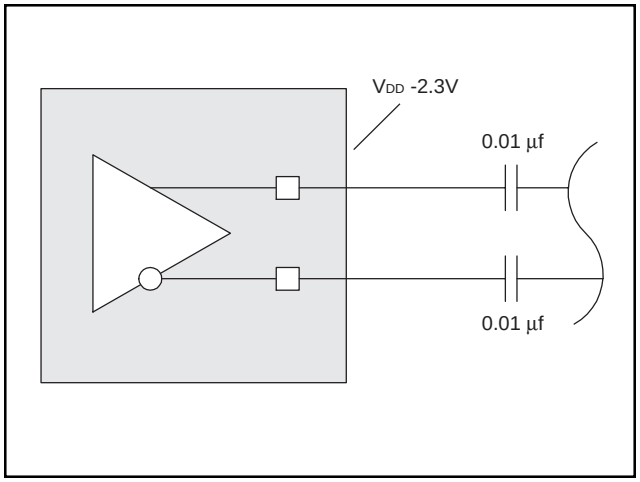


Figure 21. High Speed Differential Inputs

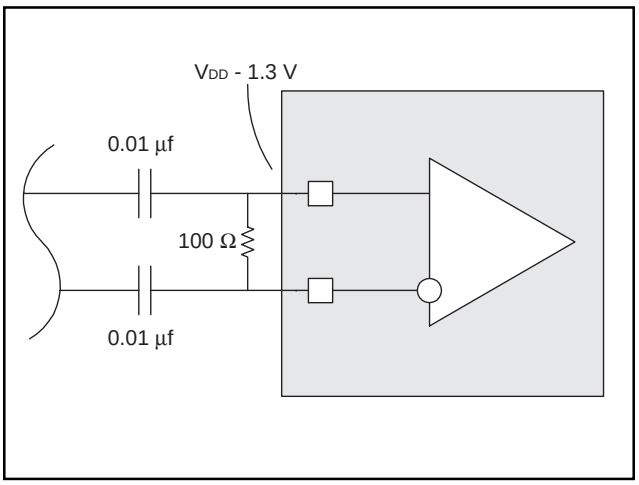


Figure 22. Receiver Input Eye Diagram Jitter Mask

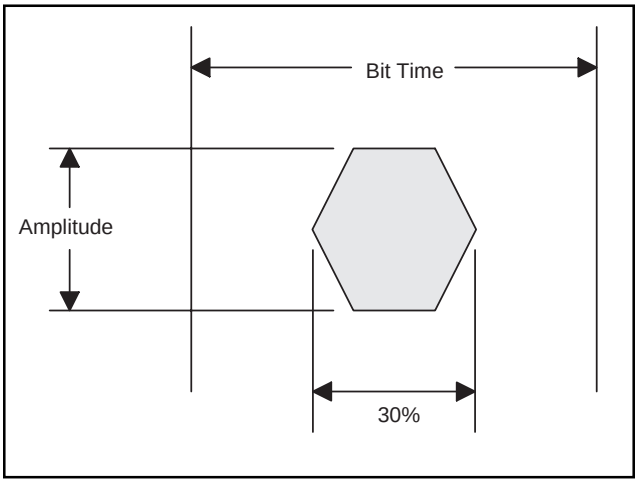
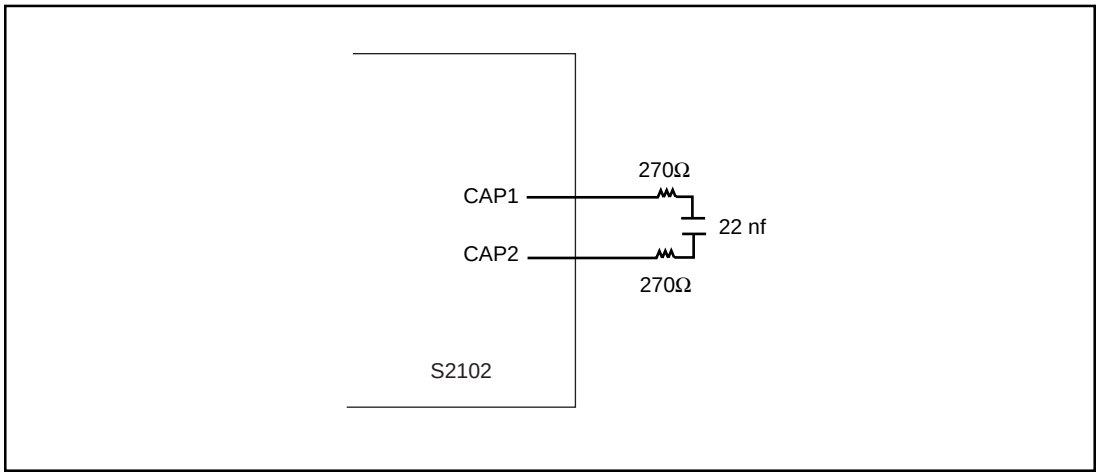
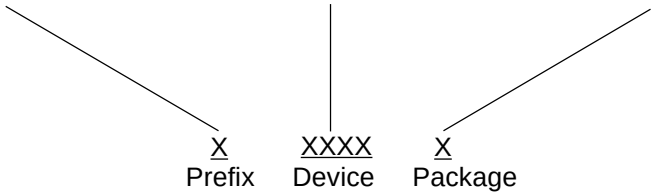


Figure 23. Loop Filter Capacitor Connections



Ordering Information

PREFIX	DEVICE	PACKAGE
S- Integrated Circuit	2102	TB – 156 TBGA



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